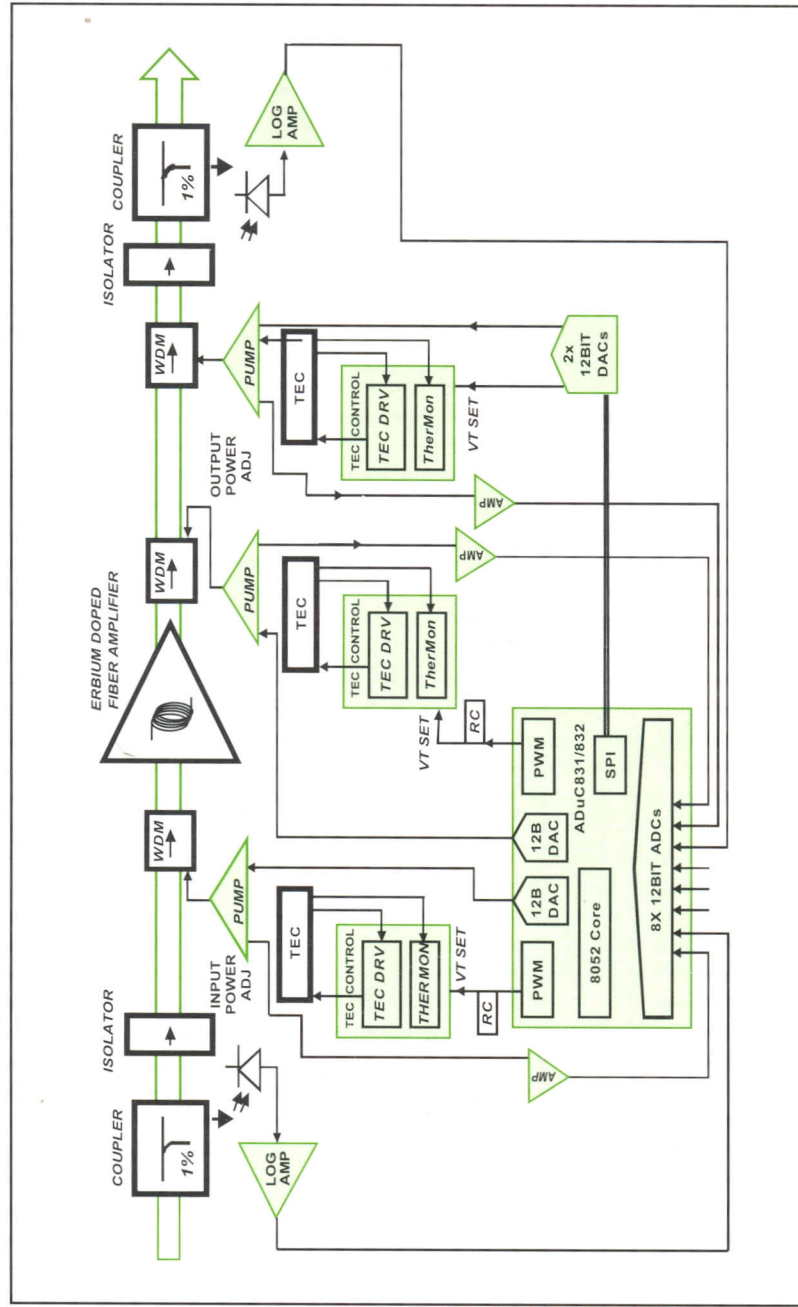


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SECTION 1

Amplifiers

Current Feedback Amplifiers
High-Speed

High-Speed Voltage Feedback

Precision, Low Power

High-Speed Comparator

Instrumentation Amplifier

High-Speed Current Feedback Amplifiers

AD8007/08 Low Distortion High Speed Amp

- Single (AD8007) and Dual (AD8008)
- High Speed
 - 600 MHz, -3 dB Bandwidth (G = +1)
 - 1000 V/μs Slew Rate
- Extremely Low Distortion
 - 2 nd Harmonic: -88dB @ 5MHz -101dB @ 5MHz
 - 3 rd Harmonic: -80dB @ 20MHz -84dB @ 20MHz
- Low Noise
 - $2.7 \text{ nV}/\sqrt{\text{Hz}}$ and $22.5 \text{ pA}/\sqrt{\text{Hz}}$
- 8.8 mA/ Amplifier Typ Supply Current
- Wide Supply Voltage Range 5 V to 12 V
- Small Packaging SOIC-8, μSOIC-8 and SC-70

High-Speed Voltage Feedback Amplifiers

- High-Speed Amplifiers
- Differential Input/Output
- Rail-to-Rail Amplifiers

AD8021 16-Bit Accurate 280 MHz Low Power Op Amp

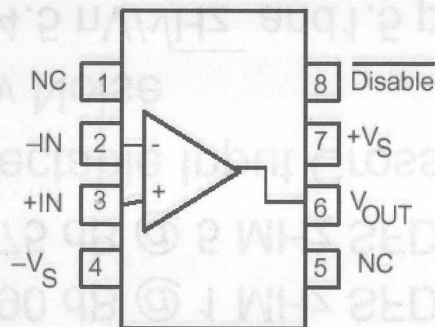
- Noise: 2.1 nV/ $\sqrt{\text{Hz}}$; 2.1 pA/ $\sqrt{\text{Hz}}$ Typ
- High-Speed
 - 480 MHz, 120 V/ μs (–3 dB, G = +1)
 - 150 MHz, 420 V/ μs (–3 dB, G = +10)
 - External compensation
- Low Power 34 mW (6 mA for ± 2.5 V Supplies)
- Power-Down
- Low Distortion:
 - –93 dB 2ND Harmonics at 1 MHz
 - 108 dB 3RD Harmonics at 1 MHz
- Wide Supply Range 5 V to 24 V

AD8029/30/40 Single/Dual/Quad Low-power, High-Speed Rail-to-Rail Input/Output Amps

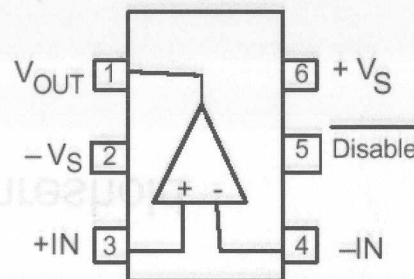
- Rail-to-Rail Input and Output
- High Speed
 - 200 MHz, -3 dB Bandwidth ($G = +1$)
 - 75 V/ μ s Slew Rate
 - 45 ns Settling Time to 0.1%
- Low Cost
- Low Noise
 - 11 nV/ $\sqrt{\text{Hz}}$ and 1 pA/ $\sqrt{\text{Hz}}$
- Wide Supply Range 2.7 V to +12 V
- Low Power
 - 1.3 mA supply current
- Small Packaging SOIC-8, SC70, SOT23-8, TSSOP14

AD8029/30/40 Single/Dual/Quad Low-power, High-Speed Rail-to-Rail Input/Output Amps

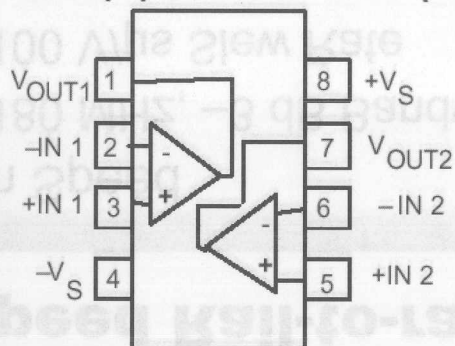
SOIC-8



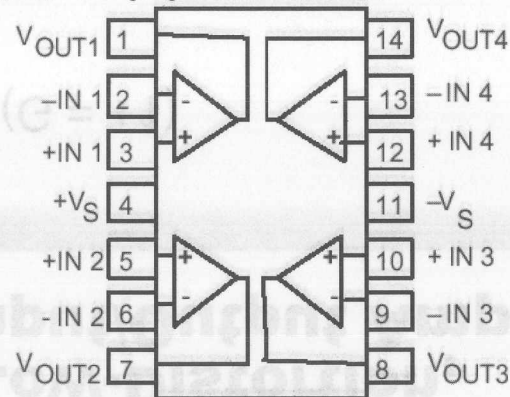
SC70-6 (KS)



SOIC-8 (R) and SOT23-8 (RT)



SOIC-14 (R) and TSSOP-14



AD8027/28 Single/Dual Low-Distortion, High-Speed Rail-to-rail Input/Output Amps

- High Speed
 - 180 MHz, -3 dB Bandwidth ($G = +1$)
 - 100 V/ μ s Slew Rate
- Low Distortion
 - 90 dB @ 1 MHz SFDR
 - 75 dB @ 5 MHz SFDR
- Selectable Input Cross-over Threshold
- Low Noise
 - 4.5 nV/ $\sqrt{\text{Hz}}$ and 1.5 pA/ $\sqrt{\text{Hz}}$
- Low Power 6 mA supply current
- Power Down Disable Feature
- Wide Supply Range 2.7 V to +12 V
- Small Packaging SO-8, SOT23-6, μ SO-10

AD8065/66 Single/Dual High Performance High-Speed *FAST FET™* Op Amp

- FET Input Amplifier
- 1 pA Input Bias Current
- High Speed
 - 150 MHz, -3 dB Bandwidth (G = +1)
 - 180 V/μs Slew Rate
- Low Noise
 - 7.0 nV/√Hz and 5 fA/√Hz
- Wide Supply Voltage Range 5 V to 24 V
- Excellent Distortion Specs
 - SFDR -90 dB @ 1 MHz
- Low Power 6.5 mA/Amplifier Typ Supply Current
- Small Packaging SOIC-8, SOT23-5, m mSOIC
- Low Cost

AD8067 High Gain Bandwidth Product Precision *FAST FET*™ OP AMP

- FET Input Amplifier
- Stable for gains of ≥ 8
- Low Cost
- High Speed
 - 55 MHz, -3 dB Bandwidth ($G = +10$): 500 V/ μ s Slew Rate
- Excellent Distortion Specs
 - SFDR -90dB @ 1MHz
- Low Noise
 - 7.0 nV/ $\sqrt{\text{Hz}}$: 5 fA/ $\sqrt{\text{Hz}}$
- Wide Supply Voltage Range
 - 5 V to 24 V; 6.5 mA Typ Supply Current
- Small Packaging (SOIC-8, SOT23-5)

AD8091/92 Single and Dual Low Cost High Performance Amplifiers

- High-Speed
 - 110 MHz Bandwidth
 - 145 V/μs Slew Rate
- Single Supply Operation
 - +3 V, +5 V
- Low Distortion
 - -80 dBc Total harmonic @ 1 MHz
- Good Video Specification (G=+2)
 - 0.03% Differential Gain
 - 0.03° Differential Phase
- Low Power
 - 4.4 mA/Amplifier
- Rail-to-Rail Output

AD8033/34 Very Low-Cost High-Speed FET Input Amplifiers

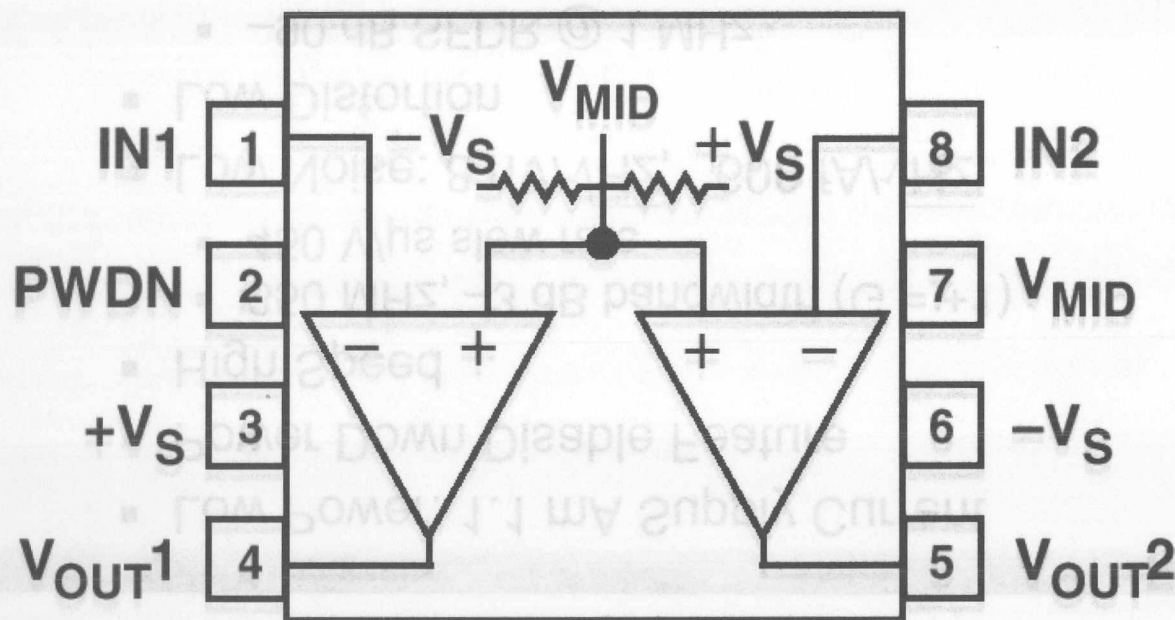
- FET Input Amplifier
 - Single (AD8033) and Dual (AD8034)
- 85 MHz, -3 dB Bandwidth ($G = +1$)
- 80 V/ μ s Slew Rate ($G = -1$)
- Low Noise: 11 nV/ $\sqrt{\text{Hz}}$ 5 fA/ $\sqrt{\text{Hz}}$
- Rail-to-Rail Output
- Wide Supply Voltage Range: 4 V to 24 V
- Low Power
 - 3.3 mA/amplifier typ supply current
- Small Packaging
 - SC-70 (AD8033)
 - SOT23-8 and μ SOIC (AD8034)
 - SOIC-8 (AD8033/34)

AD8038/39 Low Power High-Speed Voltage Feedback Amps

- Low Power: 1.1 mA Supply Current
- Power Down Disable Feature
- High Speed
 - 350 MHz, -3 dB bandwidth ($G = +1$)
 - 450 V/ μ s slew rate
- Low Noise: 8 nV/ $\sqrt{\text{Hz}}$, 600 fA/ $\sqrt{\text{Hz}}$
- Low Distortion
 - -90 dB SFDR @ 1 MHz
 - -65 dB SFDR @ 5 MHz
- Wide Supply Range: +3 V to +12 V
- Small Packaging
 - SOIC-8, SC-70, SOT23-8
- Low Cost

AD8391 xDSL Line Driver

Ideal xDSL line driver for V_O DSL or low power applications such as USB, PCMCIA, or PCI based Customer Premise Equipment (CPE).



Thermal Coastline
8-Pin SOIC

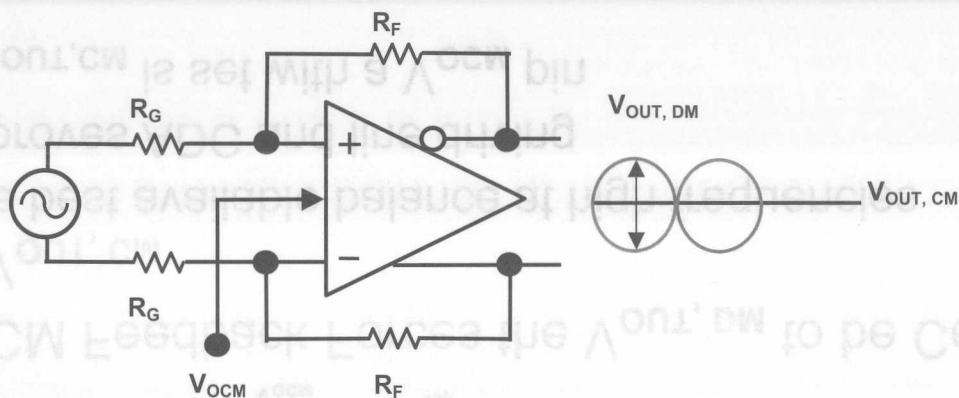
AD8391 xDSL Line Driver

- High Speed
 - 60 MHz bandwidth (–3 dB)
 - 600 V/μs slew rate
- 250 mA Minimum Output Drive Current
- 10 V p-p Output Voltage, Differential Load of $R_L = 21 \Omega$
- Low Power Operation
 - +3.3 V to +12 V power supply range
 - 1-pin logic controlled stand-by, shutdown
 - Low supply current of 19 mA (typical)
- Low Distortion
 - –94 dBc SFDR, 8 Vp-p into differential 21Ω @ 100 kHz
 - 4.5 nV/√Hz input voltage noise density, 100 kHz

Differential Amplifiers

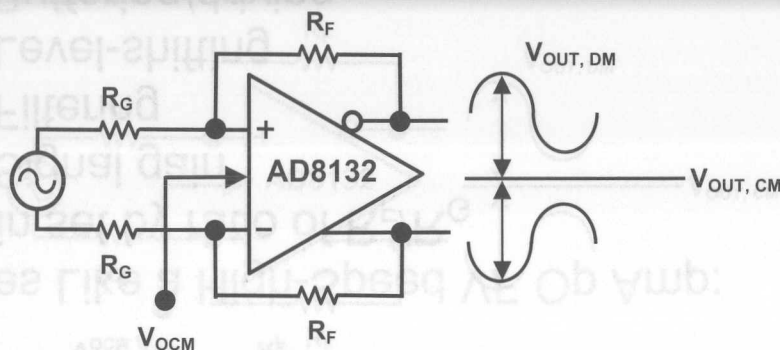
- Low Distortion
 - Low supply current of 18 mA (typical)
 - 1-bit logic controlled stand-by, shutdown
 - +3.3
- Low Power Operation
 - 10 V-b Output Voltage, Differential Load of $R_L = 51 \Omega$
 - 520 mA Minimum Output Drive Current
 - 800 V/s slew rate
 - 80 MHz bandwidth (-3 dB)
 - High Speed

Differential Amps—How Do They Work?



- Behaves Like a High-Speed VF Op Amp:
 - Gain set by ratio of R_F/R_G
 - Signal gain
 - Filtering
 - Level-shifting
 - Buffering/driving
- Differential or Single-Ended Input with Differential Output
 - 2x the dynamic range of op amps

Differential Amps — How Do They Work?



- Internal CM Feedback Forces the $V_{OUT,DM}$ to be Centered Around $V_{OUT,CM}$
 - Create best available balance at high frequencies
 - Improves ADC and line driving
 - The $V_{OUT,CM}$ is set with a V_{OCM} pin
- Gain Set by Ratio of R_F/R_G
 - Mismatches between R_F/R_G on each side causes only gain errors
 - Balance is unaffected because of CM feedback

Primary Uses For Differential Amps

- Differential Signal Processing
 - Avoid ground noise
 - High dynamic range on low supplies
- High-Speed ADC Driving
- Twisted-Pair Line Driving/Receiving
 - Simplifies circuit design
 - Balanced outputs minimize EMI
 - High CMRR reduces EMI susceptibility
- Can Be Used For:
 - SE → DIFF
 - Diff → DIFF
 - Diff → SE

Benefits Of Differential Signal Processing

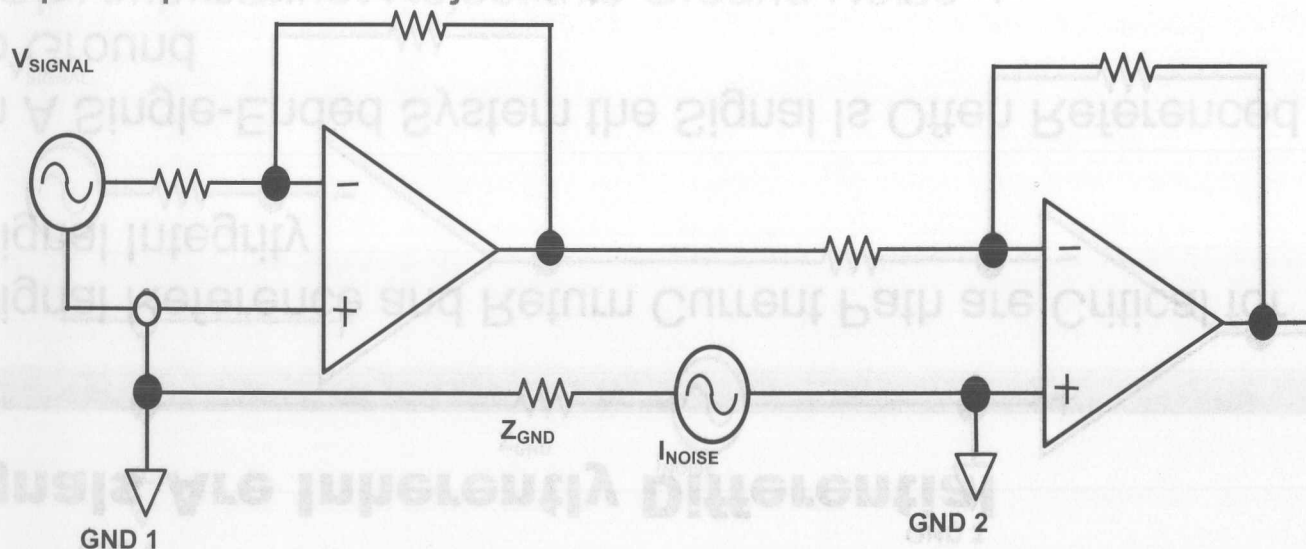
- The Benefits Become Apparent When Trying to Attain the Most Speed and/or Resolution from a Design
 - Avoid grounding/return noise problems
 - Better distortion/dynamic range
 - For the same amplitude differential signal the outputs do not swing as close to the rail
 - Lower distortion, especially the seconds
- Analog signals in high-performance systems start and end differential
 - Almost always the signal source from the real world is differential
 - Many high-speed ADCs have differential inputs

Signals Are Inherently Differential

- Signal Reference and Return Current Path are Critical for Signal Integrity
- In A Single-Ended System the Signal Is Often Referenced to Ground
 - Ground is the return path for numerous signals
 - Ground planes and runs have high-frequency impedance that convert the return current from one signal to a noise source for other signals
 - Grounding is often a source of considerable frustration for designers in single-ended systems

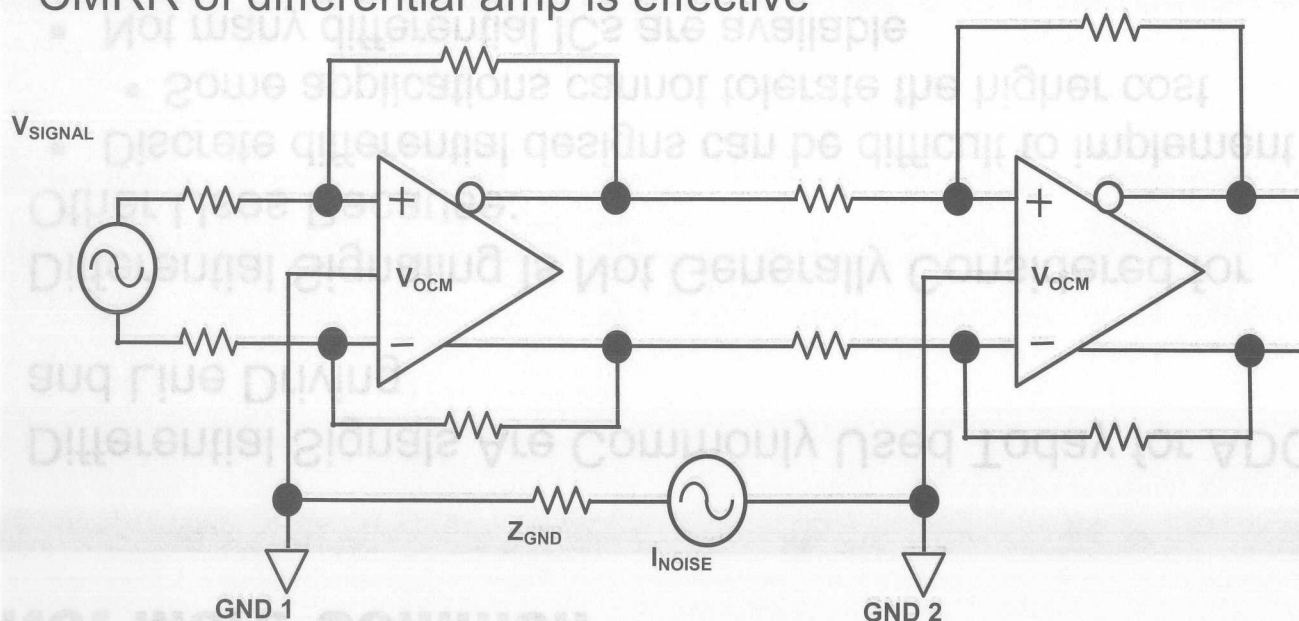
Single-Ended Components Cannot Reject Ground Noise

- Each Part Of the Circuit Has a Different Reference Point
- No Matter How Careful You Are with Grounding, High-Frequency Ground Currents Will Cause Some Problems That May Be Difficult to Work Around
- Op Amp Cannot Reject this Ground Noise



Differential Amps Have Effective CMRR

- Differential Signal Does Not Need a Reference
- Ground and Other Noise Sources Are Common to Both Inputs
 - CMRR of differential amp is effective



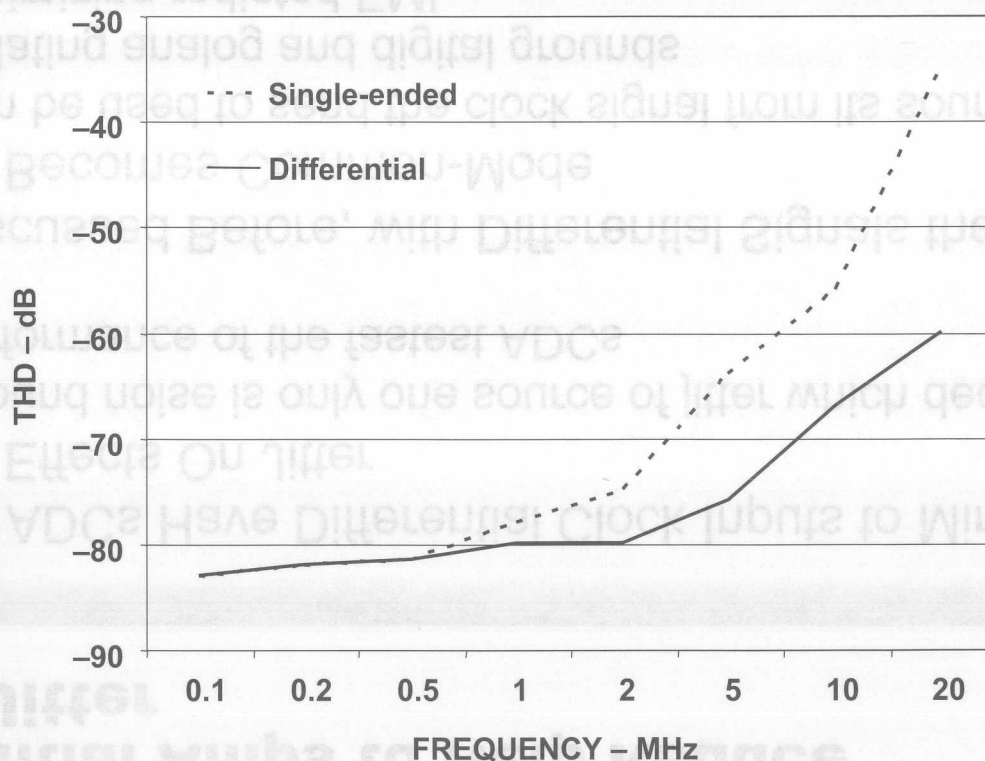
Why Differential Signal Processing Is Not More Common

- Differential Signals Are Commonly Used Today for ADC and Line Driving
- Differential Signaling Is Not Generally Considered for Other Uses Because:
 - Discrete differential designs can be difficult to implement
 - Some applications cannot tolerate the higher cost
 - Not many differential ICs are available
 - Transformers must be used
- As Speeds and Resolution Increase, the Benefits of Differential Signaling Become More Necessary

ADCs Perform Better When Driven Differentially

- Especially As Frequency Increases

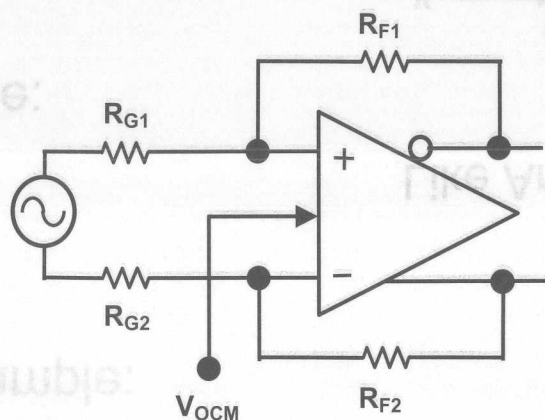
AD9240 (–6 dBFS, 5 V SPAN)



Differential Amps to Help Reduce Clock Jitter

- Some ADCs Have Differential Clock Inputs to Minimize Ground Noise Effects On Jitter
 - Ground noise is only one source of jitter which decreases the performance of the fastest ADCs
- As Discussed Before, with Differential Signals the Ground Noise Becomes Common-Mode
 - Can be used to send the clock signal from its source into the ADC
 - Isolating analog and digital grounds
 - Minimizing radiated EMI

General Single-Ended to Differential Circuit



Generalized Four-Resistor Single-Ended into Diff-Out Equation

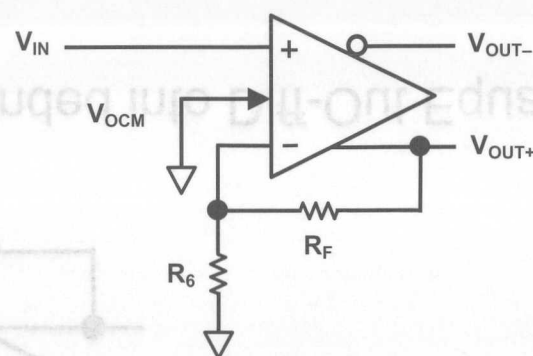
$$G = \frac{2 \times (1 - \beta_1)}{(\beta_1 + \beta_2)}$$

$$\beta_1 = \frac{R_{G1}}{(R_{F1} + R_{G1})} \quad \beta_2 = \frac{R_{G2}}{(R_{F2} + R_{G2})}$$

Understanding How They Work with Alternate Circuit Configurations

- Two Feedback Loops
 - Differential feedback forces Inputs to the same voltage
 - Common-mode feedback forces $V_{OUT-} = -V_{OUT+}$

Like A Noninverting Op Amp



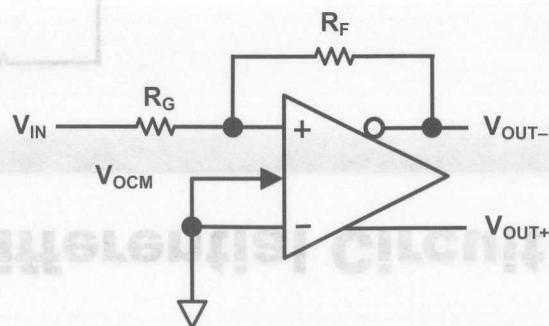
- Noninverting Example:

- For $R_F = 0$
 - $V_{OUT+} = V_{IN}$
 - Gain = 2

Like An Inverting Op Amp

- Inverting Example:

- For $R_F = R_G$
- High input Z summing node
 - $V_{OUT-} = -V_{IN}$
 - Gain = 2



More About the V_{OCM} Pin

- V_{OCM} Pin Separates Our Diff Amps from Other Diff Amp Configurations
 - Creates best available balance at high frequencies
 - Can be used with AC signal for modulation as well as DC reference voltages
- Easy Level-Shift
 - From ground referenced signals (± 5 V supplies) to single 5 V supply signals for ADCs
 - Better distortion in signal chain for ± 5 V, than +5 V
 - Connect to the ADC reference or any other reference voltage

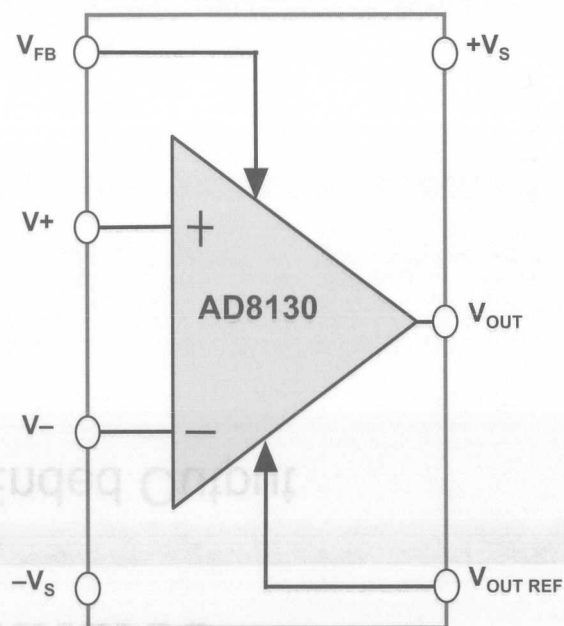
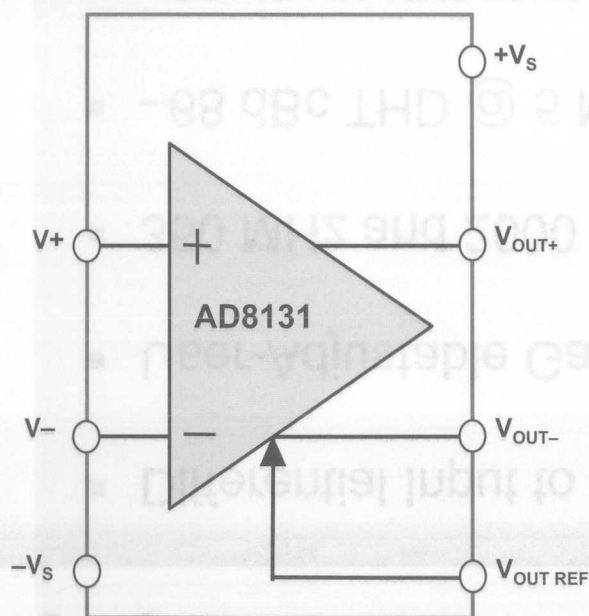
The New High-Speed Differential Amp Family

ADI MULTIPURPOSE DIFFERENTIAL AMP FAMILY

Part #	AD8131	AD8138	AD8132	AD8129	AD8130	AD830
	Differential-to-Differential			Differential-to-Single-Ended		
Features	Fixed Gain = 2x	Adjustable Gain/Feedback		10x Stable	1x Stable	1x Stable
Position	Line Driver	Highest Perf. ADC Driver	Low Cost Gen. Purp.	New Receiver		Old Receiver
Release Status	Released	Released	Released	Released		Released
Sample Status	Released	Released	Released	Released		Released
100 Price	\$2.12	\$4.25	\$1.95	\$1.83		\$3.14

AD8130/31 Low Cost Differential Driver and Receiver

The AD8130 and AD8131 are designed for analog and digital video signal distribution over twisted pair—(NTSC to SMPTE259)



AD8130 Differential Receiver

Key Specifications and Features

- Differential Input to Single-Ended Output
- User-Adjustable Gain
- 350 MHz and 2000 V/ μ s
- -68 dBc THD @ 5 MHz
- -80 dB CMRR @ 10 MHz
- 4 V to 12 V Supply Range
- 7.5 mA Supply Current

AD8131 Differential Driver

Key Specifications and Features

- Differential or Single-Ended-to-Differential Output
- Fixed Gain-of-Two
- Separate Input Sets Common-Mode Range
- Internal Common-Mode Feedback to Improve Gain and Phase Response
- 300 MHz Bandwidth, 1500 V/ μ s Slew Rate
- -80 dBc THD @ 5 MHz
- 3.7 V to 5 V Supply Range
- 11 mA Quiescent Current

What's Inside the AD8131/AD8132/AD8138 Differential Amps?

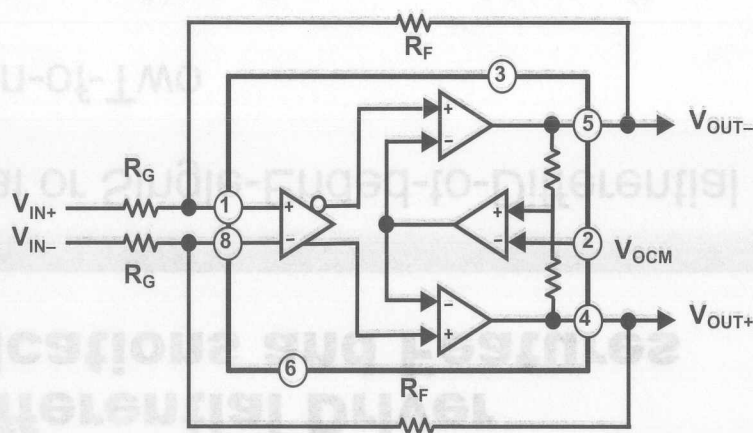
Internal CM Feedback forces both outputs to be balanced,
Equal in amplitude 180° out of phase:

$$V_{OUT, CM} = (V_{OUT+} + V_{OUT-})/2$$

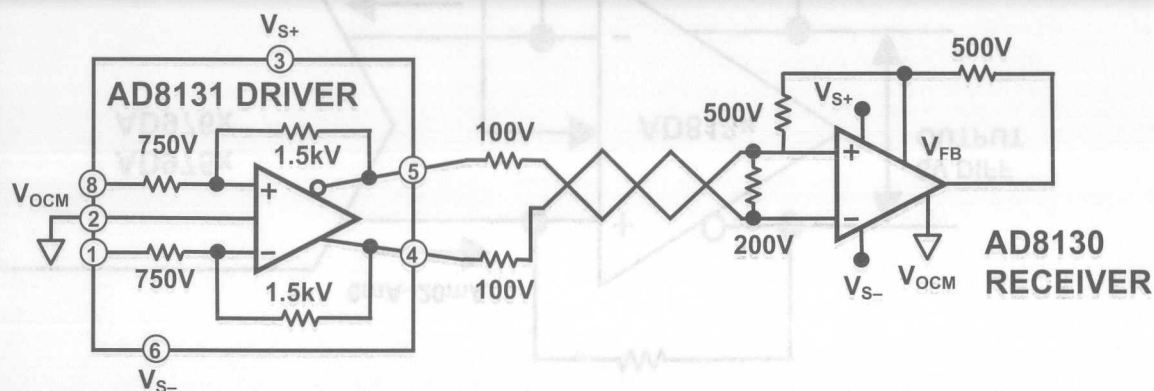
Balance is unaffected by R_F/R_G matching.

Differential feedback effectively creates two summing nodes.
Forces both inputs to the same voltage when the loop is closed.

High Input Z, Low Output Z



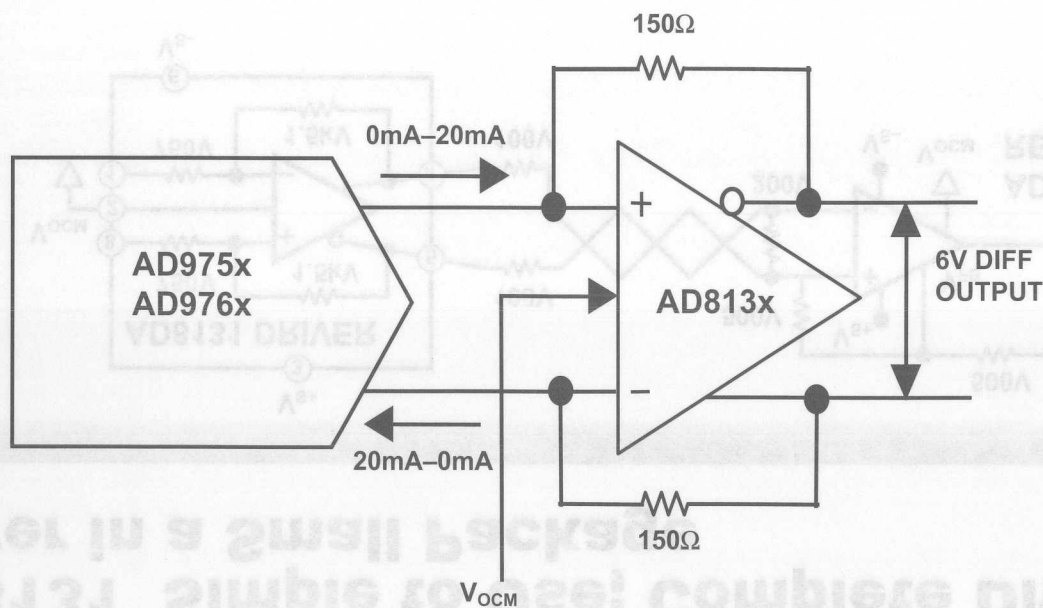
AD8131 Simple to Use; Complete Differential Driver in a Small Package



- Target Applications
 - Video signal distribution
 - KVM
 - High-speed instrumentation
- Competition
 - Two op amp line drivers
 - About the same price, cannot achieve the same balance, and uses considerable board space

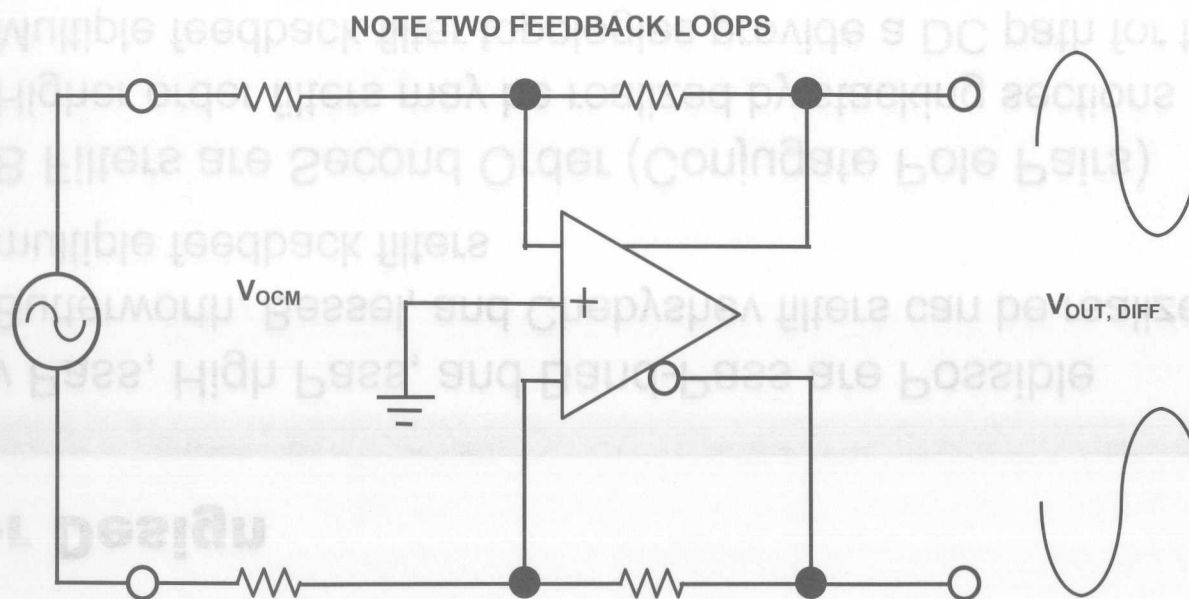
Buffered Differential Output for 12-/16-Bit High-Speed DACs

“Virtual GND” reduces effect of DAC’s nonlinear output impedance to achieve larger output power without having a large compliance voltage on the DAC output. When level-shifting is needed, use V_{OCM} .



Using the Differential Amps In Active Filters

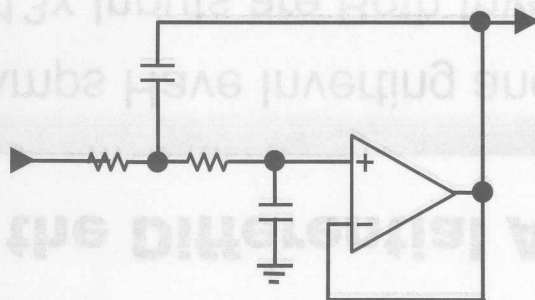
- Op Amps Have Inverting and Noninverting Inputs Available
- AD813x Inputs are Both Inverting
 - Filter topologies must be inverting types



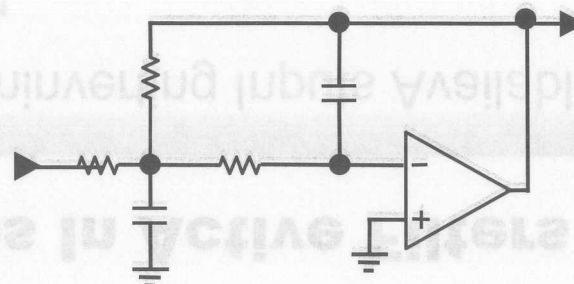
Filter Design

- Low Pass, High Pass, and Band-Pass are Possible
 - Butterworth, Bessel, and Chebyshev filters can be realized in multiple feedback filters
- MFB Filters are Second Order (Conjugate Pole Pairs)
 - Higher order filters may be realized by stacking sections
 - Multiple feedback filter topologies provide a DC path for the input bias current.

NOT ACCEPTABLE
Sallen Key Low Pass

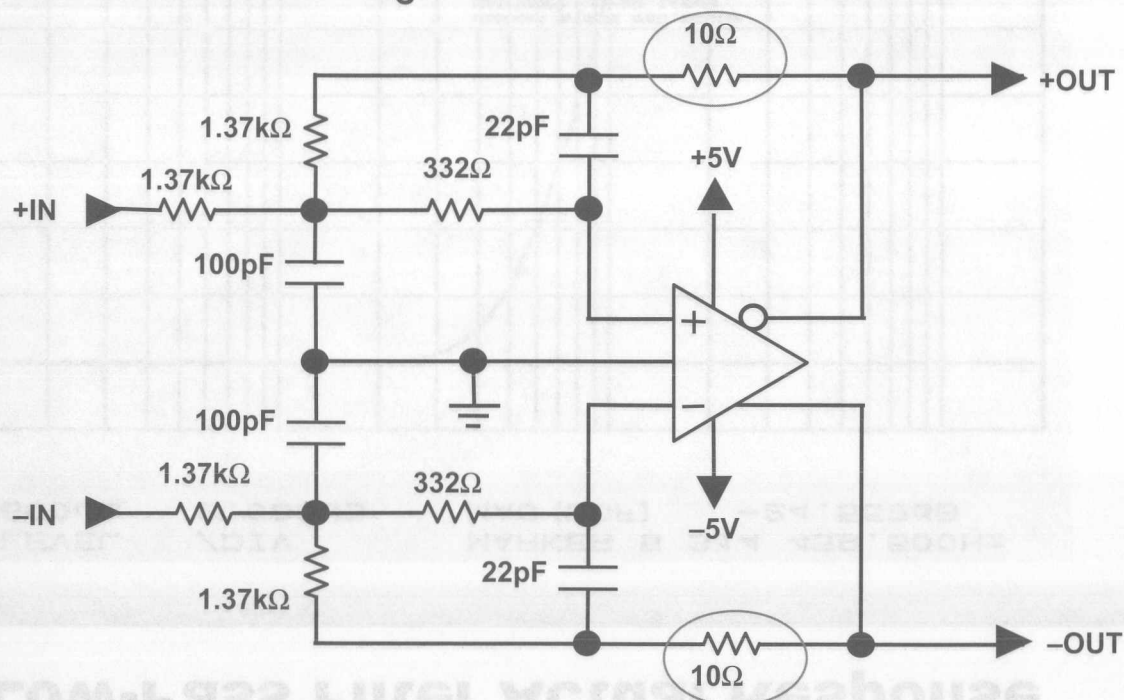


ACCEPTABLE
Multiple Feedback Low Pass

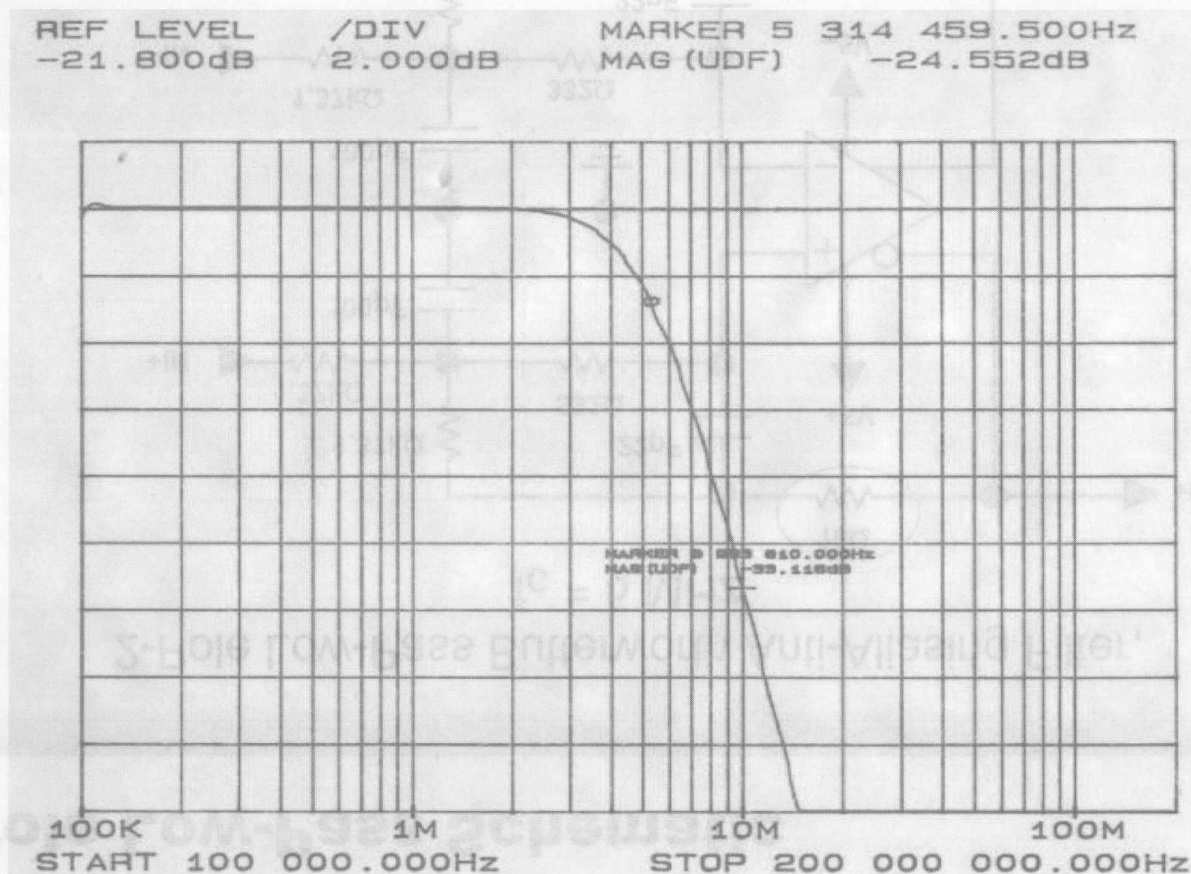


2-Pole Low-Pass Schematic

2-Pole Low-Pass Butterworth Anti-Aliasing Filter,
 $f_c = 5 \text{ MHz}$

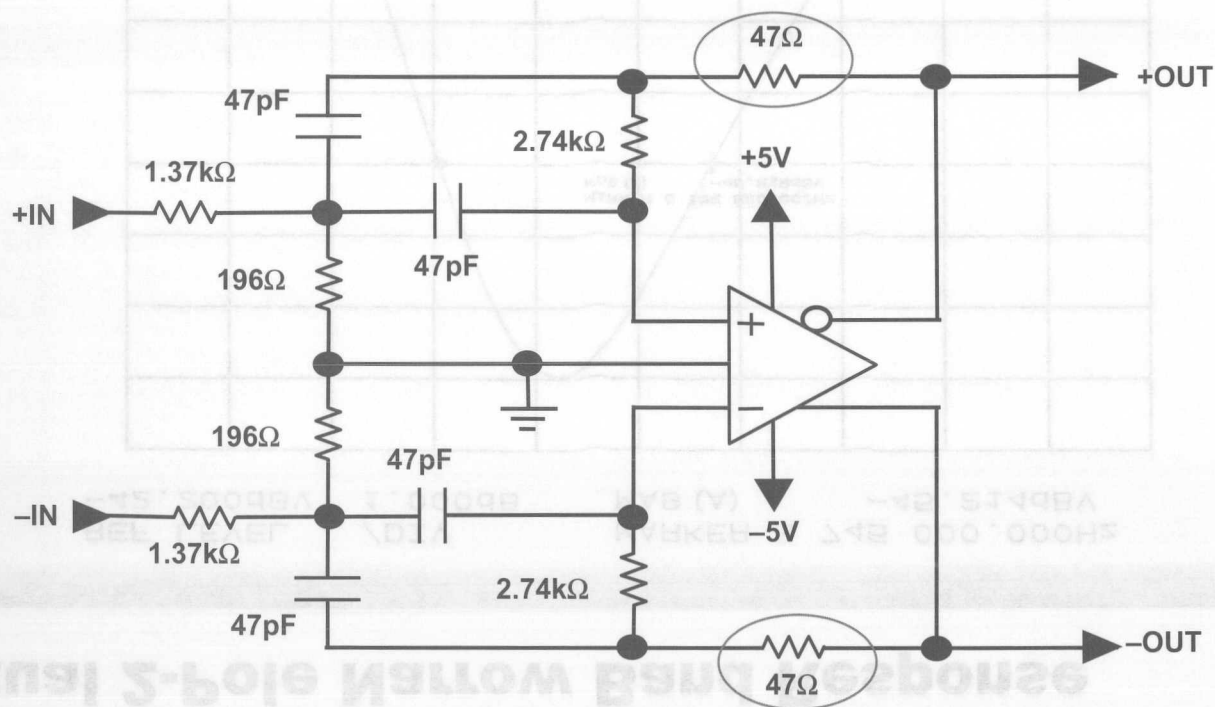


5 MHz Low-Pass Filter Actual Response



Band-Pass Filter Schematic

2-Pole Band-Pass Butterworth Filter,
 $f_c = 5 \text{ MHz}$, $Q = 2$

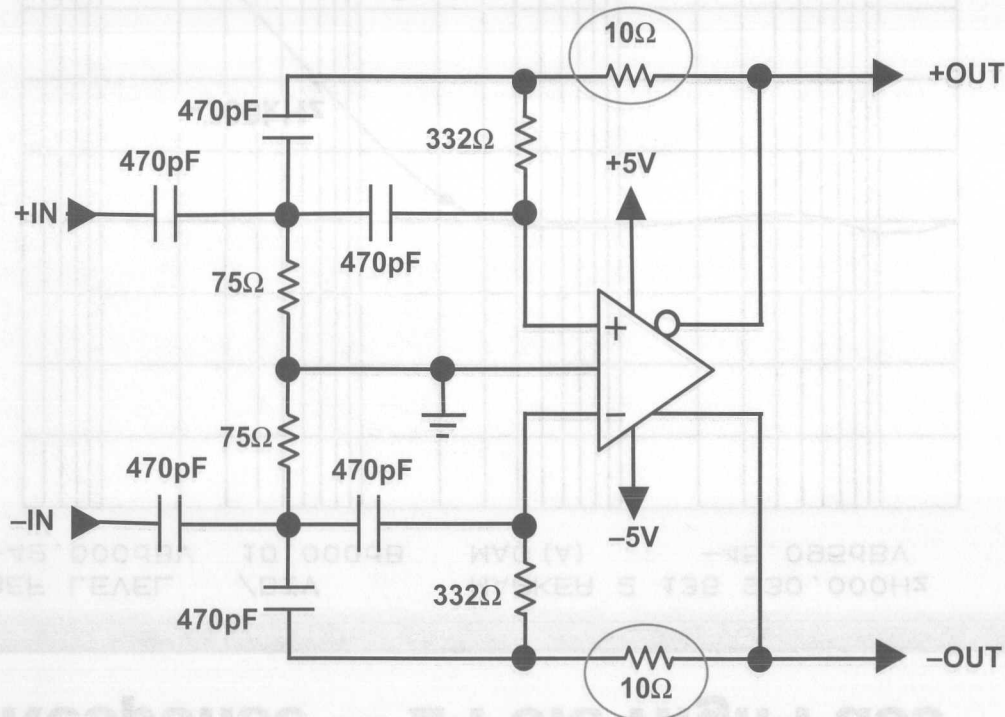


Actual 2-Pole Narrow Band Response

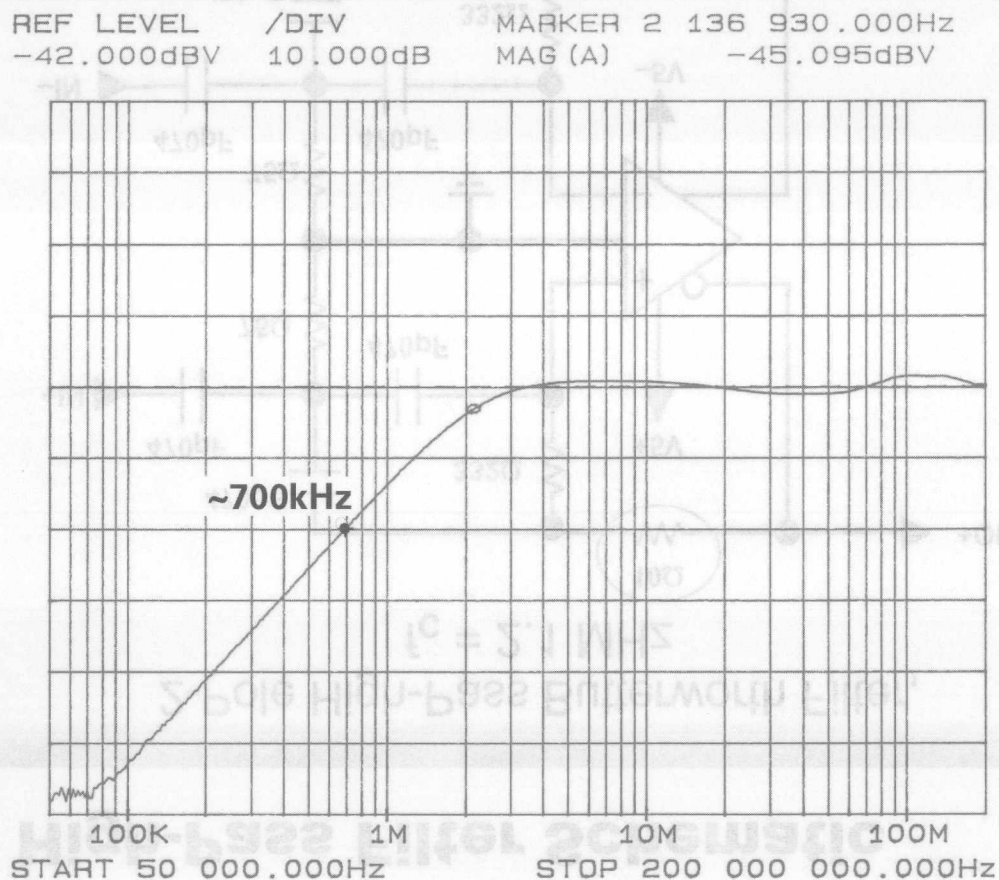


2-Pole High-Pass Filter Schematic

2-Pole High-Pass Butterworth Filter,
 $f_c = 2.1 \text{ MHz}$



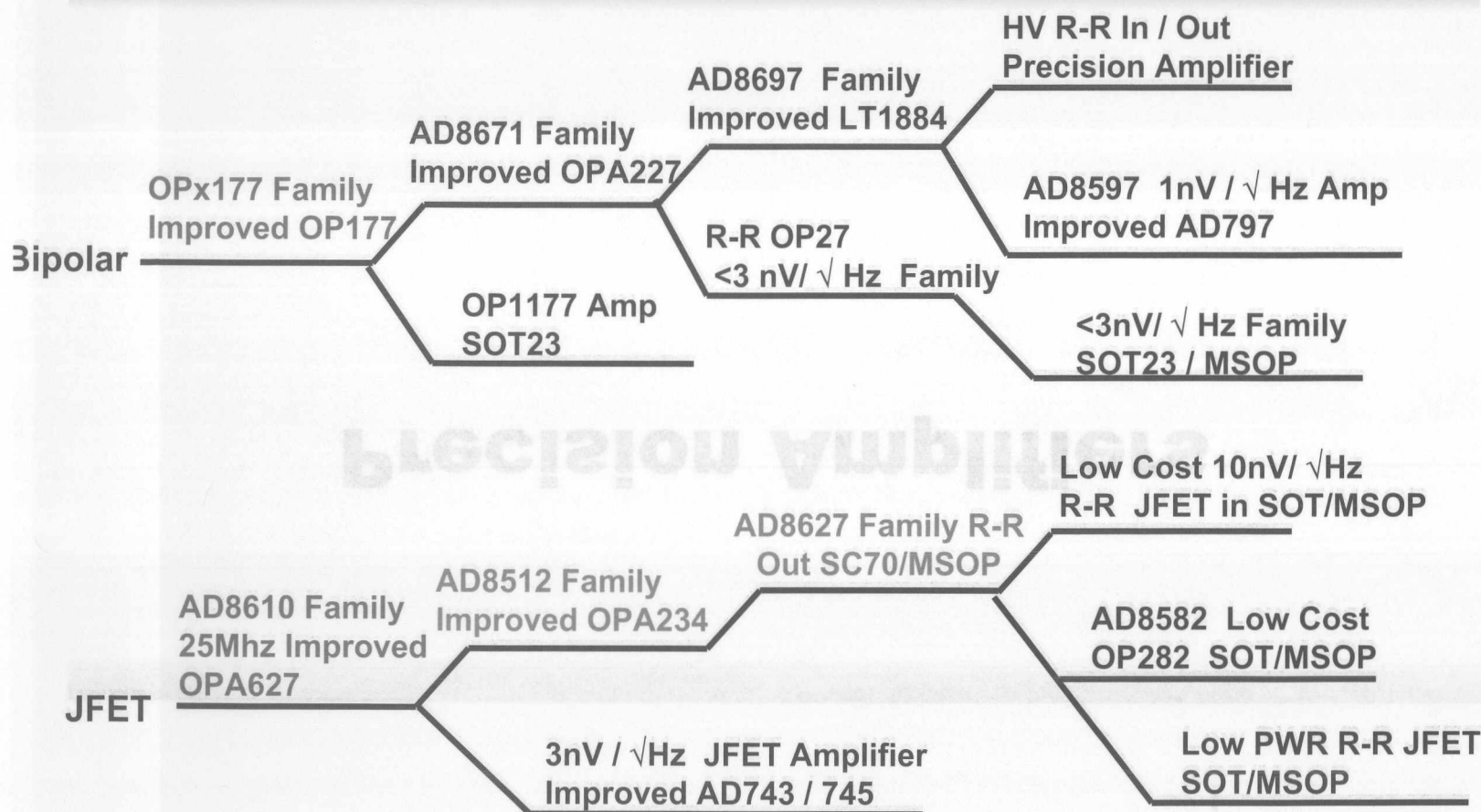
Actual Response — 2-Pole High-Pass





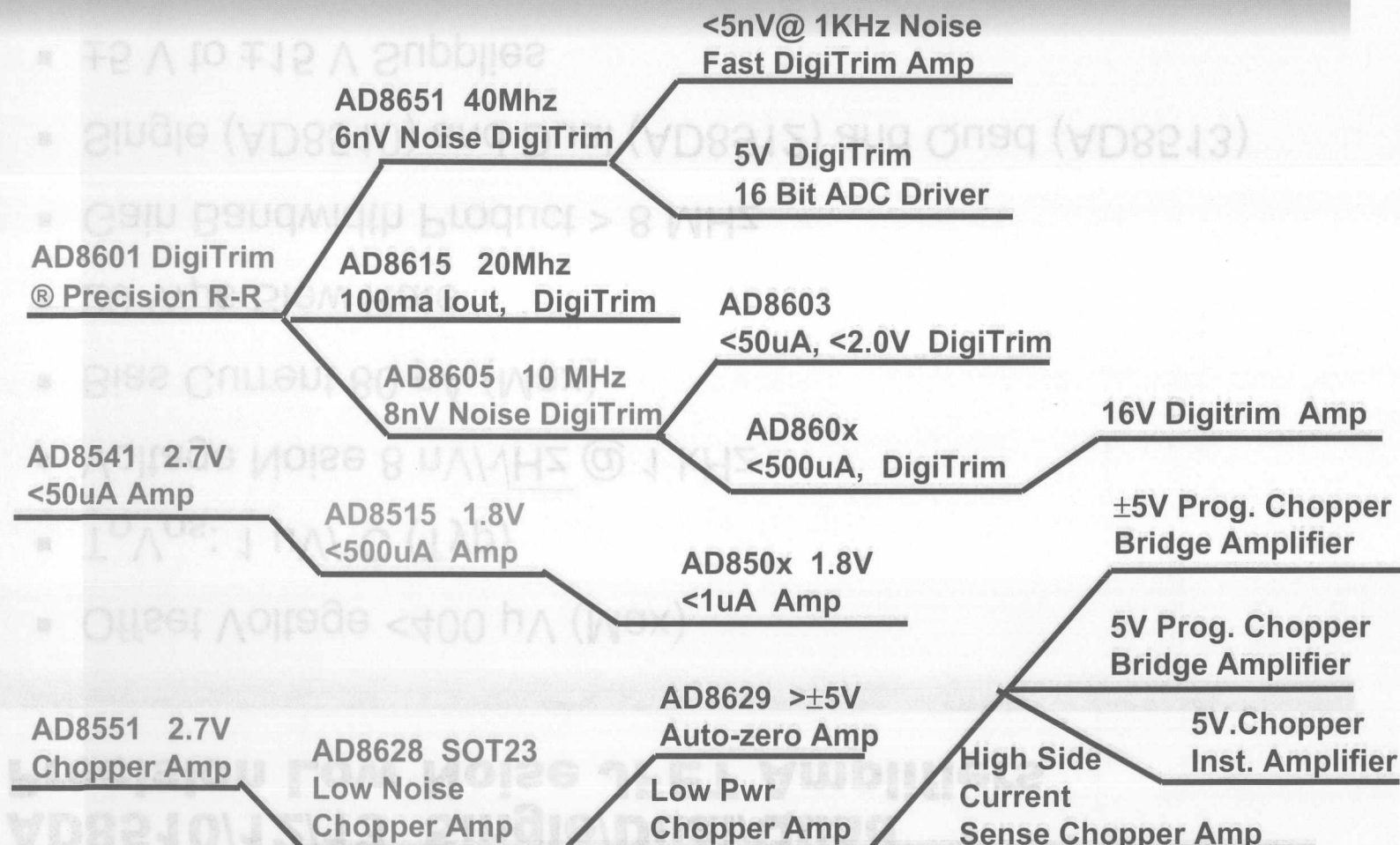
Precision Bipolar Amplifier Roadmap

Improved Performance, Lower Cost in Small Packages



Precision CMOS Amplifier Roadmap

High Performance, Low Cost in Small Packages



AD8510/12/13 Single/Dual/Quad Precision Low Noise JFET Amplifiers

- Offset Voltage $<400 \mu\text{V}$ (Max)
- $T_O V_{OS}$: $1 \mu\text{V}/^\circ\text{C}$ (Typ)
- Voltage Noise $8 \text{ nV}/\sqrt{\text{Hz}}$ @ 1 kHz
- Bias Current 80 pA (Max)
- $20 \text{ V}/\mu\text{s}$ Slew Rate
- Gain Bandwidth Product $> 8 \text{ MHz}$
- Single (AD8510) and Dual (AD8512) and Quad (AD8513)
- $\pm 5 \text{ V}$ to $\pm 15 \text{ V}$ Supplies
- MSOP or SOIC (Single/Dual) TSSOP (Quad)

AD8625/26/27 Single/Dual/Quad Precision, Low Power, Single Supply JFET Amplifiers

- Single-Supply Operation: 5 V to 26 V
- Dual Supply Operation: ± 2.5 V to ± 13 V
- Very low I_B : 1 pA (max)
- Rail-to-Rail Output
- Low Supply Current: 750 μ A/Amp
- Low Offset Voltage: 500 μ V Max @ $V_s = 5$ V
- 5 MHz Bandwidth
- Unity Gain Stable
- No Phase Reversal
- Outputs Stable with Capacitive Loads over 500 pF
- Small Packages: Single SC-70 and SOIC-8
Dual MSOP-8
Quad TSSOP-14

AD8610/20 Single/Dual Fast, Low Noise, Ultraprecision JFET Amplifier

- Voltage Noise 6 nV/√Hz
- Current Noise 2.5 fA/√Hz
- Offset Voltage 250 μV (Max) [100 μV (Max) B Grade]
- $T_c V_{os}$: 3.5 μV/°C [1 μV/°C (B Grade)]
- Bias Current 10 pA (Max)
- Open-Loop Gain 100 dB (Min)
- 50 V/μs Slew Rate (Min)
- 25 MHz Bandwidth
- ±5 V to ±13 V Supplies

AD8697/98/99 Single/Dual/Quad Very Low Input Bias Current, Low Noise, High Precision, Rail-to-Rail Output, Op Amps

- 600 μ A Max Supply Current
- 50 μ V Max Offset Voltage
- 0.6 μ V/ $^{\circ}$ C Max Offset Voltage Drift
- 100 pA Max Input Bias Current
- 14 nV/ $\sqrt{\text{Hz}}$ Noise
- 114 dB Min Common Mode Rejection
- Wide Operating Temperature: -40 $^{\circ}$ C to +125 $^{\circ}$ C
- No Phase Reversal
- Fits Industry Standard Precision Op Amp Sockets
- Packages: AD8697 & AD8698 SOIC & μ SOIC,
AD8699 SOIC & TSSOP

AD8565/66/67 Single/Dual/Quad High Current Output Amplifiers

- Rail-to-Rail Input and Output
 - Input Capability Beyond the Rails
- Output Current 35 mA Continuous — 200 mA Short Circuit
- Stable with Capacitive Loads (1 μ F)
- 4.5 V to 16 V Supply 700 μ A/Amplifier
- Offset Voltage 10 mV (Max)
- 6 V/ μ s Slew Rate
- Small Package
 - AD8565 (single) — SC-70
 - AD8566 (dual) — MSOP
 - AD8567 (quad) — TSSOP and LFCSP

AD8568/69/70 Dual/Quad/Octal High Current Output Buffer Amplifiers

- Rail-to-Rail Input and Output
 - Input capability beyond the rails
- Output Current 35 mA Continuous — 200 mA Short Circuit
- Stable with Capacitive Loads (1 μ F)
- 4.5 V to 16 V Supply 700 μ A/Amplifier
- Offset Voltage 10 mV (Max)
- 6 V/ μ s Slew Rate
- Small Package
 - AD8568 (dual) — SOT-23-6
 - AD8569 (quad) — MSOP-10
 - AD8570 (octal) — LFCSP-32

OP1177/2177/4177 Single/Dual/Quad Precision Dual Supply Bipolar Amplifiers

- 60 μ V Max Offset Voltage
- 2 nA Max Bias Current
- 8 nV/ $\sqrt{\text{Hz}}$ Noise
- 1.3 MHz Bandwidth
- Input/Output Voltages within 1/1.5 V of the Supplies
- Supply Range ± 2.5 V to ± 15 V
- Low Power — 600 μ A
- Small Packages
 - MSOP single (OP1177)/dual (OP2177)
 - TSSOP-14 quad (OP4177)

AD8671/72/74 Single/Dual/Quad Low Noise Precision Dual Supply Bipolar Amplifiers

- 75 μ V Max Offset Voltage
- 10 nA Max Bias Current
- $<3 \text{ nV}/\sqrt{\text{Hz}}$ Noise
- 10 MHz Bandwidth, 4 V/ μ s Slew Rate
- High Gain: 120 dB min
- Supply Range $\pm 5 \text{ V}$ to $\pm 15 \text{ V}$
- Small Packages
 - MSOP single
 - 8/14 lead narrow SOIC dual and quad

AD8515/25 Single/Dual 1.8V Low Power CMOS Rail-to-Rail Input/Output Op Amps

- Single-Supply Operation: 1.8 to 5 Volts
- Offset Voltage: 4 mV max
- SOIC, SOT-23 and μ SOP Packaging
- Slew Rate: 2.7 V/ μ s
- Bandwidth: 5 MHz
- Rail to Rail Input and Output Swing
- Low Input Bias Current: 5 pA max
- Low Supply Current: 450 μ A/Amp max.

The AD860x Family of DigiTrim Amplifiers

- Low Cost and Precision In SOT-23 and MSOP Packages
- Trimming Is Done after the Device Is Packaged!
 - A digital code is entered into the device to adjust the offset voltage
- This Means Lower Cost Because:
 - No lasers or extra capital equipment required
 - Wafer testing not required—only final test
 - Low-cost CMOS process is used
 - As process size shrinks, trim area becomes smaller

AD8605/06/08 Single/Dual/Quad Low Noise Precision CMOS DigiTrim Amplifier

- Second-Generation DigiTrim Amplifier
 - (V_{os} : 65 μ V Max)
- First ADI Low Noise CMOS Amplifier
 - (8 nV/ $\sqrt{\text{Hz}}$ @ 1 kHz)
- 1 pA Bias Current (Max)
- Rail-to-Rail Input and Output
- No Phase Reversal
- Unity Gain Stable
- 10 MHz Bandwidth
- 5 V/ μ s Slew Rate
- 2.7 V to 6 V Supply
- SOT-23 and WLCSP Package (AD8605)
- μ SOIC and SOIC Package (AD8606)
- TSSOP and SOIC Package (AD8608)

AD8603/07/09 Single/Dual/Quad Precision Micropower Low Noise CMOS Rail-to-Rail Input/Output Op Amps

- Low Offset Voltage: 60 μV max
- Low Input Bias Current: 1 pA max
- Single-Supply Operation: 1.8 V to 5 V
- Low Noise: 28 nV/ $\sqrt{\text{Hz}}$
- Micropower: 50 $\mu\text{A}/\text{Amp}$ max.
- No Phase Reversal
- Unity Gain Stable
- Packages: AD8603 SOT-23,
AD8607 SOIC & μSOIC ,
AD8609 SOIC & TSSOP

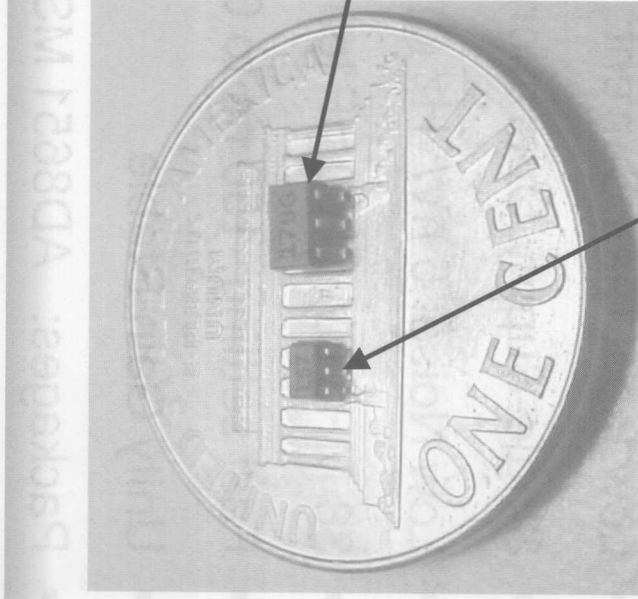
AD8615/16/18 Single/Dual/Quad Precision Fast, Low Noise CMOS Rail-to-Rail Op Amps

- Low Offset Voltage: 60 μ V max
- Low Input Bias Current: 1 pA max
- Single-Supply Operation: 2.7 V to 5 V
- Low Noise: 8 nV/ $\sqrt{\text{Hz}}$
- 20 MHz BW (100 pF load), 12 V/ μ s Slew Rate
- 150 mA output current
- 1.4 mA max I_{sy}
- Packages: AD8615 SOT-23,
AD8616 SOIC & μ SOIC,
AD8618 SOIC & TSSOP

AD8651/52/54 Single/Dual/Quad Very Fast Low Noise Precision CMOS Rail-to-Rail Op Amps

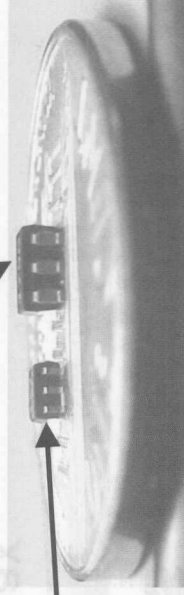
- Low Offset Voltage: 100 μ V max
- Low Input Bias Current: 10 pA max
- Single-Supply Operation: 1.8 V to 5 V
- Low Noise: 5 nV/ $\sqrt{\text{Hz}}$ @ 100 kHz
- 38 MHz BW (100 pF load), 22 V/ μ s Slew Rate
- Fast settling: 150 ns to 0.01%
- Unity Gain Stable
- Packages: AD8651 MSOP8, SOIC8

Size Is All Relative...

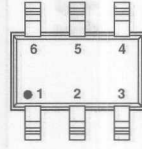


SOT-23

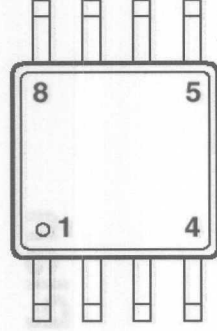
SC-70



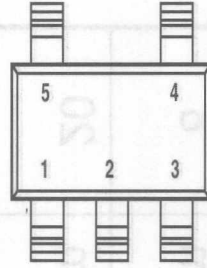
Package Size Relative Comparison



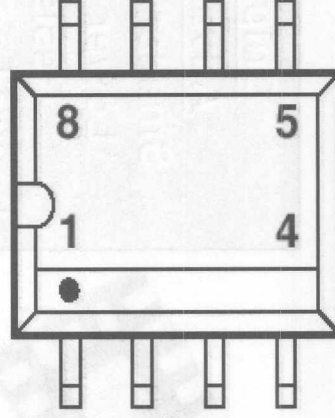
SC-70



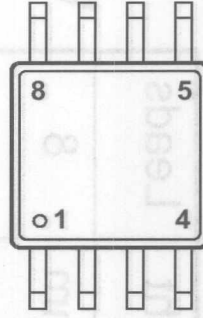
mSOIC



SOT-23



SOIC



MSOP8

0.1 in

DRAWN TO SCALE

New tiny package options: CSP Packages and Bumped Dies

Width	Height	Leads
2X3 mm	0.9 mm	8
3X3 mm	0.9 mm	8
4X4 mm	0.9 mm	20



Chip Scale
Advantages
Smaller Footprint
Lower Thermal
Resistance
Lower Lead Parasitics

New Product Plan

SSM2211	3x3 8L	LFCSP
AD8567	4x4 16L	LFCSP
AD8605	Bumped Die	WLCSP

AD8628 Low Noise Auto-Zero Amplifier

- 2x The Bandwidth At $\frac{1}{2}$ x The Noise
 - 2.2 MHz bandwidth
 - 22 nV/ $\sqrt{\text{Hz}}$ @ 1 kHz noise
 - Lowest Noise of any Auto-Zero Amplifier
- 10 μV Offset (Max over Temperature)
 - -40° C to +125° C
- 20 nV/°C (Max) Drift
- Rail-to-Rail Input and Output
- <100 pA Bias Current
- High Gain, CMRR, and PSRR: 120 dB
- Overload Recovery Time: 0.2 ms
- No External Components Required
- SOT-23 Package

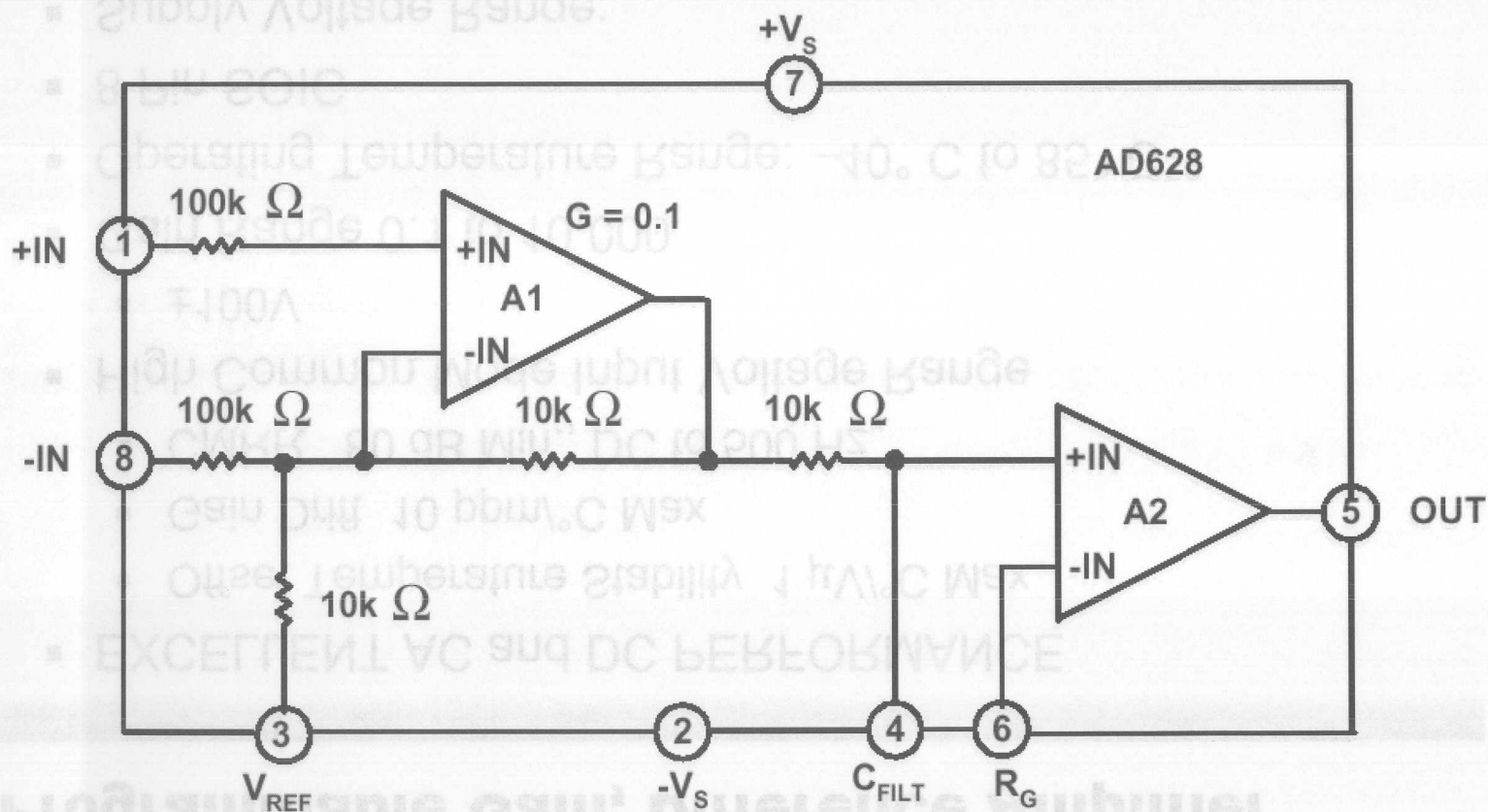
- 201-S3 Package
- No External Components Required
- Overshoot Recovery Time: 0.8 μ s
- High Gain, CMRR, and PSRR: 150 dB
- <100 μ A Bias Current

Instrumentation Amplifiers

- $\pm 10^6$ C to $+125^{\circ}$ C
- 10 μ V Offset (Max over Temperature)
- Lowest Noise of any Auto-Zero Amplifier
- 55 μ V/Hz @ 1 kHz noise
- 5.5 MHz bandwidth
- 5X the Bandwidth At 1% x the Noise

AD8628 Low Noise Auto-Zero Amplifier

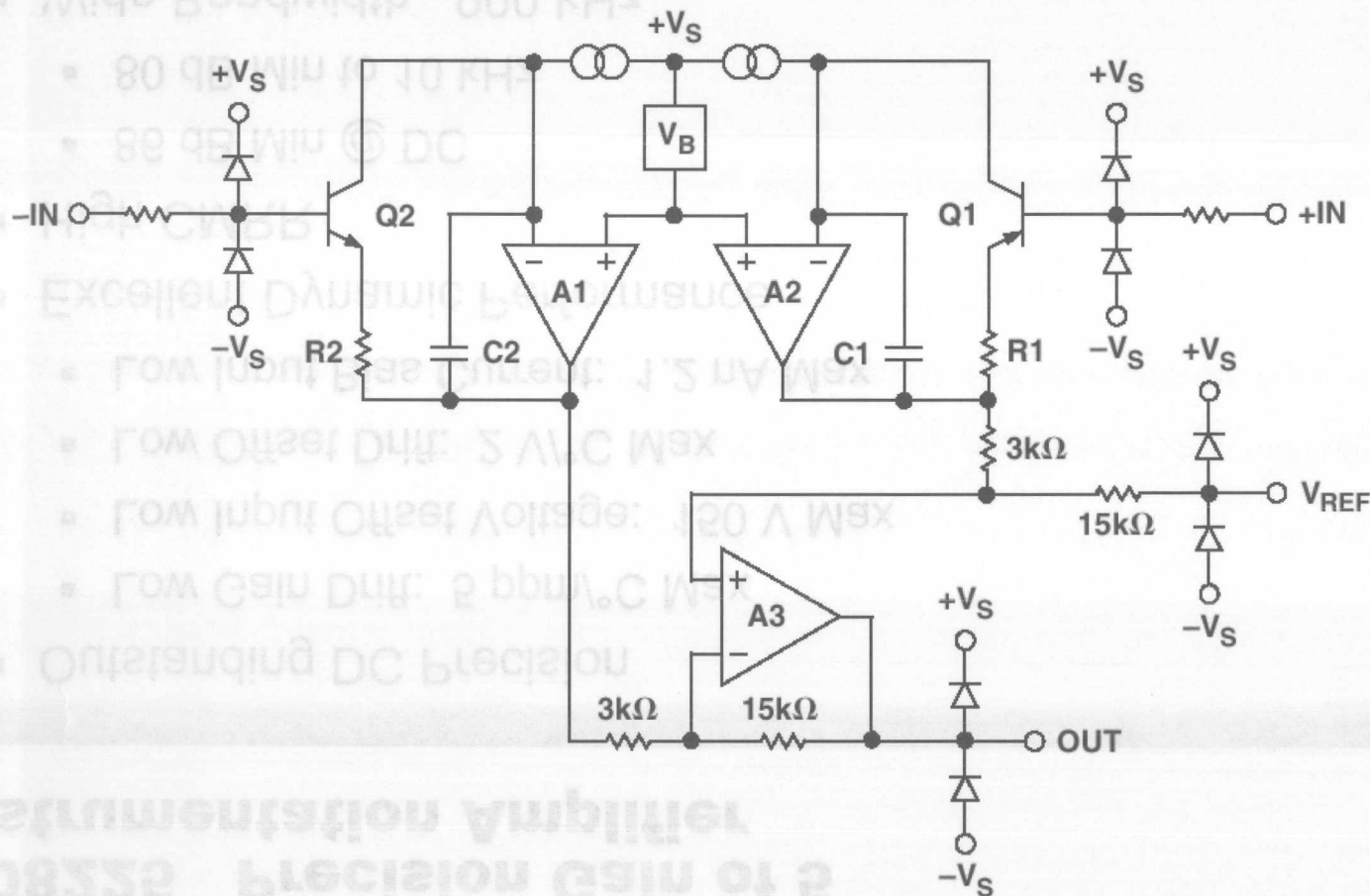
AD628 High Common-Mode Voltage, Programmable Gain, Difference Amplifier



AD628 High Common-Mode Voltage, Programmable Gain, Difference Amplifier

- EXCELLENT AC and DC PERFORMANCE
 - Offset Temperature Stability $1 \mu\text{V}/^\circ\text{C}$ Max
 - Gain Drift $10 \text{ ppm}/^\circ\text{C}$ Max
 - CMRR 80 dB Min., DC to 500 Hz
- High Common Mode Input Voltage Range
 - $\pm 100\text{V}$
- Gain Range 0.1 to $10,000$
- Operating Temperature Range: -40°C to 85°C
- 8 Pin SOIC
- Supply Voltage Range:
 - Dual Supply $\pm 5 \text{ V}$ to $\pm 18 \text{ V}$
 - Single Supply 5 V to 36 V

AD8225 Precision Gain of 5 Instrumentation Amplifier



AD8225 Precision Gain of 5 Instrumentation Amplifier

- Outstanding DC Precision
 - Low Gain Drift: 5 ppm/°C Max
 - Low Input Offset Voltage: 150 V Max
 - Low Offset Drift: 2 V/°C Max
 - Low Input Bias Current: 1.2 nA Max
- Excellent Dynamic Performance
- High CMRR
 - 86 dB Min @ DC
 - 80 dB Min to 10 kHz
- Wide Bandwidth 900 kHz
- High Slew Rate
 - 5 V/μs Min

AD8225 Precision Gain of 5 Instrumentation Amplifier

- No External Components Required
- Highly Stable, Factory Trimmed Gain of 5
- Low Power,
 - 1.2 mA Max Supply Current
- Wide Power Supply Range (1.7 V to 18 V)
 - Single and Dual Supply Operation
- -40° C to + 85° C Operation
- 8 Pin SOIC Package

Comparators

Wide Power Supply Range (1.5 V to 18 V)

1.5 nA Max Supply Current

Low Power

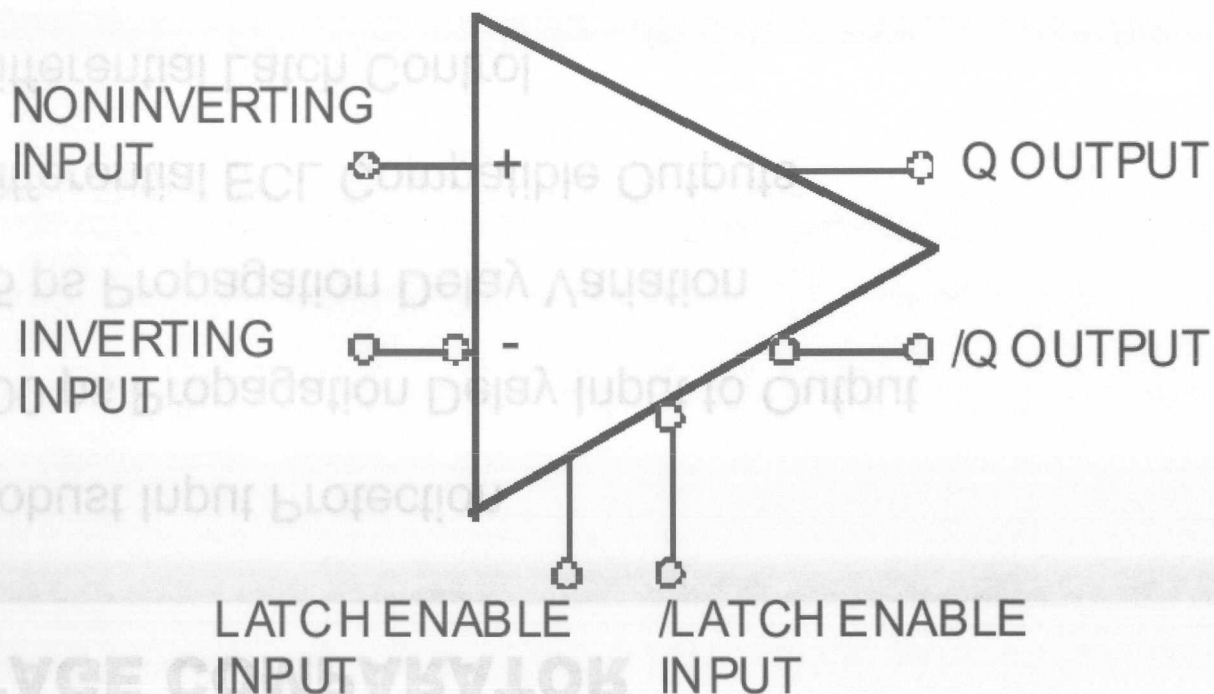
Highly Stable, Factory Trimmed Gain of 2

No External Components Required

AD8552 Precision Amplifier

AD53519 DUAL ULTRAFAST VOLTAGE COMPARATOR

- Typical Offset Voltage of 120 μ V
- Power Supply Rejection Greater than 10 dB
- Differential Gain Control
- Differential ECG Compatible Outputs
- 12 ps Propagation Delay Variation
- 30 ps Propagation Delay Input to Output
- Output Input Protection



AD53519 DUAL ULTRAFAST VOLTAGE COMPARATOR

- Robust Input Protection
- 300 ps Propagation Delay Input to Output
- 75 ps Propagation Delay Variation
- Differential ECL Compatible Outputs
- Differential Latch Control
- Power Supply Rejection Greater than 70 dB
- Typical 3.0 dB Bandwidth > 2.5 GHz
- Typical Output Rise/Fall of 150 ps

SECTION 2

Analog-to-Digital Converters

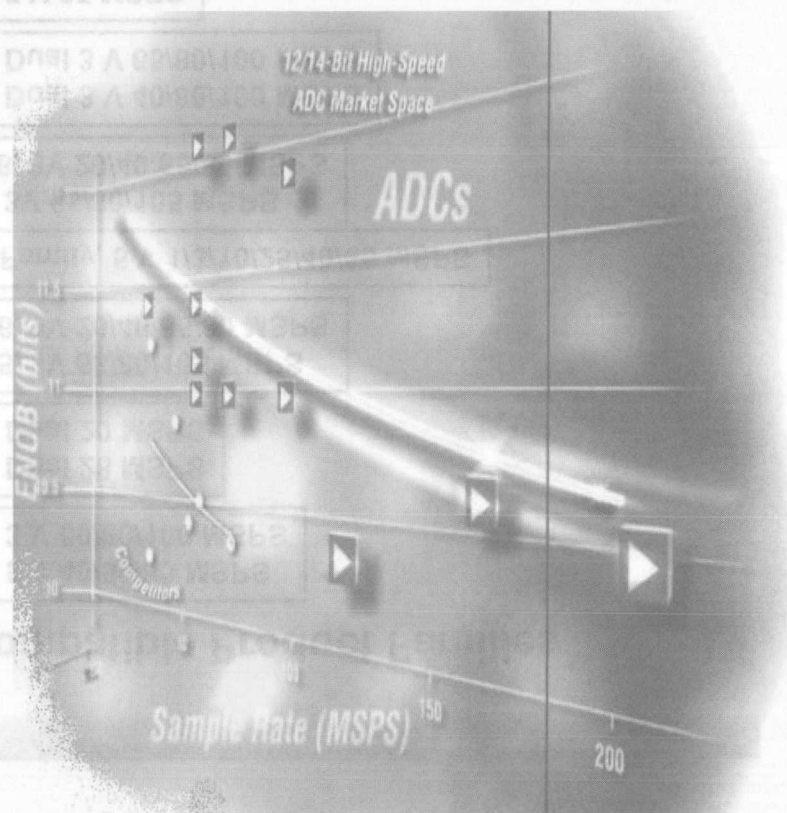
High-Speed ADCs
General-Purpose ADCs
Sigma-Delta ADCs
Special-Purpose ADCs

High-Speed ADCs

SECTION 5

Converter Trends in High Performance Signal Processing Applications

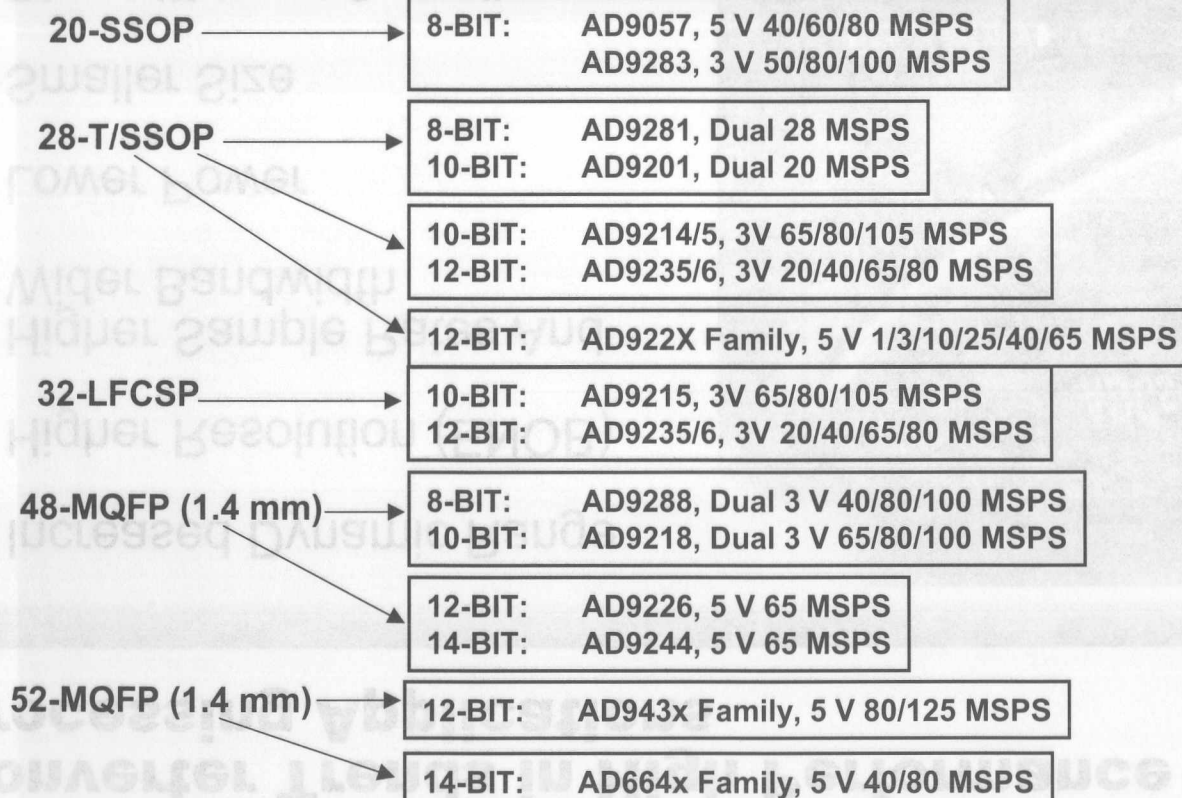
- Increased Dynamic Range
- Higher Resolution (ENOB)
- Higher Sample Rates And Wider Bandwidth
- Lower Power
- Smaller Size
- Direct IF Input Sampling
- Increased Functionality / Flexibility



www.analog.com/fastADCs

ADC Pin Compatibility

ADI Continues to Develop Pin-Compatible Product Families



6-/8-/10-Bit ADC Product Roadmap

10-BIT

AD9051 (60 MSPS)
AD9071 (100 MSPS)
AD9200 (20 MSPS)
AD9203 (40 MSPS)
AD9214 (65/80/105 MSPS)
AD9410 (210 MSPS)
AD9201 (DUAL 20 MSPS)
AD9218 (DUAL 40/65/80/105 MSPS)

8-BIT

AD9054A (135/200 MSPS)
AD9057 (40/60/80 MSPS)
AD9059 (DUAL 60 MSPS)
AD9280 (32 MSPS)
AD9281 (DUAL 28 MSPS)
AD9283 (50/80/100 MSPS)
AD9288 (DUAL 40/80/100 MSPS)
AD9483 (TRIPLE 100/140 MSPS)

6-BIT

AD9066 (DUAL 60 MSPS)

10-BIT

AD9215
3 V, 10-BIT
105 MSPS
120 mW

Multi-
channel
3V 60+MSPS

8-BIT

AD9480
250MSPS
3.3V

3V Cores
400+MSPS

Released

12-/14-/16-Bit ADC Product Roadmap

16-BIT

AD9260 [20 MSPS (8x)]

14-BIT

AD9240 (10 MSPS)

AD9241 (1 MSPS)

AD9243 (3 MSPS)

AD6644 (40/65 MSPS)

AD6645 (80 MSPS)

12-BIT

AD9220 (10 MSPS)

AD9221 (1.5 MSPS)

AD9223 (3 MSPS)

AD9224 (40 MSPS)

AD9225 (25 MSPS)

AD9226 (65 MSPS)

AD9235 (20/40/65 MSPS)

AD9430 (170 MSPS)

AD9432 (80/105 MSPS)

AD9433 (105/125 MSPS)

AD9042 (41 MSPS)

AD6640 (65 MSPS)

16-BIT

14-BIT

AD6645

14-BIT, 5 V

105 MSPS

AD9244

14-BIT, CMOS

40/65 MSPS

Low Power
80MSPS

12-BIT

AD9430

12-BIT, 3 V

210 MSPS

3.3V Ultra

Low Power

20/40/60

AD9238

12-BIT, Dual

20/40/65 MSPS

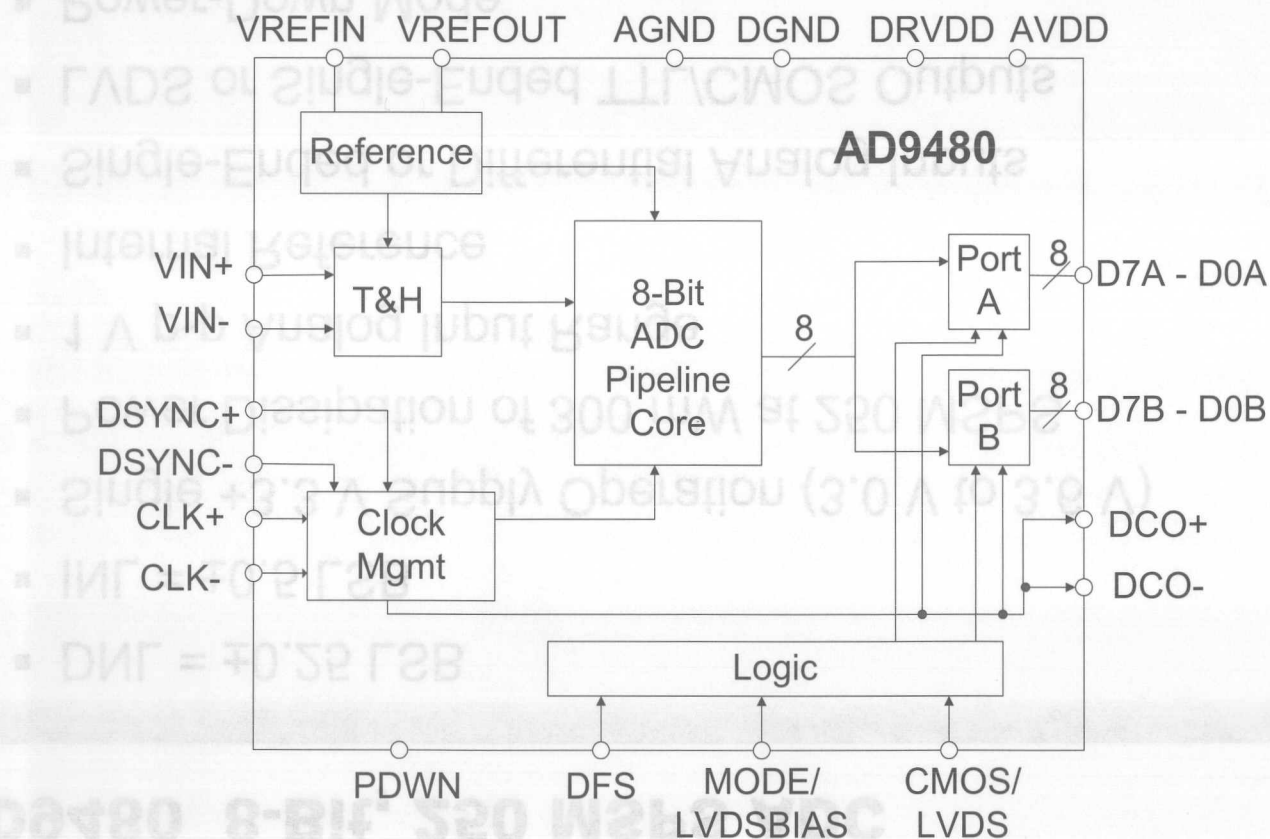
AD9236

12-BIT, 3.3 V

80 MSPS

Released

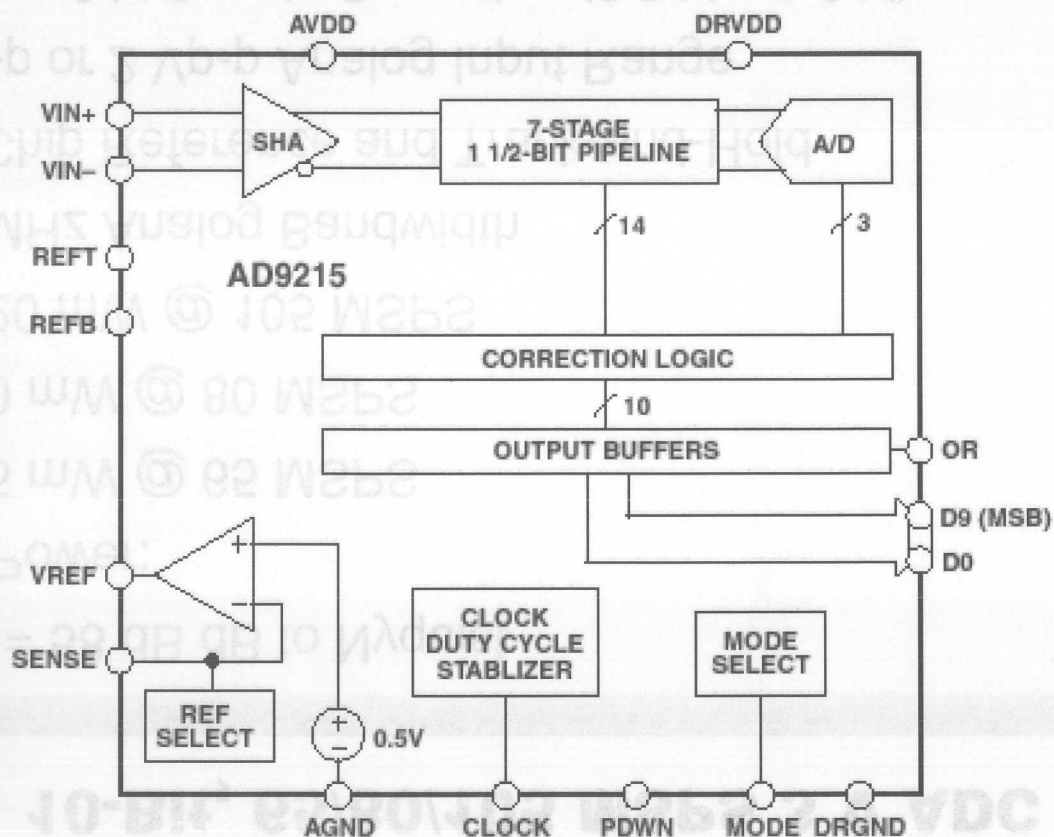
AD9480 8-Bit, 250 MSPS ADC



AD9480 8-Bit, 250 MSPS ADC

- DNL = ± 0.25 LSB
- INL = ± 0.5 LSB
- Single +3.3 V Supply Operation (3.0 V to 3.6 V)
- Power Dissipation of 300 mW at 250 MSPS
- 1 V p-p Analog Input Range
- Internal Reference
- Single-Ended or Differential Analog Inputs
- LVDS or Single-Ended TTL/CMOS Outputs
- Power-Down Mode
- Clock Duty Cycle Stabilizer
- Pin-Similar to AD9054A

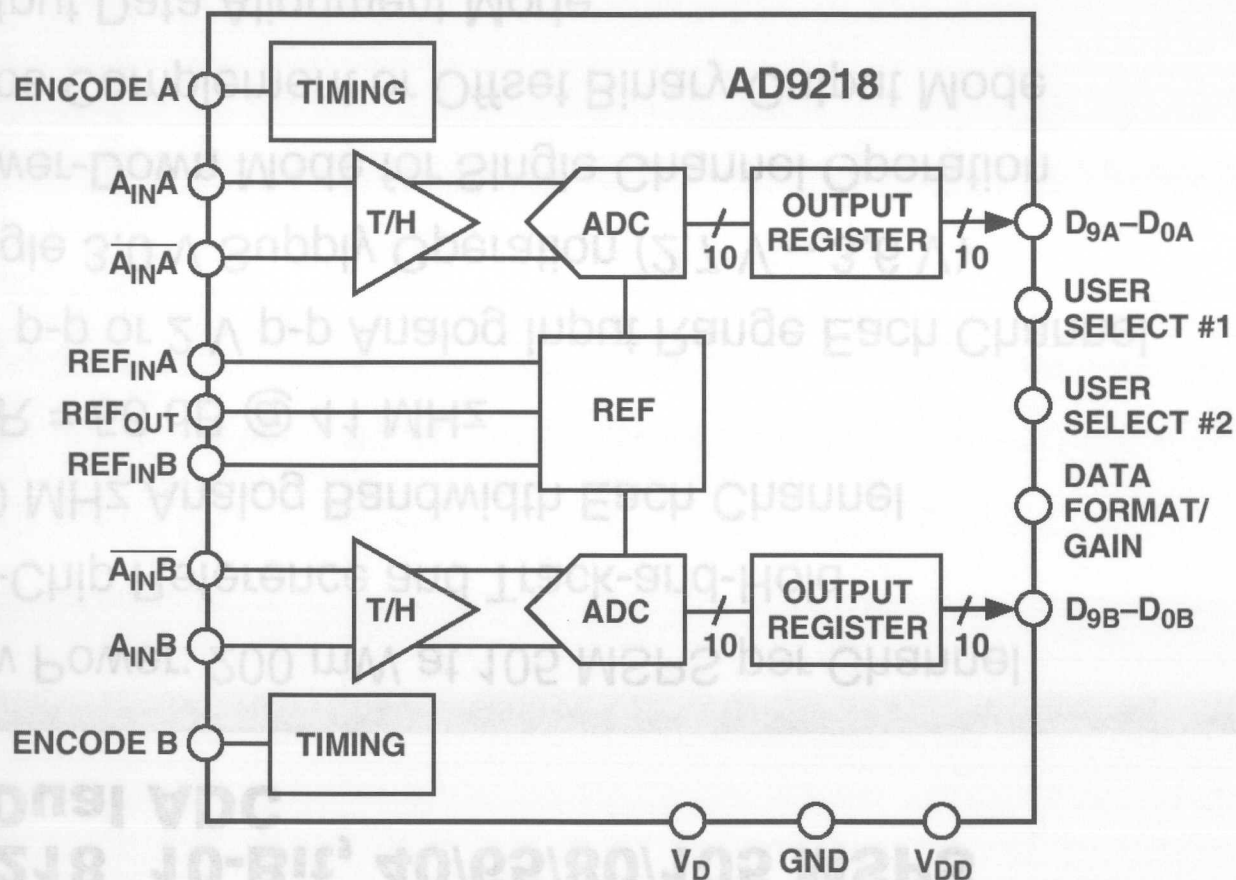
AD9215 10-Bit, 65/80/105 MSPS, 3 V ADC



AD9215 10-Bit, 65/80/105 MSPS 3 V ADC

- SNR = 58 dB dB to Nyquist
- Low Power:
 - 75 mW @ 65 MSPS
 - 90 mW @ 80 MSPS
 - 120 mW @ 105 MSPS
- 400 MHz Analog Bandwidth
- On-Chip Reference and Track-and-Hold
- 1 Vp-p or 2 Vp-p Analog Input Range
- Single +3 V Supply Operation (2.7 V – 3.6 V)
- Twos Complement or Offset Binary Data Format
- Power-Down Mode = 1 mW

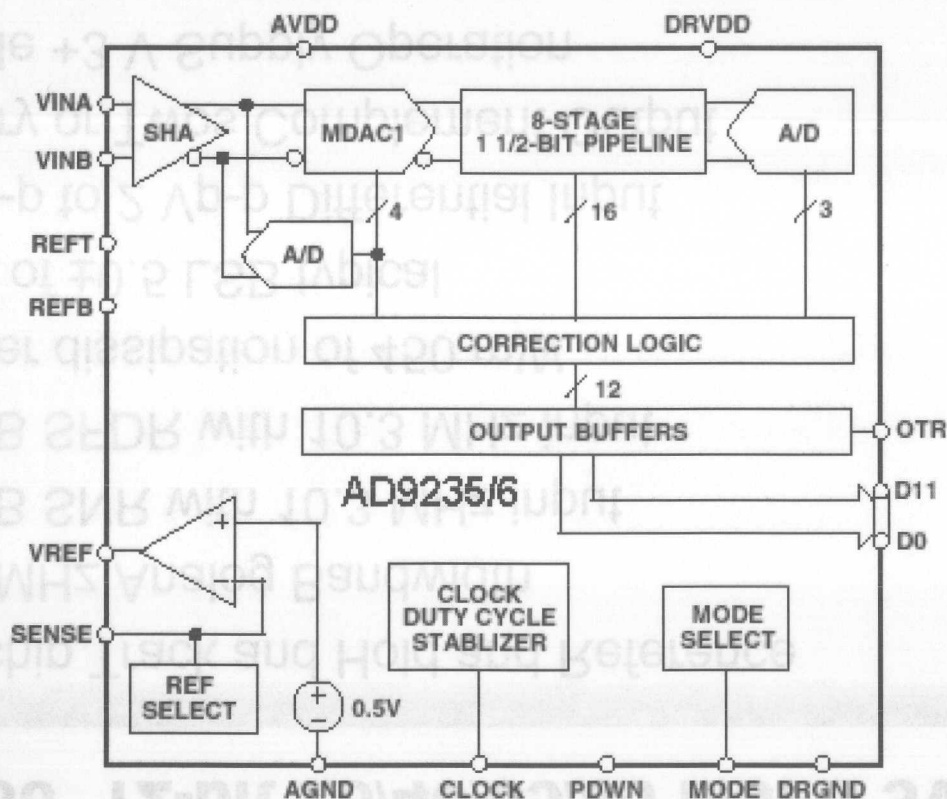
AD9218 10-Bit, 40/65/80/105 MSPS 3 V Dual ADC



AD9218 10-Bit, 40/65/80/105 MSPS 3 V Dual ADC

- Low Power: 200 mW at 105 MSPS per Channel
- On-Chip Reference and Track-and-Hold
- 300 MHz Analog Bandwidth Each Channel
- SNR = 56 dB @ 41 MHz
- 1 V p-p or 2 V p-p Analog Input Range Each Channel
- Single 3.0 V Supply Operation (2.7 V – 3.6 V)
- Power-Down Mode for Single Channel Operation
- Twos Complement or Offset Binary Output Mode
- Output Data Alignment Mode
- Pin-Compatible with 8-Bit AD9288
- -75 dBc Crosstalk between Channels

AD9235/36 12-bit 20/40/65/80 MSPS 3V ADC

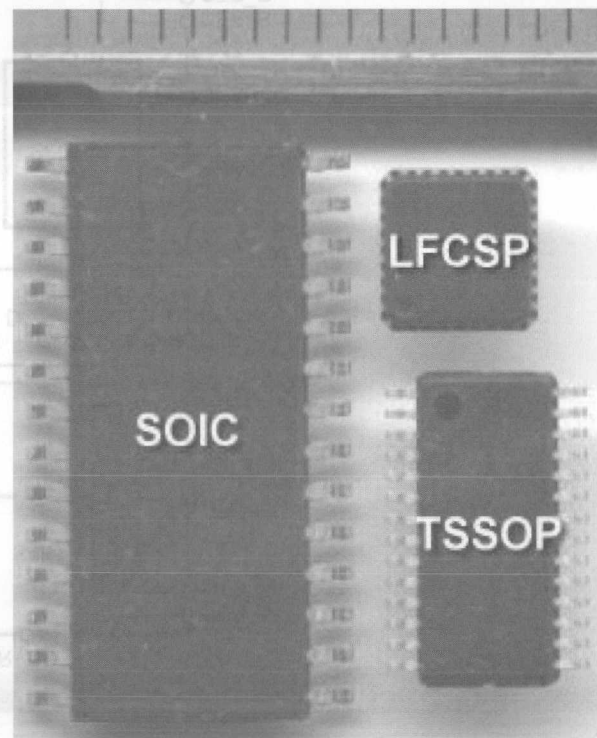


AD9235/36 12-bit 20/40/65/80 MSPS 3V ADC

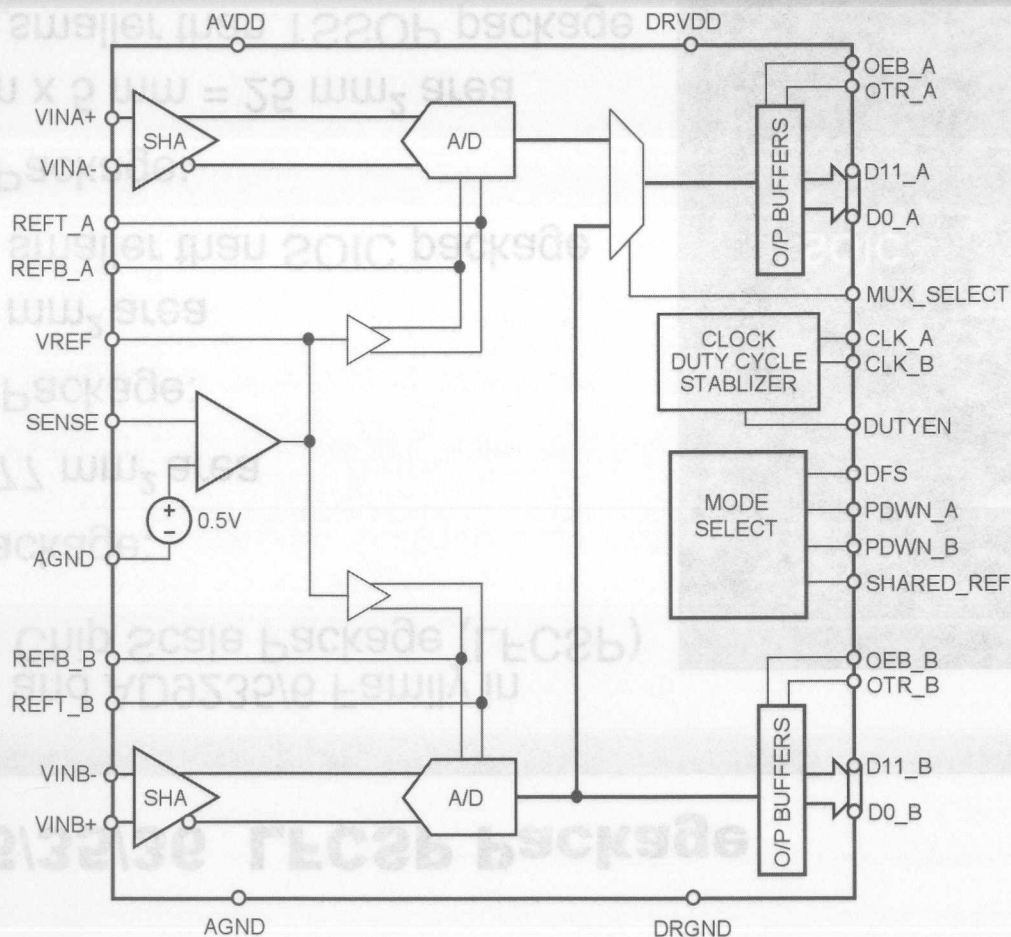
- On-chip Track and Hold and Reference
- 200 MHz Analog Bandwidth
- 69 dB SNR with 10.3 MHz input
- 80 dB SFDR with 10.3 MHz input
- Power dissipation of 450 mW
- DNL of ± 0.5 LSB typical
- 1 Vp-p to 2 Vp-p Differential Input
- Binary or Twos Complement Output
- Single +3 V Supply Operation
- 20 and 40, 65 MSPS speed grades (AD9235)
- 28 pin T-SSOP and 32 lead LFCSP
- Pin compatible to AD9215 (10-bit)

AD9215/35/36 LFCSP Package

- AD9215 and AD9235/6 Family in 32-Lead Chip Scale Package (LFCSP)
- SOIC Package:
 - 192.77 mm² area
- TSSOP Package:
 - 63.7 mm² area
 - 67% smaller than SOIC package
- LFCSP Package:
 - 5 mm x 5 mm = 25 mm² area
 - 60% smaller than TSSOP package
 - 87% smaller than SOIC package



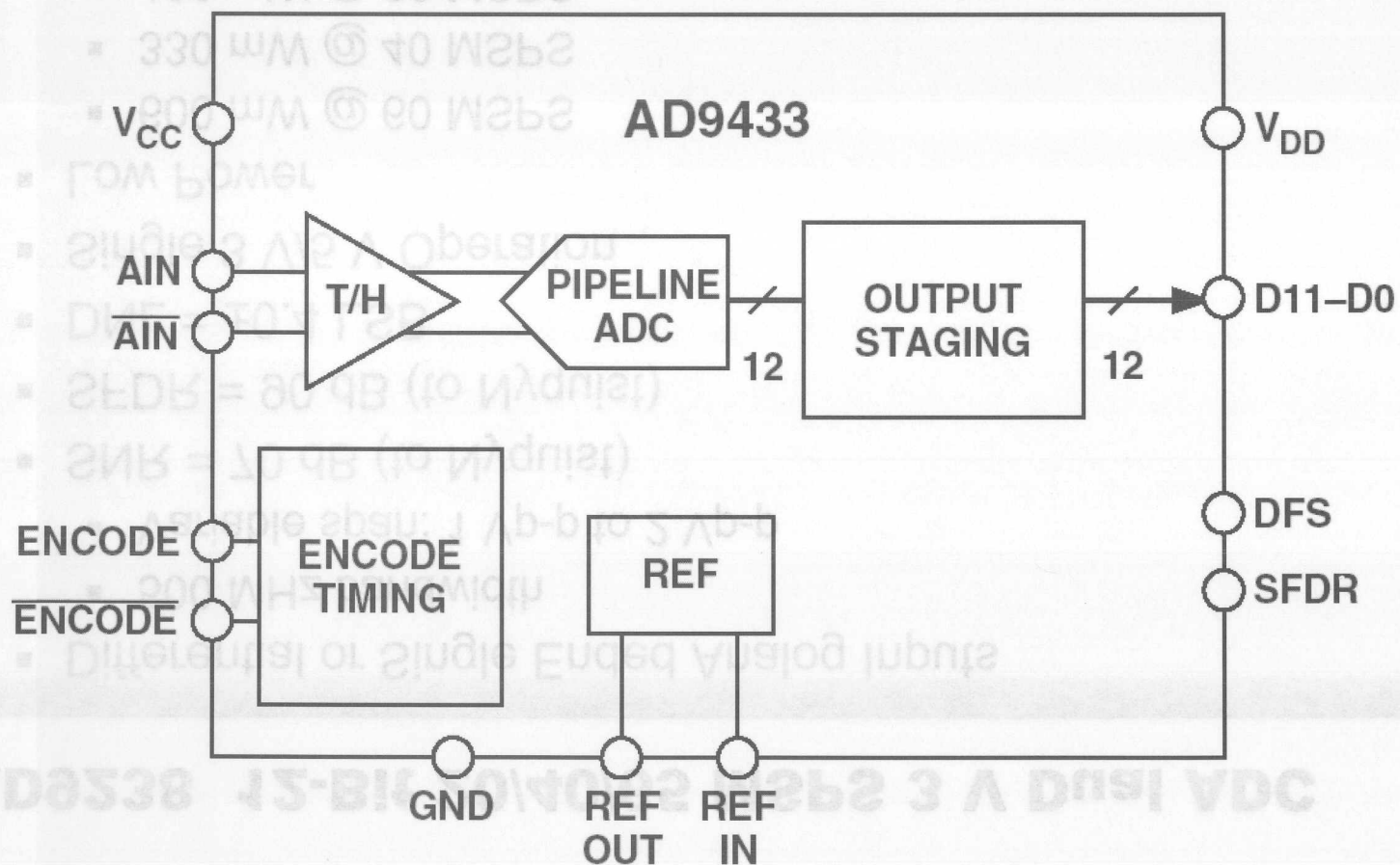
AD9238 12-Bit 20/40/65 MSPS 3 V Dual ADC



AD9238 12-Bit 20/40/65 MSPS 3 V Dual ADC

- Differential or Single Ended Analog Inputs
 - 500 MHz bandwidth
 - Variable span: 1 Vp-p to 2 Vp-p
- SNR = 70 dB (to Nyquist)
- SFDR = 90 dB (to Nyquist)
- DNL = ± 0.4 LSB
- Single 3 V/5 V Operation
- Low Power
 - 600 mW @ 60 MSPS
 - 330 mW @ 40 MSPS
 - 190 mW @ 20 MSPS
- Clock Duty Stabilizer
- Binary or Twos Complement Output Data Format

AD9433 12-Bit, 105/125 MSPS IF Sampling ADC



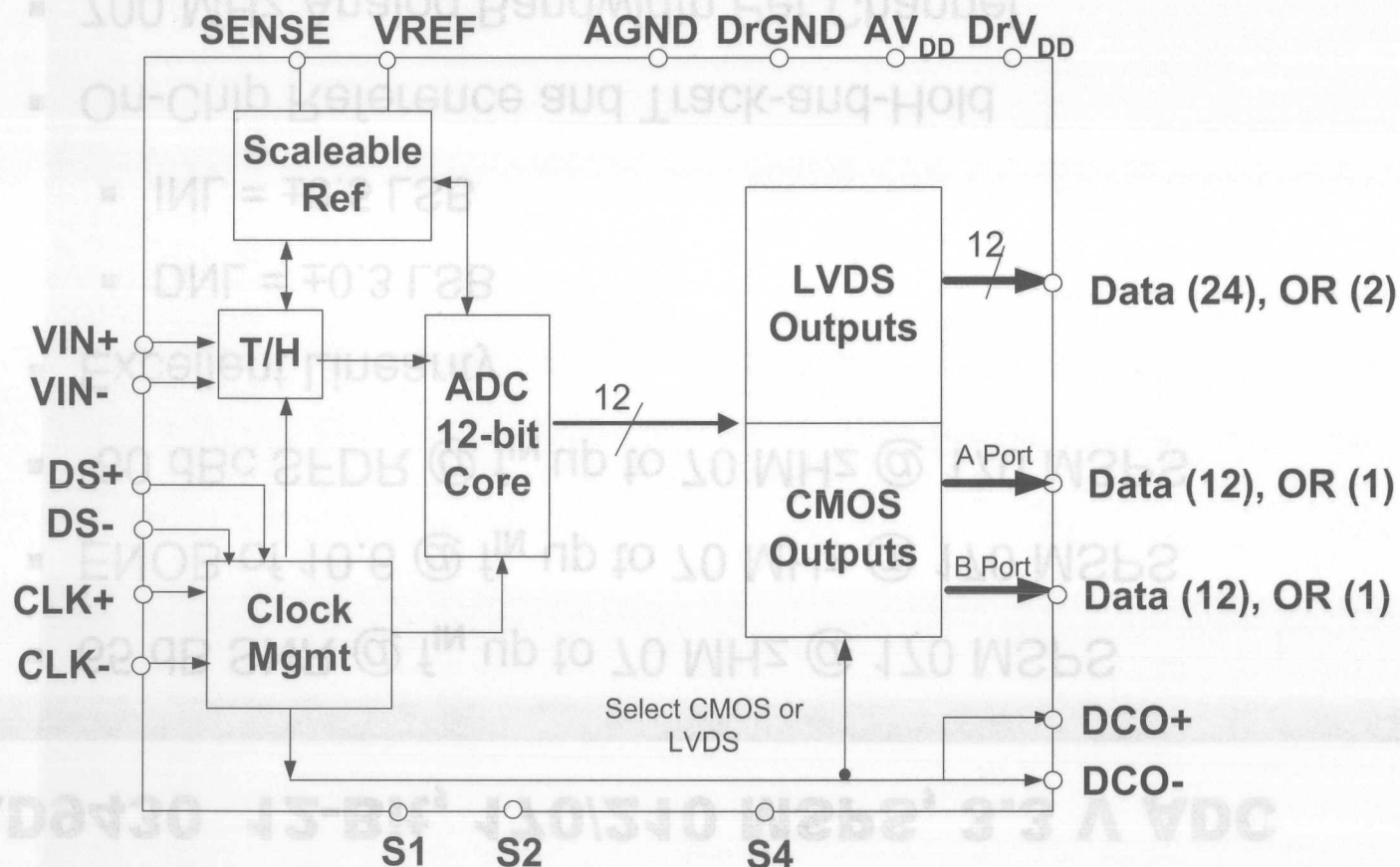
AD9433 12-Bit, 105/125 MSPS IF Sampling ADC

- IF Sampling up to 350 MHz
- Selectable SFDR Mode for Improved SFDR
- 1 V p-p or 2 V p-p Input Voltage Range
- Excellent Linearity:
 - –DNL: ± 0.25 LSB (typ)
 - –INL: ± 0.5 LSB (typ)
- 750 MHz Full Power Analog Bandwidth
- SNR = 68 dB @ f_{IN} up to Nyquist
- SFDR = 90 dBc @ f_{IN} up to 125 MHz
- SFDR = 80 dBc @ f_{IN} up to 250 MHz

AD9433 12-Bit, 105/125 MSPS IF Sampling ADC

- On-Chip Reference and Track/Hold
- Twos Complement or Binary Output Data Format
- 5.0 V Analog Supply Operation
- 2.5 V to 3.3 V TTL/CMOS Outputs
- Power Dissipation = 1.2 W @ 105 MSPS
- Pin-Compatible to AD9432

AD9430 12-Bit, 170/210 MSPS ADC



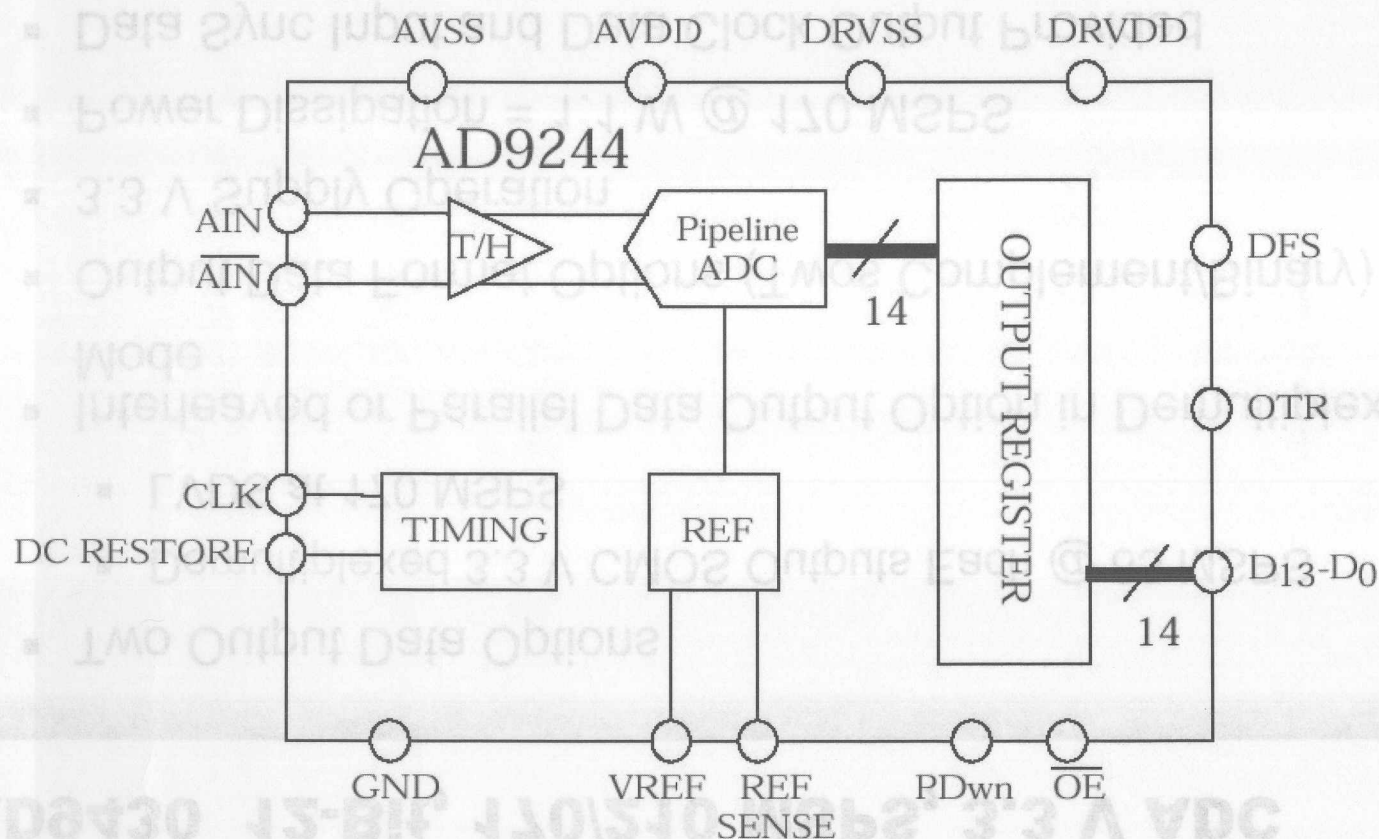
AD9430 12-Bit, 170/210 MSPS, 3.3 V ADC

- 65 dB SNR @ f_{IN} up to 70 MHz @ 170 MSPS
- ENOB of 10.6 @ f_{IN} up to 70 MHz @ 170 MSPS
- -80 dBc SFDR @ f_{IN} up to 70 MHz @ 170 MSPS
- Excellent Linearity
 - DNL = ± 0.3 LSB
 - INL = ± 0.5 LSB
- On-Chip Reference and Track-and-Hold
- 700 MHz Analog Bandwidth Per Channel
- 1.5 V_{p-p} Analog Input Range

AD9430 12-Bit, 170/210 MSPS, 3.3 V ADC

- Two Output Data Options
 - Demultiplexed 3.3 V CMOS Outputs Each @ 85 MSPS
 - LVDS at 170 MSPS
- Interleaved or Parallel Data Output Option in Demultiplexed Mode
- Output Data Format Options (Twos Complement/Binary)
- 3.3 V Supply Operation
- Power Dissipation = 1.1 W @ 170 MSPS
- Data Sync Input and Data Clock Output Provided
- Clock Duty Cycle Stabilizer
- 100 e-PAD TQFP

AD9244 IF Sampling, Low Power CMOS 14-Bit, 40/65 MSPS ADC

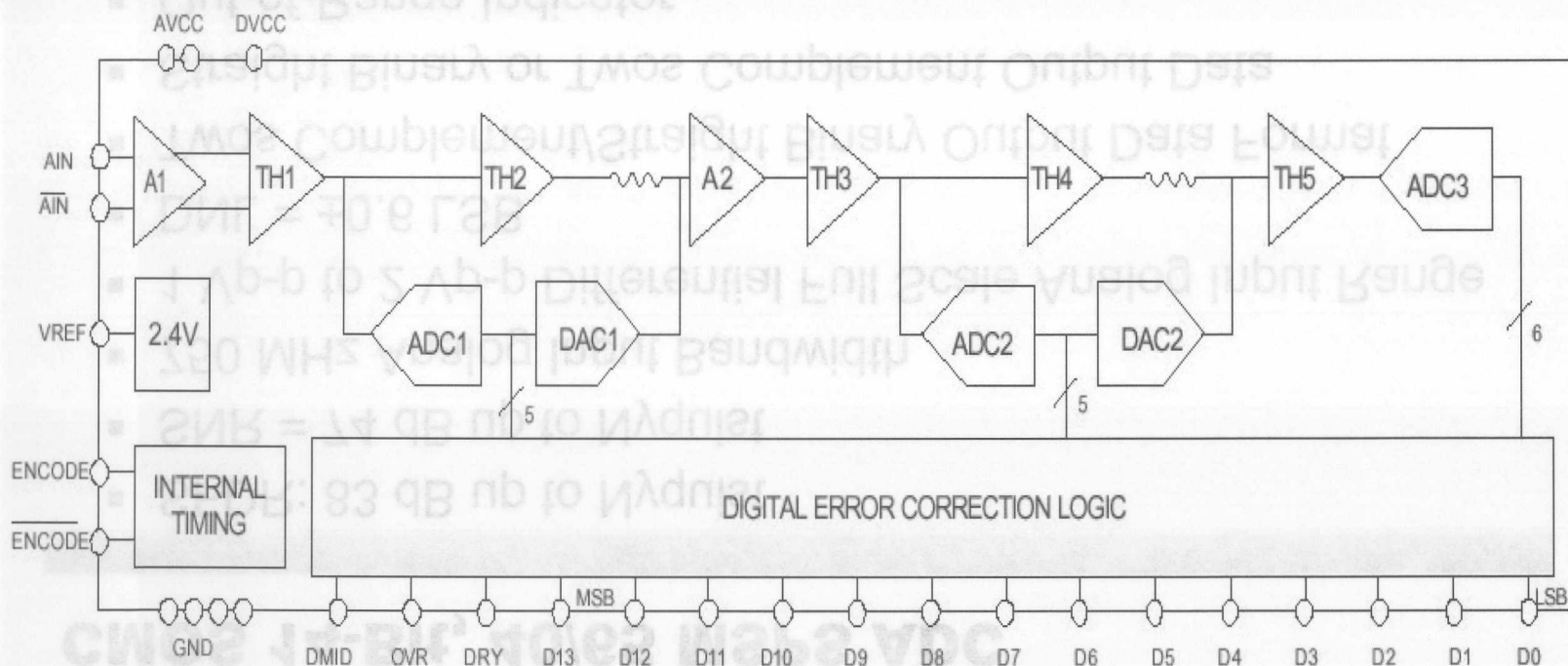


AD9244 IF Sampling, Low Power CMOS 14-Bit, 40/65 MSPS ADC

- SFDR: 83 dB up to Nyquist
- SNR = 74 dB up to Nyquist
- 750 MHz Analog Input Bandwidth
- 1 V_{p-p} to 2 V_{p-p} Differential Full Scale Analog Input Range
- DNL = ±0.6 LSB
- Twos Complement/Straight Binary Output Data Format
- Straight Binary or Twos Complement Output Data
- Out-of-Range Indicator
- Low Power: 590 mW at 65 MSPS with f_{IN} up to Nyquist
- 340 mW at 40 MSPS with f_{IN} up to Nyquist
- 48-Lead LQFP Package
- Pin-Compatible to AD9226 (12-Bit)

AD6645 14-Bit 80/105 MSPS A/D Converter

Designed for multichannel multimode receivers, the AD6645 is also useful in single-channel, wide bandwidth systems



AD6645 14-Bit, 80/105 MSPS A/D Converter

- 250 MHz Bandwidth
- Differential Inputs with 2.2 V_{p-p} Input Range
- SNR = 75 dB with 15 MHz f_{IN} @ 80 MSPS
- SFDR = 89 dBc with 70 MHz f_{IN} @ 80 MSPS
- 100 dB Multitone SFDR
- IF Sampling to 200 MHz
- 0.1 ps Sampling Jitter
- Single 5 V Analog Supply, 1.5 W Dissipation
- Output Data 3.3 V or 5 V CMOS-Compatible
- Pin-Compatible to AD6644

AD6645 14-Bit, 80/105 MSPS ADC

- Enabling Technology for SoftCell Multicarrier Receiver Platform
 - 100 dBc Multitone SFDR
 - 89 dBc FS SFDR
 - 75 dB SNR
- WB-CDMA Receiver Design
 - Wide band single carrier solution
 - Dynamic range provides flexible filtering for emerging 3G blocking specifications

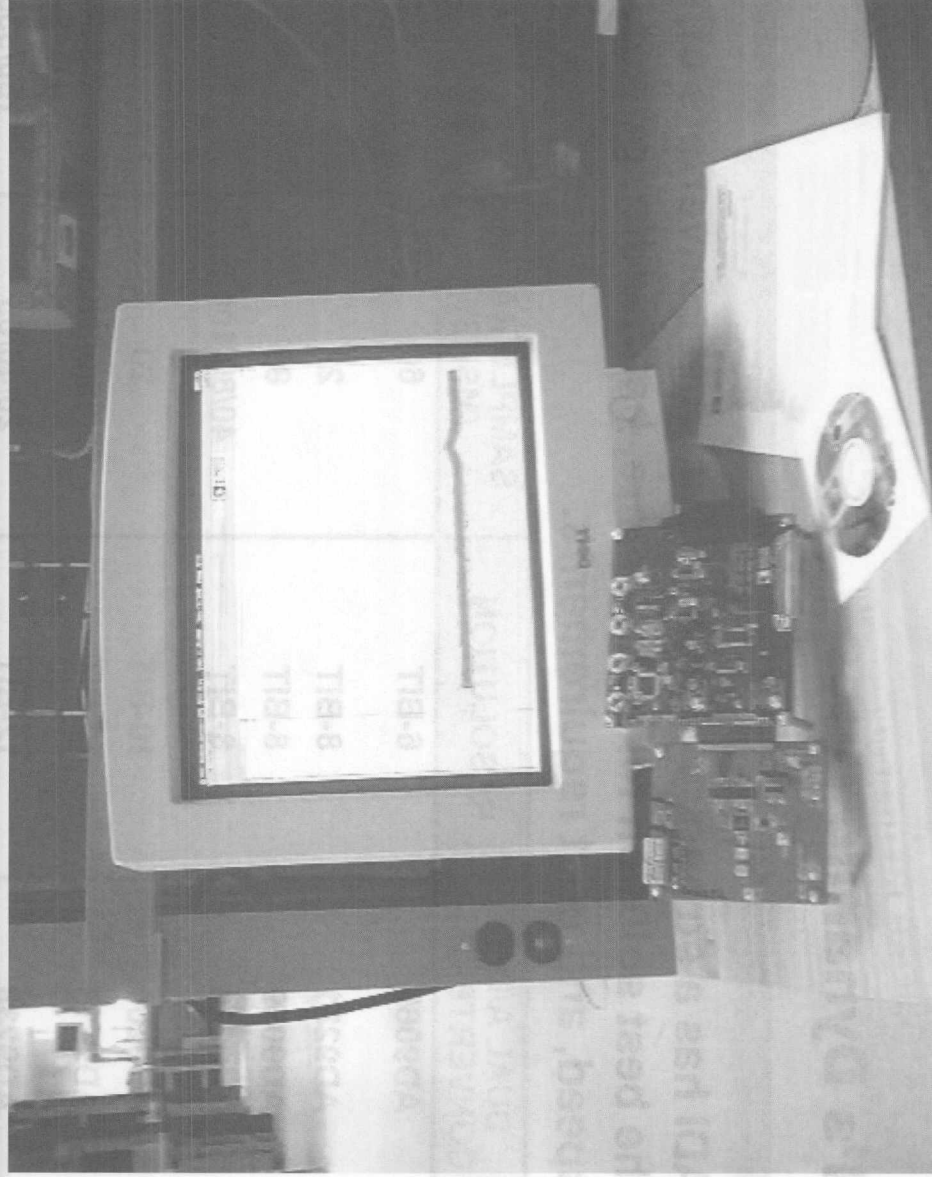


ADI's Dynamic Duos

ADI has a strong portfolio of dual A/D converters offering the best solution for sample rate, bandwidth, power, speed, and cost requirements.

DUAL A/D CONVERTERS	RESOLUTION	SAMPLE RATE (MSPS)	POWER (mW)
AD9066	6-BIT	60	400
AD9281	8-BIT	28	225
AD9059	8-BIT	80	400
AD9288	8-BIT	40/80/100	156/171/180
AD9201	10-BIT	20	215
AD9218	10-BIT	40/65/80/105	350/550
AD9238	12-BIT	20/40/65	180/330/600
AD10242	12-BIT	40	1750
AD10265	12-BIT	65	2100
AD10201	12-BIT	105	1800

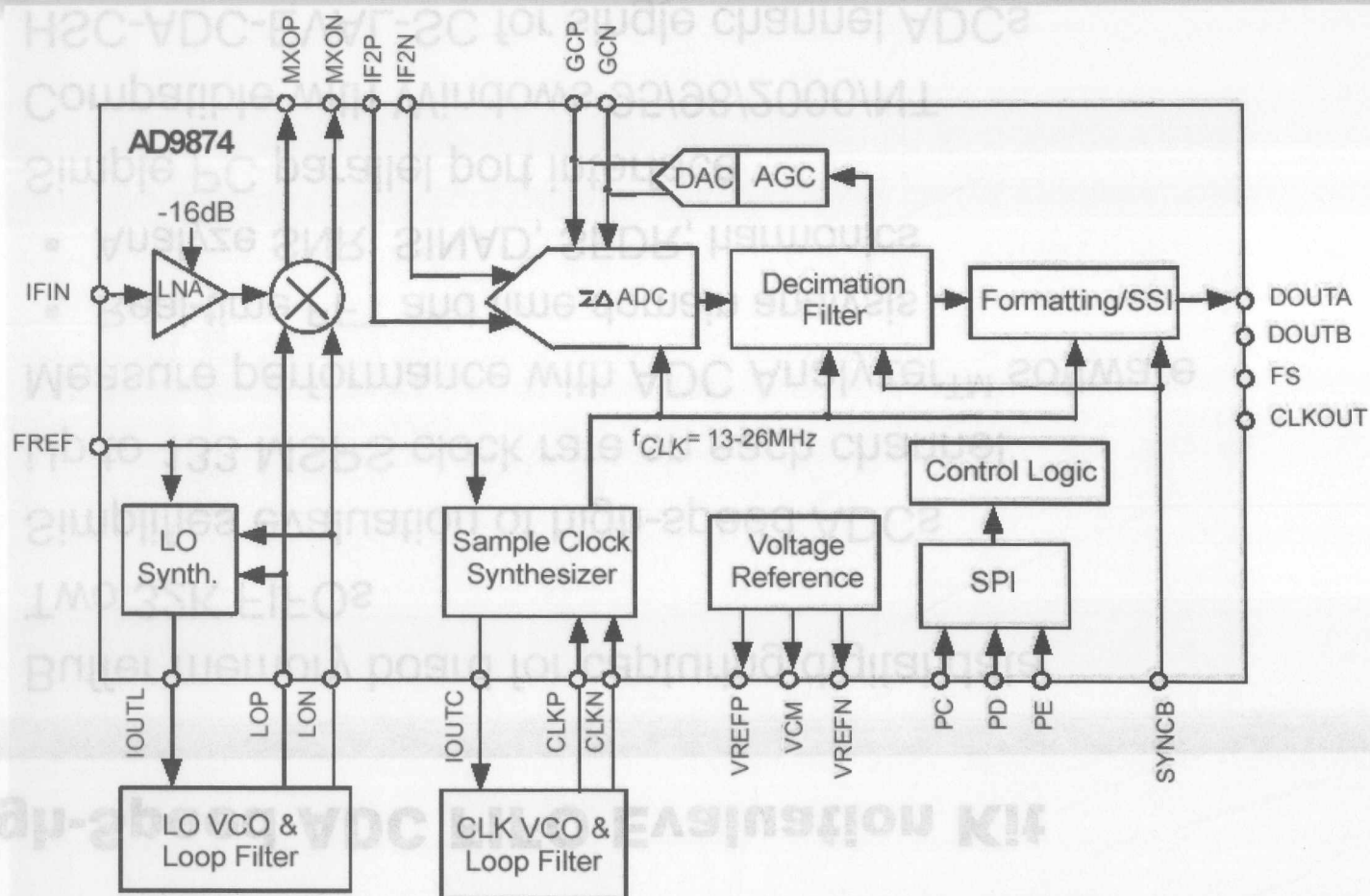
High-Speed ADC FIFO Evaluation Kit



High-Speed ADC FIFO Evaluation Kit

- Buffer memory board for capturing digital data
- Two 32K FIFOs
- Simplifies evaluation of high-speed ADCs
- Up to 133 MSPS clock rate on each channel
- Measure performance with ADC Analyzer™ software
 - Real-time FFT and time domain analysis
 - Analyze SNR, SINAD, SFDR, harmonics
- Simple PC parallel port interface
- Compatible with Windows 95/98/2000/NT
- HSC-ADC-EVAL-SC for single channel ADCs
- HSC-ADC-EVAL-DC for dual or demuxed ADCs
- www.analog.com/hsc-FIFO

AD9874 IF Digitizing Subsystem



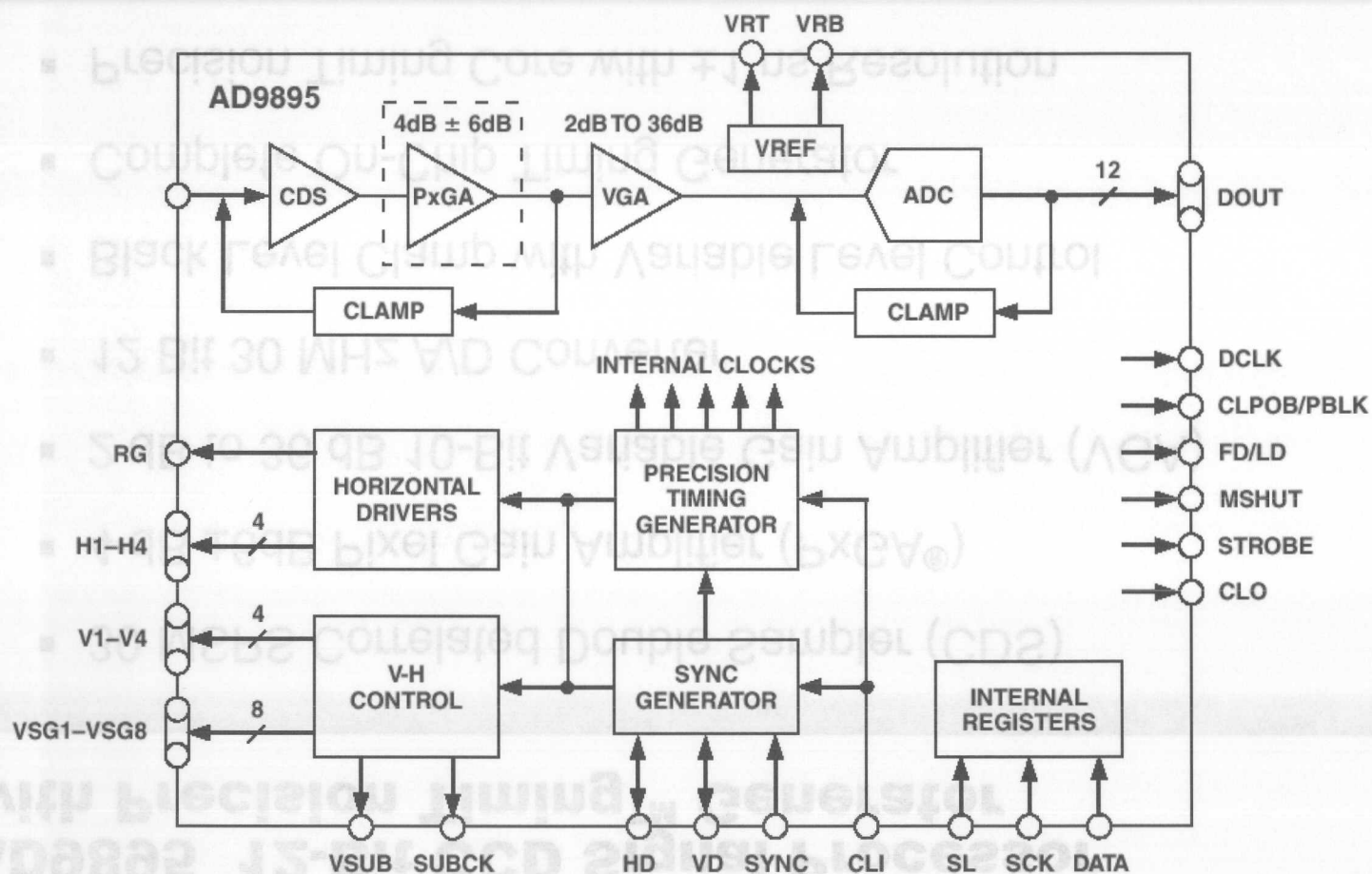
AD9874 IF Digitizing Subsystem

- 10 - 300 MHz Input Frequency
- Baseband (I/Q) Digital Output
- 10 - 270 kHz Output Signal Bandwidth
- 8.7 dB SSB NF (typ.)
- +1.1 dBm IP3 (typ.; max. bias)
- AGC Free Range up to -28 dBm
- 12 dB Continuous AGC Range
- 16 dB Front End Attenuator

AD9874 IF Digitizing Subsystem

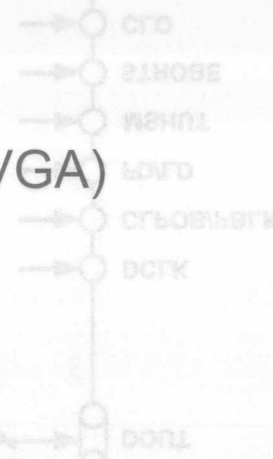
- LO and Sampling Clock Synthesizers
- Programmable decimation factor, output format, AGC and synthesizer settings
- 370 Ω Input Impedance
- 2.7 V - 3.6 V Supply Voltage
- Low Current: 22 mA (typ., max. bias)
- 48-Pin LQFP package (1.4mm thick)
- Applications:
 - Portable and Mobile Radio Products
 - Digital UHF/VHF FDMA products
 - TETRA, APCO25, GSM/EDGE

AD9895 12-Bit CCD Signal Processor with Precision Timing™ Generator



AD9895 12-Bit CCD Signal Processor with Precision Timing™ Generator

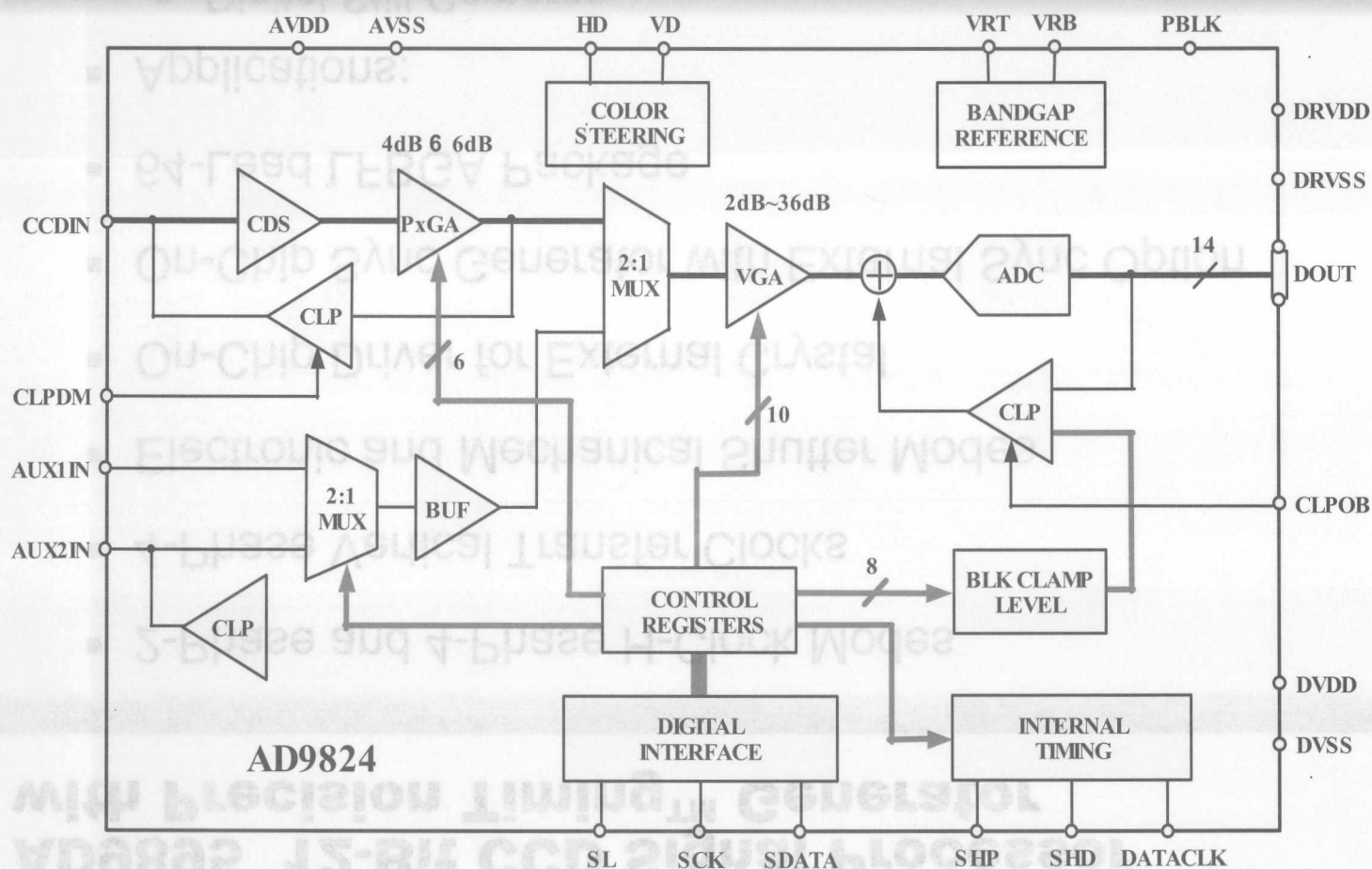
- 30 MSPS Correlated Double Sampler (CDS)
- 4 dB ± 6 dB Pixel Gain Amplifier (PxGA®)
- 2 dB to 36 dB 10-Bit Variable Gain Amplifier (VGA)
- 12 Bit 30 MHz A/D Converter
- Black Level Clamp with Variable Level Control
- Complete On-Chip Timing Generator
- Precision Timing Core with ± 1 ns Resolution
- On-Chip 5 V Horizontal and RG Drivers



AD9895 12-Bit CCD Signal Processor with Precision Timing™ Generator

- 2-Phase and 4-Phase H-Clock Modes
- 4-Phase Vertical Transfer Clocks
- Electronic and Mechanical Shutter Modes
- On-Chip Driver for External Crystal
- On-Chip Sync Generator with External Sync Option
- 64-Lead LFBGA Package
- Applications:
 - Digital Still Cameras
 - Industrial Imaging

AD9824 14-Bit, 30 MSPS Analog Front-end for Digital Imaging Applications



AD9824 14-Bit, 30 MSPS Analog Front-end for Digital Imaging Applications

- 14-bit, 30MSPS ADC with high-performance analog processing front-end (CDS, PGA)
- 48-pin LFCSP package – smaller than the TQFP
- 2 - 36dB 10-bit Variable Gain Amplifier (VGA)
- PxGA™ function for added color gain
- Lowest noise performance in the market
- 2 Auxiliary Inputs
- Low power – 153 mW @3 V
- Markets
 - High Performance Digital Still Cameras
 - Scientific / Industrial Imaging

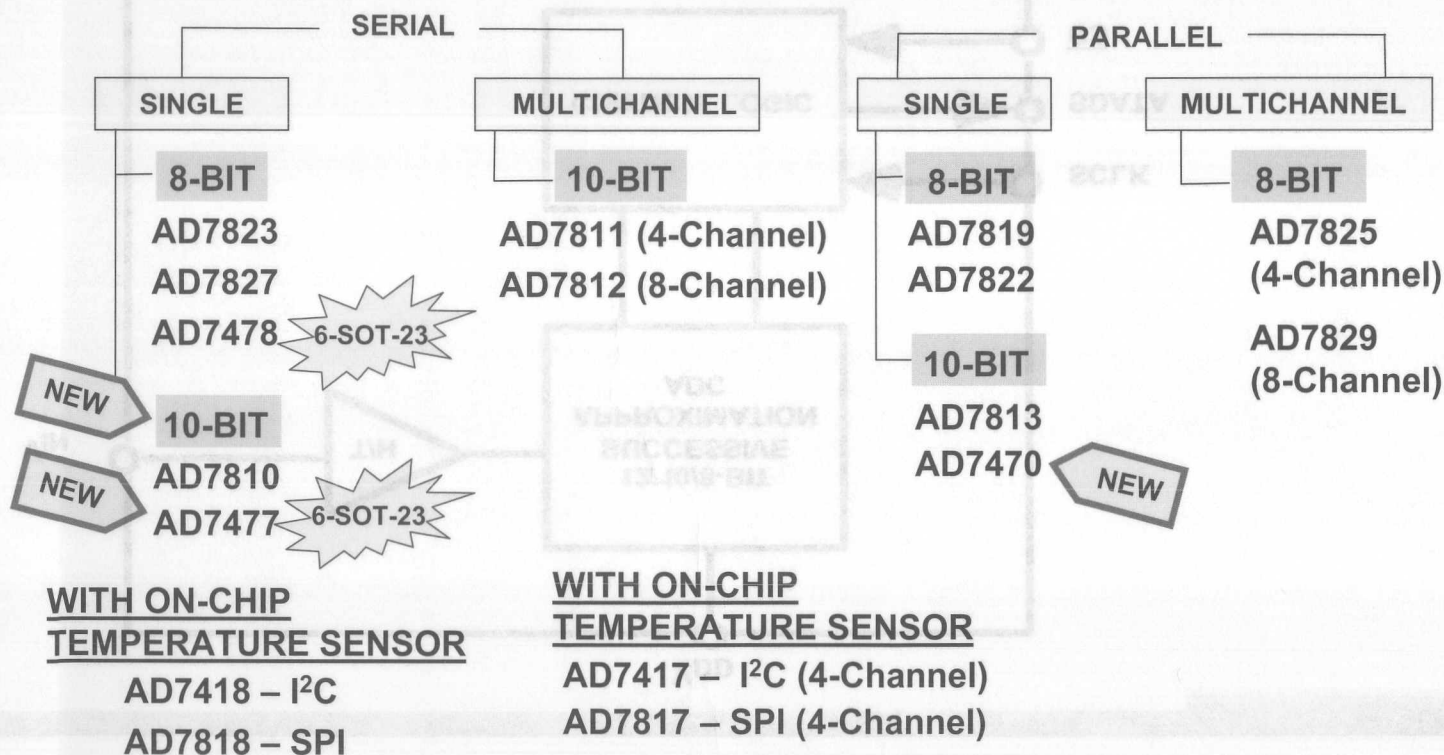
- Scientific & Industrial Imaging
- High Performance Digital Still Cameras

Markets

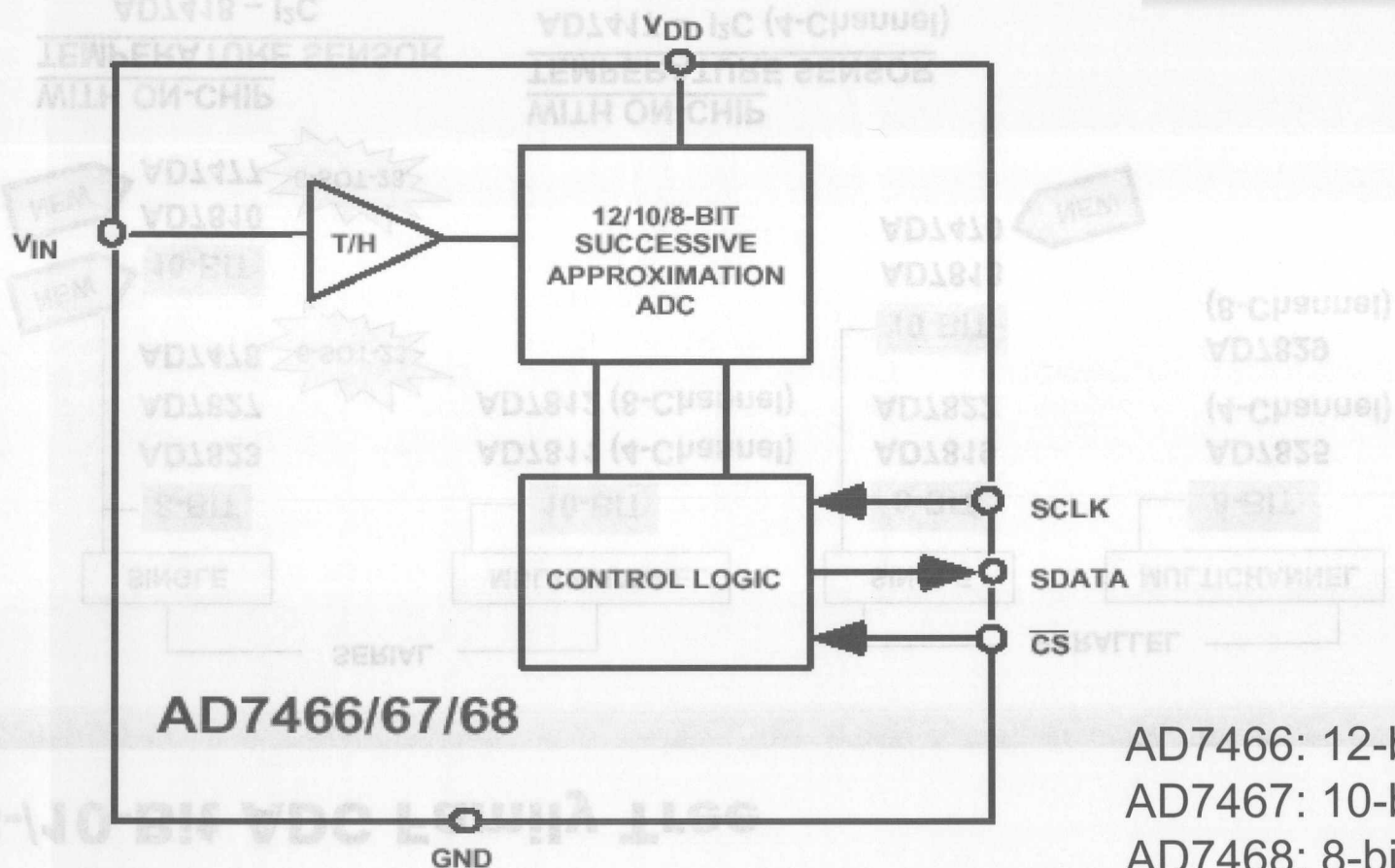
- Low power – 123 mW @3 V
- 5 Auxiliary Inputs
- Lowest noise performance in the market
- 16x64 ADCs
- 5 – 30dB 10-bit Variable Gain Amplifier (VGA)
- 48-pin LFCSP package – smaller than the TQFP
- processing front-end (CDS, PGA)
- 30MS/s VCA with high performance analog front-end

General-Purpose ADCs

8-/10-Bit ADC Family Tree



AD7466/67/68 1.8 V, Micro-Power, 12-/10-/8-Bit 100 kSPS ADCs in 6-Lead SOT-23



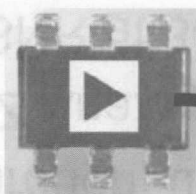
AD7466/67/68 1.8 V, Micropower, 12-/10-/8-Bit 100 kSPS ADCs in 6-Lead SOT-23

- World's Lowest Power ADCs:
 - 1 mW max at 100 kSPS with 3 V supplies
 - 0.6 mW max at 100 kSPS with 1.8 V supplies
 - Standby mode: 1 μ A max
- Specified for V_{DD} of 1.8 V – 3.3 V
- Fast Throughput Rate: 100 kSPS
- 500 kHz Analog Bandwidth
- 70 dB SNR at 30 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High-Speed Serial Interface
 - SPI/QSPI/ μ Wire/DSP compatible
- 6-Lead SOT-23 Package

New AD7476A/77A/78A Family

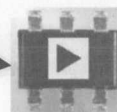
We have just **halved** the size of the worlds smallest ADC!

SOT-23
6-Lead



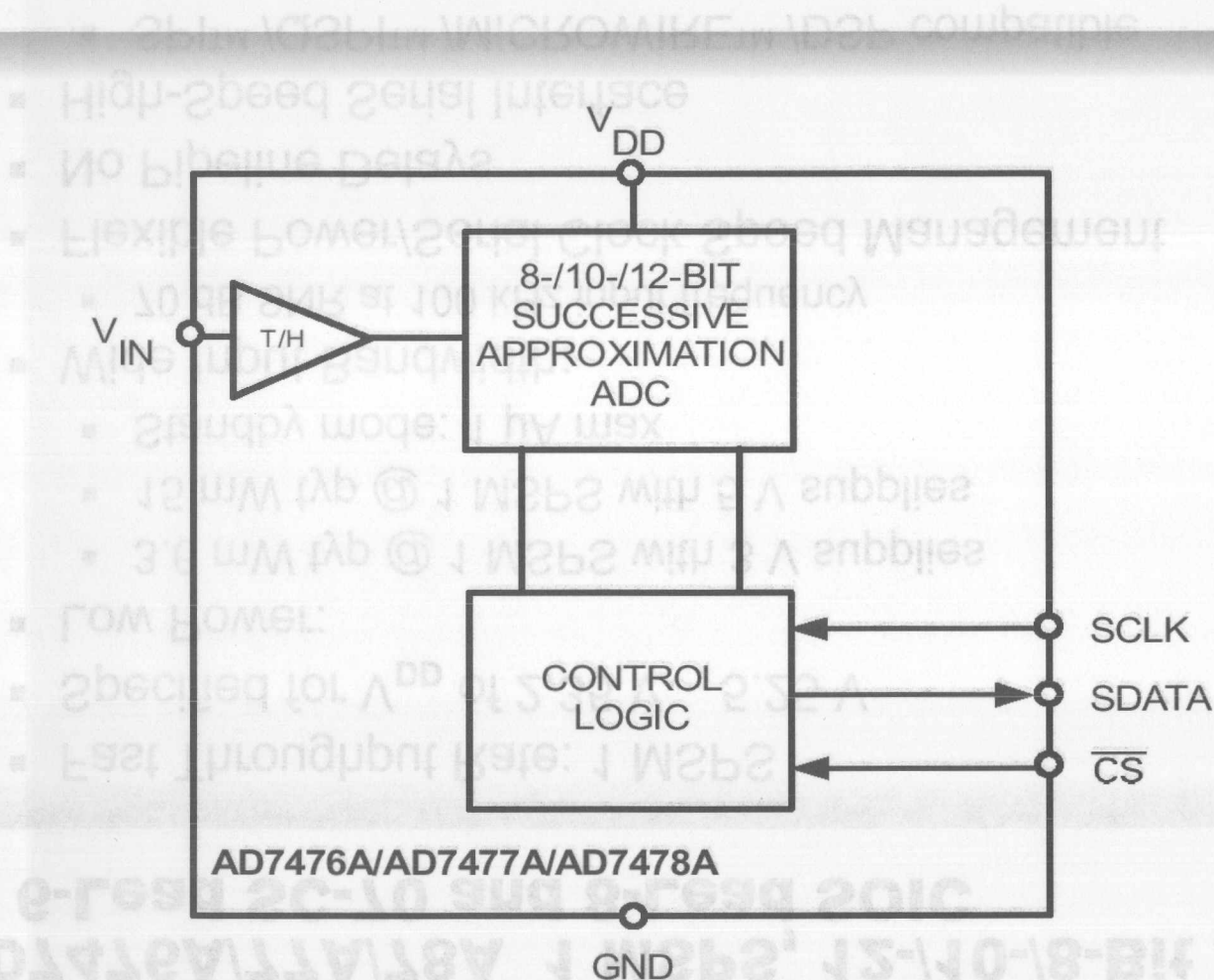
- ✓ High Speed SPI/QSPI/DSP Compatible Interface
- ✓ Low-Power: 3.6 mW typ @ 1MSPS with 3 V Supplies
- ✓ Standby Mode: 1 uA max
- ✓ No Pipeline Delays

- ✓ Fast Throughput Rate: 1MSPS(A)/600ksps(B)
- ✓ Wide Input Bandwidth: 5 MHz typ



SC-70
6-Lead

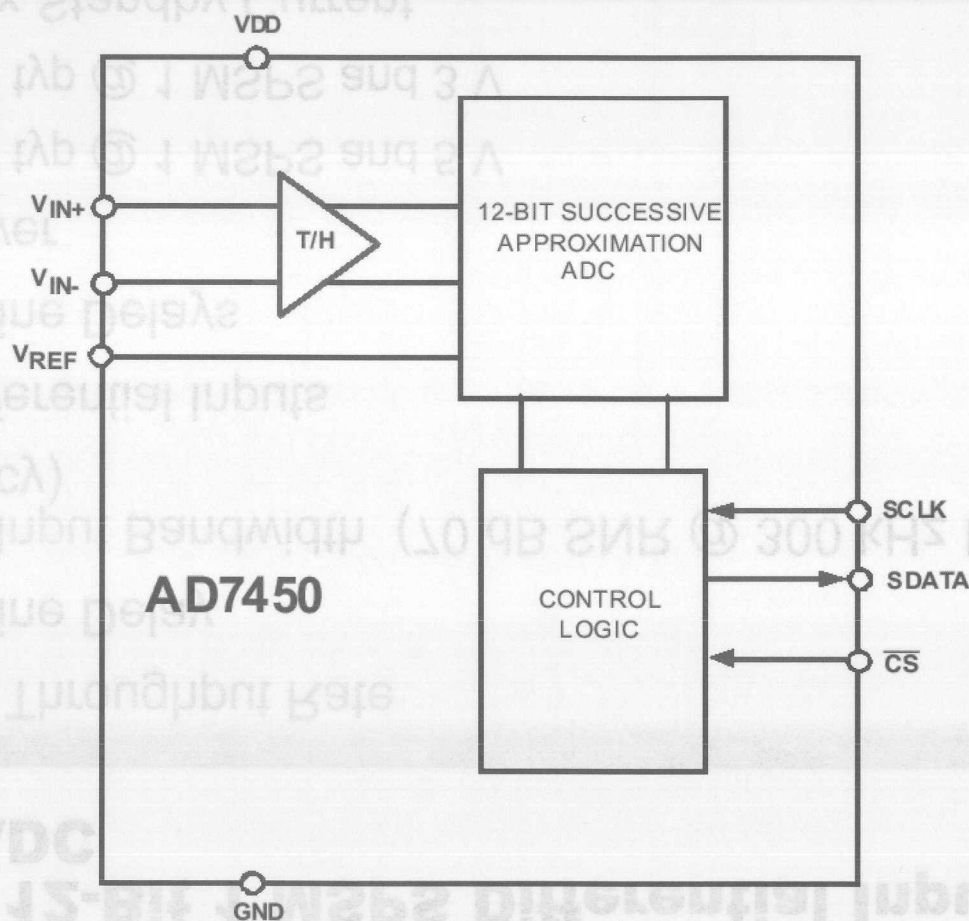
AD7476A/77A/78A 1 MSPS, 12-/10-/8-Bit ADCs in 6-Lead SC-70 and 8-Lead SOIC



AD7476A/77A/78A 1 MSPS, 12-/10-/8-Bit ADCs in 6-Lead SC-70 and 8-Lead SOIC

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.35 V – 5.25 V
- Low Power:
 - 3.6 mW typ @ 1 MSPS with 3 V supplies
 - 15 mW typ @ 1 MSPS with 5 V supplies
 - Standby mode: 1 μ A max
- Wide Input Bandwidth:
 - 70 dB SNR at 100 kHz input frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High-Speed Serial Interface
 - SPI™ /QSPI™ /MICROWIRE™ /DSP compatible
- 6-Lead SC-70 Package
- 8-Lead SOIC Package

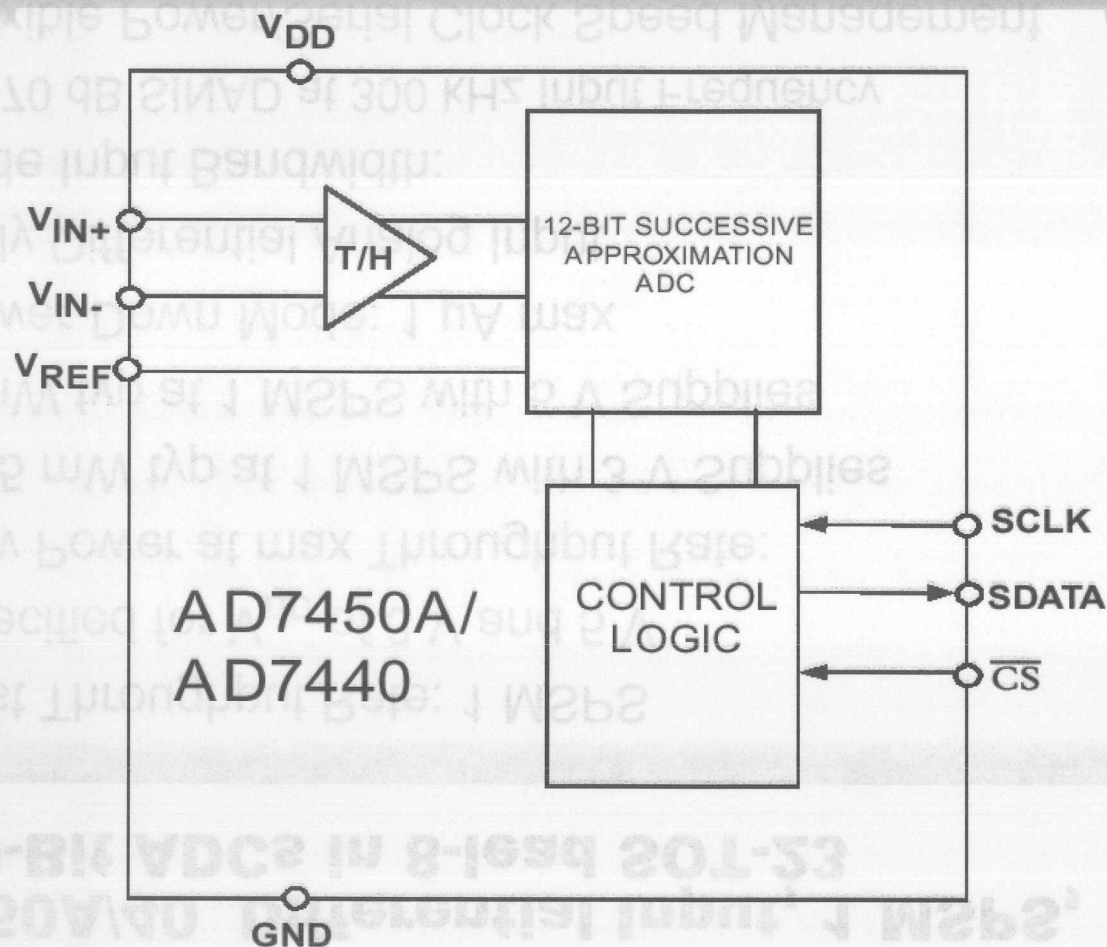
AD7450 12-Bit 1 MSPS Differential Input 3 V/5 V ADC



AD7450 12-Bit 1 MSPS Differential Input 3 V/5 V ADC

- 1 MSPS Throughput Rate
- No Pipeline Delay
- 20 MHz Input Bandwidth (70 dB SNR @ 300 kHz Input Frequency)
- Fully Differential Inputs
- No Pipeline Delays
- Low Power
 - 9 mW typ @ 1 MSPS and 5 V
 - 5 mW typ @ 1 MSPS and 3 V
- 1 μ A Max Standby Current
- SPI/QSPI/ μ Wire/DSP Compatible Serial Interface
- 8-Pin SOIC and μ SOIC Packages

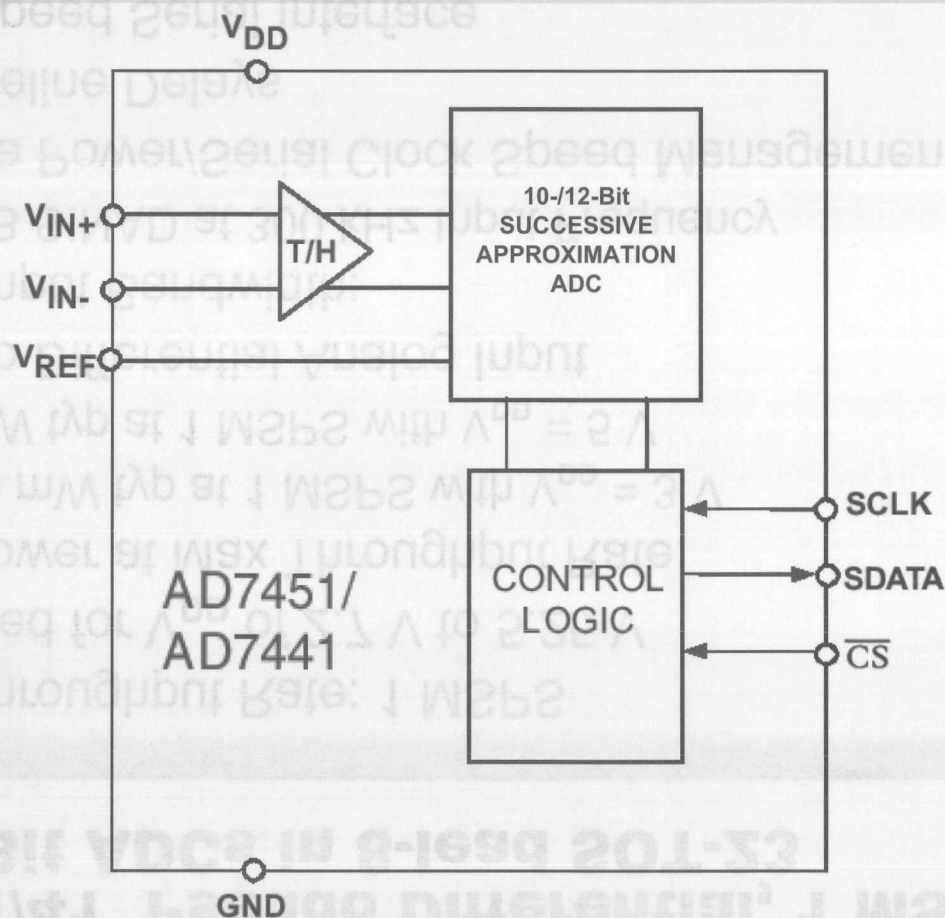
AD7450A/40 Differential Input, 1 MSPS, 12-/10-Bit ADCs in 8-lead SOT-23



AD7450A/40 Differential Input, 1 MSPS, 12-/10-Bit ADCs in 8-lead SOT-23

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 3 V and 5 V
- Low Power at max Throughput Rate:
 - 3.75 mW typ at 1 MSPS with 3 V Supplies
 - 9 mW typ at 1 MSPS with 5 V Supplies
- Power-Down Mode: 1 μ A max
- Fully Differential Analog Input
- Wide Input Bandwidth:
 - 70 dB SINAD at 300 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface

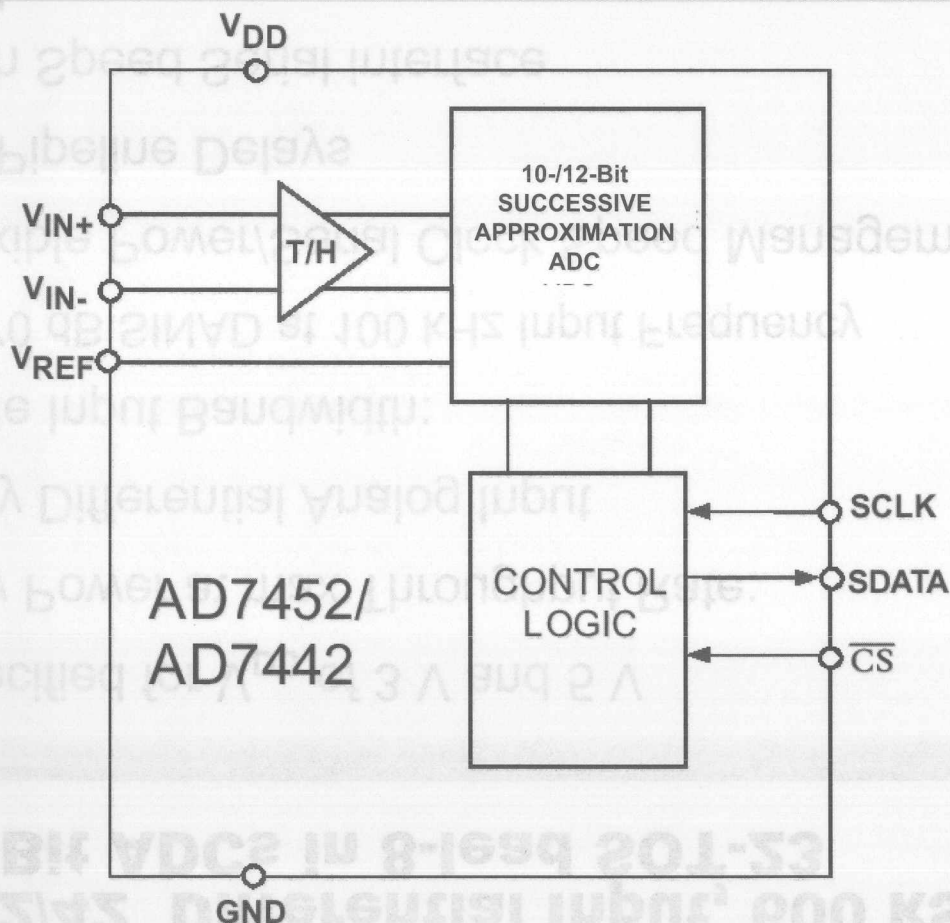
AD7451/41 Pseudo Differential, 1 MSPS, 12-/10-Bit ADCs in 8-lead SOT-23



AD7451/41 Pseudo Differential, 1 MSPS, 12-/10-Bit ADCs in 8-lead SOT-23

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power at Max Throughput Rate:
 - 3.75 mW typ at 1 MSPS with $V_{DD} = 3$ V
 - 9 mW typ at 1 MSPS with $V_{DD} = 5$ V
- Pseudo Differential Analog Input
- Wide Input Bandwidth:
 - 70dB SINAD at 300 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Power-Down Mode: 1 μ A max
- 8 Pin SOT-23 and μ SOIC Packages

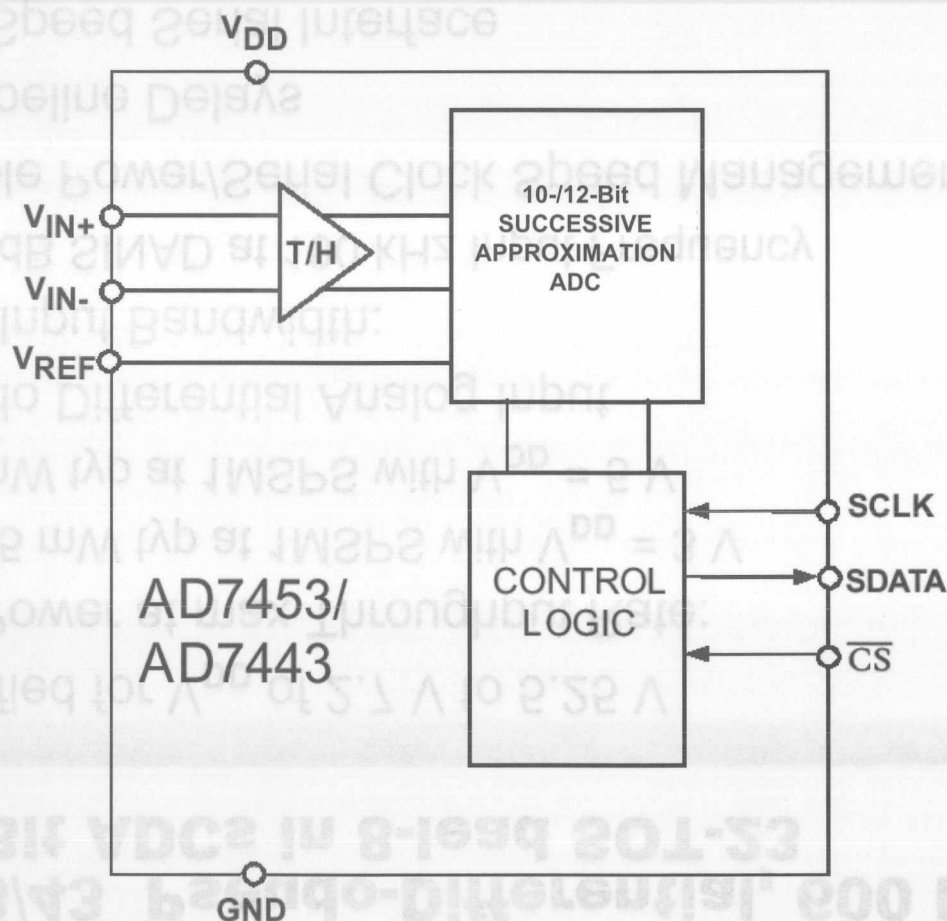
AD7452/42 Differential Input, 600 kSPS, 12-/10-Bit ADCs in 8-lead SOT-23



AD7452/42 Differential Input, 600 kSPS, 12-/10-Bit ADCs in 8-lead SOT-23

- Specified for V_{DD} of 3 V and 5 V
- Low Power at max Throughput Rate:
- Fully Differential Analog Input
- Wide Input Bandwidth:
 - 70 dB SINAD at 100 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Power-Down Mode: 1 μ A max
- 8 Lead SOT-23 and μ SOIC Packages

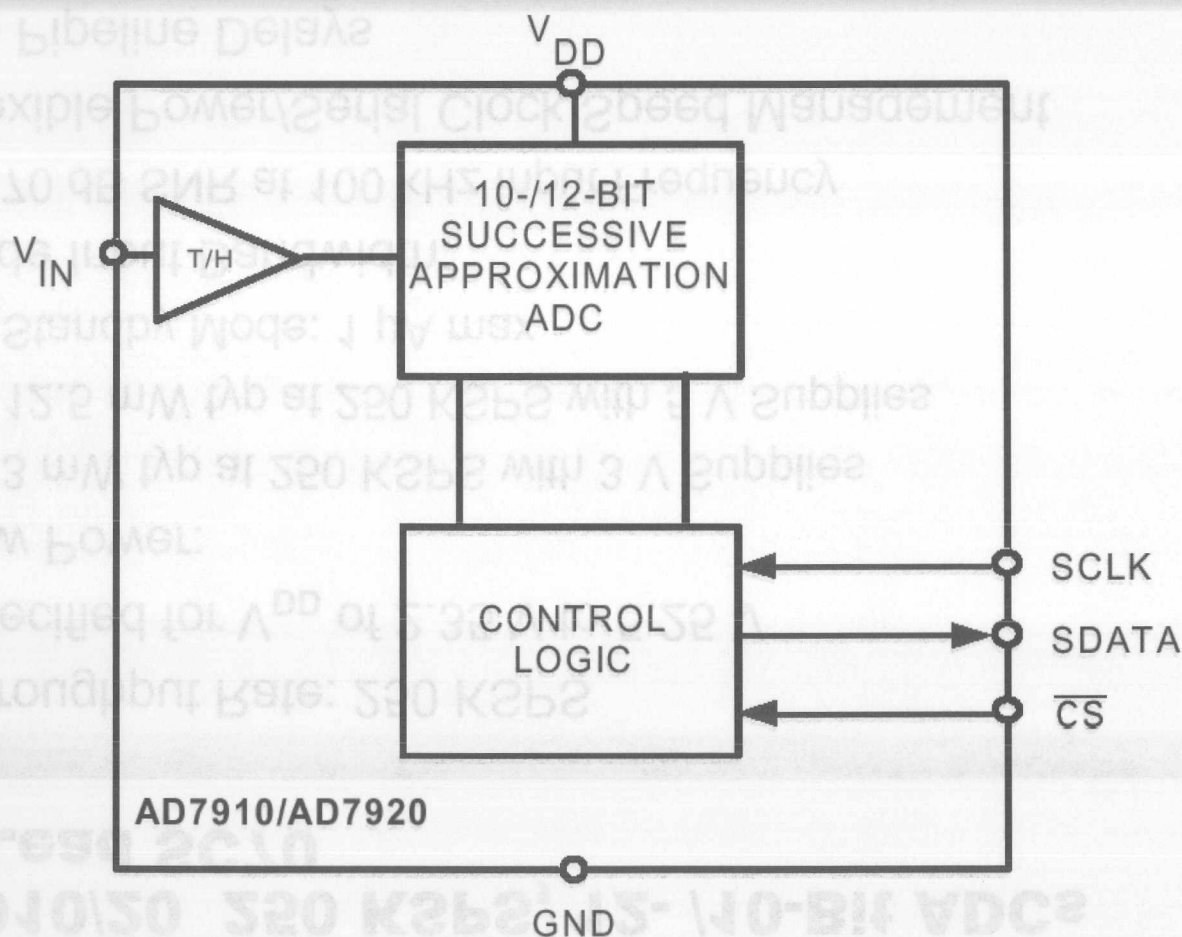
AD7453/43 Pseudo-Differential, 600 kSPS, 12-/10-Bit ADCs in 8-lead SOT-23



AD7453/43 Pseudo-Differential, 600 kSPS, 12-/10-Bit ADCs in 8-lead SOT-23

- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power at max Throughput Rate:
 - 3.75 mW typ at 1MSPS with $V_{DD} = 3$ V
 - 9 mW typ at 1MSPS with $V_{DD} = 5$ V
- Pseudo Differential Analog Input
- Wide Input Bandwidth:
 - 70 dB SINAD at 100 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Power-Down Mode: 1 μ A max
- 8 Pin SOT-23 and μ SOIC Packages

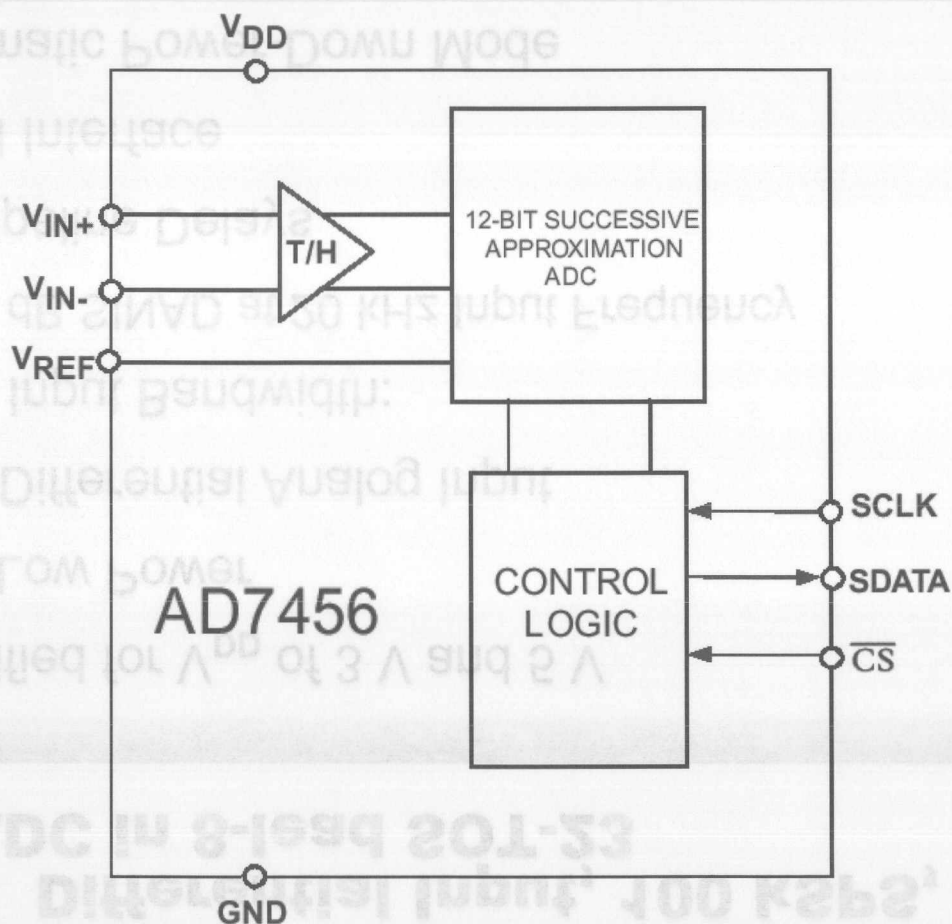
AD7910/20 250 KSPS, 12- /10-Bit ADCs in 6 Lead SC70



AD7910/20 250 KSPS, 12- /10-Bit ADCs in 6 Lead SC70

- Throughput Rate: 250 KSPS
- Specified for V_{DD} of 2.35 V to 5.25 V
- Low Power:
 - 3 mW typ at 250 KSPS with 3 V Supplies
 - 12.5 mW typ at 250 KSPS with 5 V Supplies
 - Standby Mode: 1 μ A max
- Wide Input Bandwidth:
 - 70 dB SNR at 100 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- 6-Lead SC70 Package or 8-Lead SOIC Package

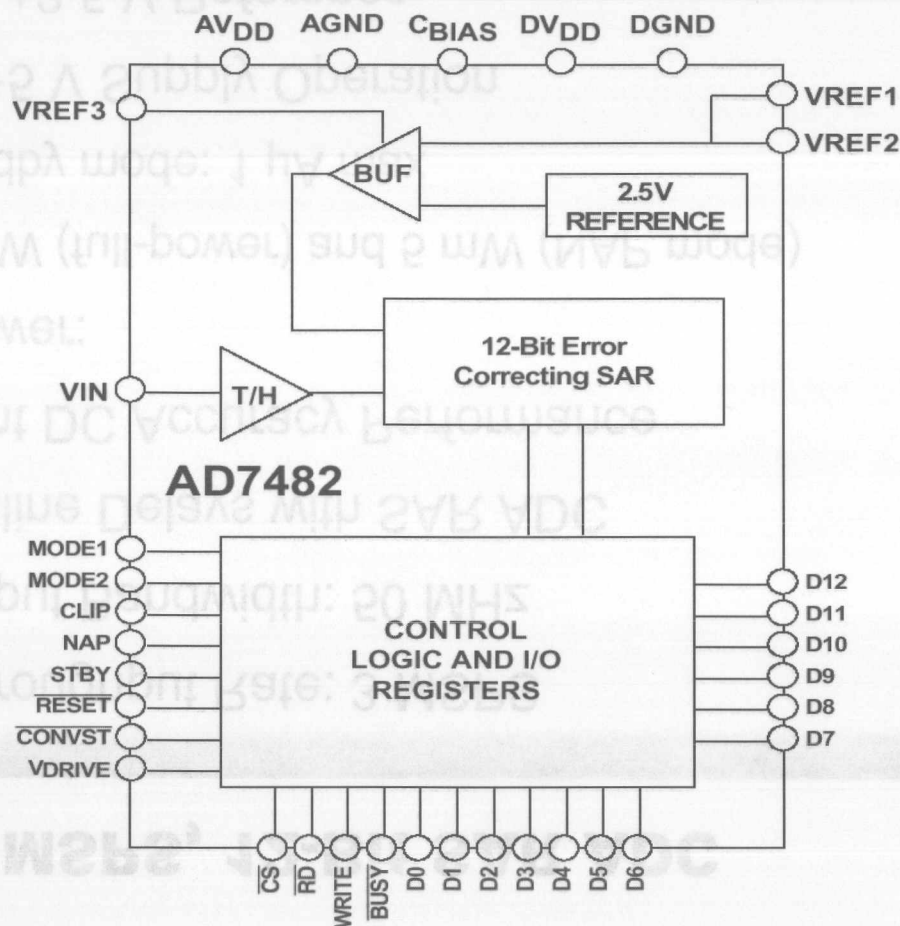
AD7456 Differential Input, 100 kSPS, 12-Bit ADC in 8-lead SOT-23



AD7456 Differential Input, 100 kSPS, 12-Bit ADC in 8-lead SOT-23

- Specified for V_{DD} of 3 V and 5 V
- Very Low Power
- Fully Differential Analog Input
- Wide Input Bandwidth:
 - 70 dB SINAD at 20 kHz Input Frequency
- No Pipeline Delays
- Serial Interface
- Automatic Power-Down Mode
- 8 Pin SOT-23 and μ SOIC Package

AD7482 3 MSPS, 12-Bit SAR ADC



AD7482 3 MSPS, 12-Bit SAR ADC

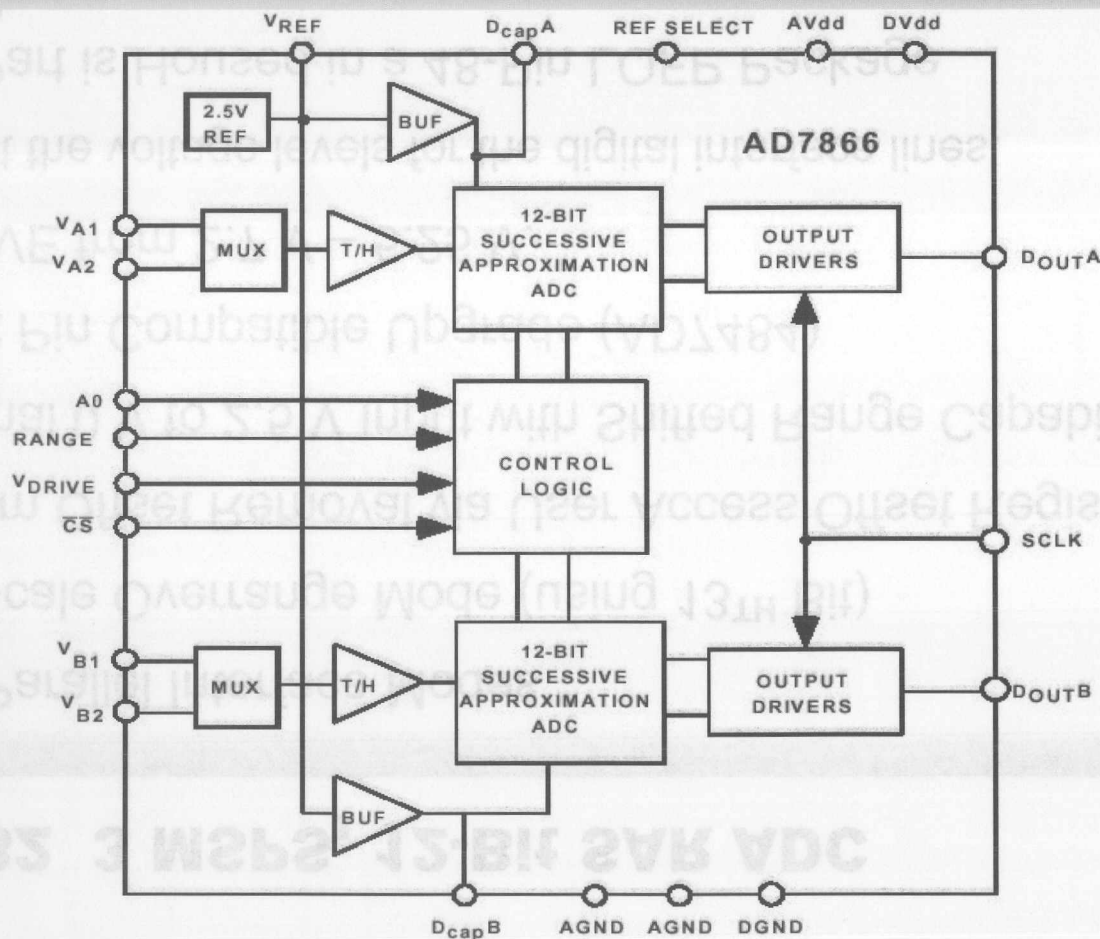
- Fast Throughput Rate: 3 MSPS
- Wide Input Bandwidth: 50 MHz
- No Pipeline Delays with SAR ADC
- Excellent DC Accuracy Performance
- Low Power:
 - 90 mW (full-power) and 5 mW (NAP mode)
 - Standby mode: 1 μ A max
- Single +5 V Supply Operation
- Internal +2.5 V Reference



AD7482 3 MSPS, 12-Bit SAR ADC

- Two Parallel Interface Modes
- Full-Scale Overrange Mode (using 13TH Bit)
- System Offset Removal via User Access Offset Register
- Nominal 0 V to 2.5 V Input with Shifted Range Capability
- 14-Bit Pin Compatible Upgrade (AD7484)
- VDRIVE from 2.7 V – 5.25 V.
 - Set the voltage levels for the digital interface lines.
- The Part is Housed in a 48-Pin LQFP Package
- Specified over a –40° C to +85° C Temperature Range.

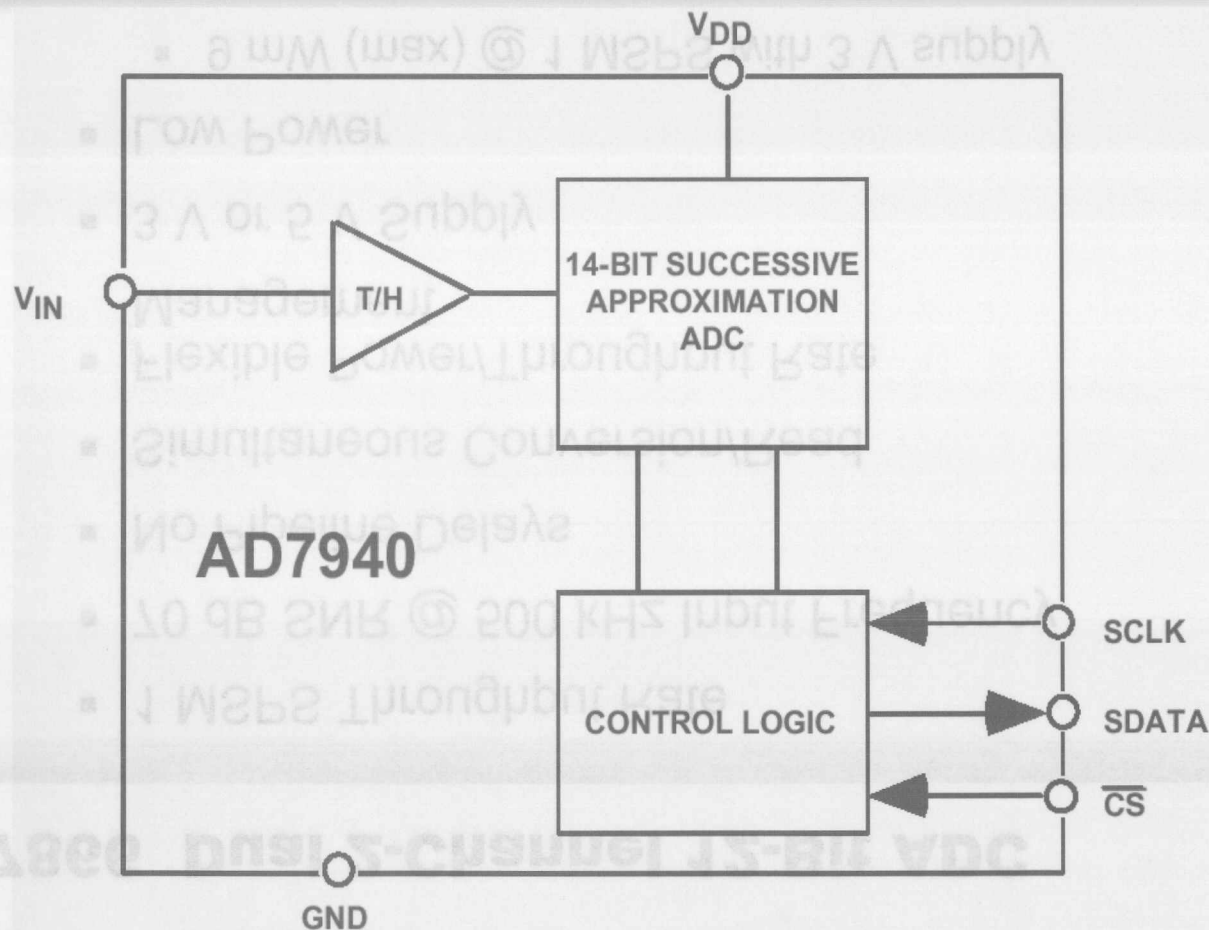
AD7866 Dual 2-Channel 12-Bit ADC



AD7866 Dual 2-Channel 12-Bit ADC

- 1 MSPS Throughput Rate
- 70 dB SNR @ 500 kHz Input Frequency
- No Pipeline Delays
- Simultaneous Conversion/Read
- Flexible Power/Throughput Rate Management
- 3 V or 5 V Supply
- Low Power
 - 9 mW (max) @ 1 MSPS with 3 V supply
 - 30 mW (max) @ 1 MSPS with 5 V supply
 - Shutdown mode 1 μ A (typ)

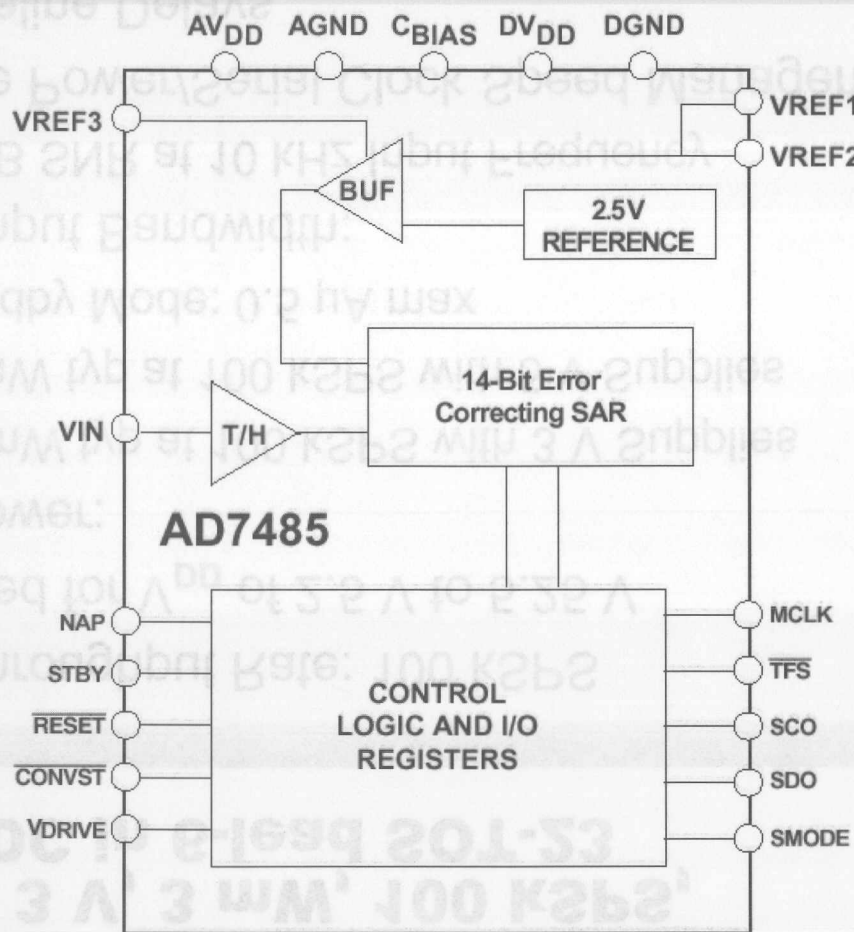
AD7940 3 V, 3 mW, 100 kSPS, 14-Bit ADC in 6-lead SOT-23



AD7940 3 V, 3 mW, 100 kSPS, 14-Bit ADC in 6-lead SOT-23

- Fast Throughput Rate: 100 kSPS
- Specified for V_{DD} of 2.5 V to 5.25 V
- Low Power:
 - 2.5 mW typ at 100 kSPS with 3 V Supplies
 - 15 mW typ at 100 kSPS with 5 V Supplies
 - Standby Mode: 0.5 μ A max
- Wide Input Bandwidth:
 - 80 dB SNR at 10 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- 6-Lead SOT-23, and 8-Lead μ SOIC Packages

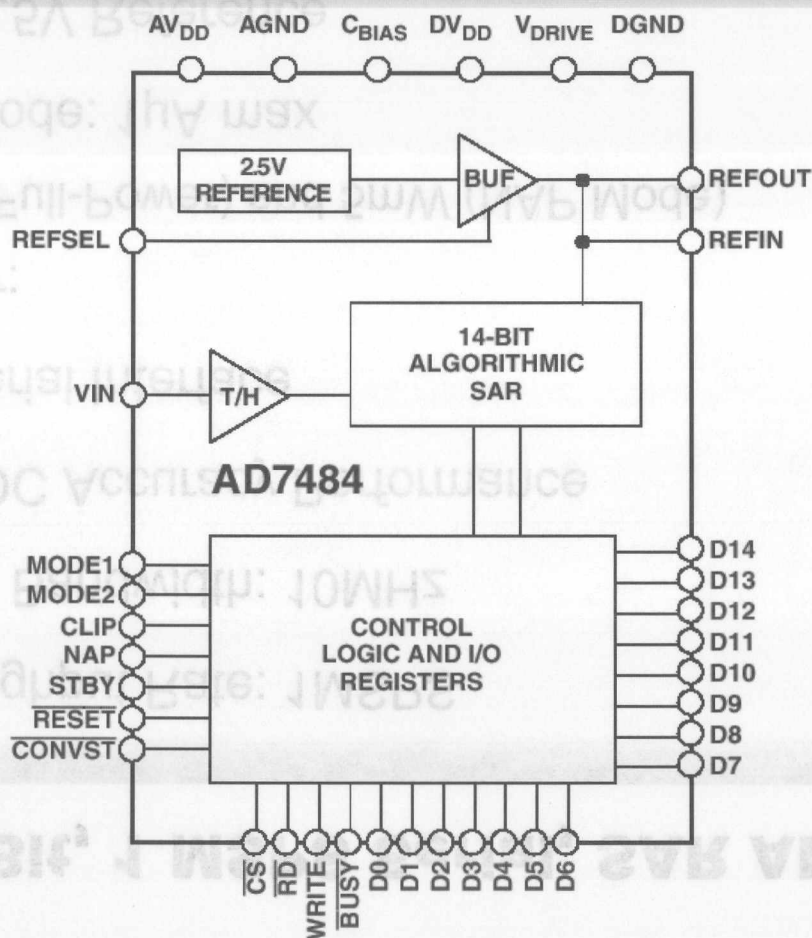
AD7485 14-Bit, 1 MSPS Serial, SAR ADC



AD7485 14-Bit, 1 MSPS Serial, SAR ADC

- Fast Throughput Rate: 1MSPS
- Wide Input Bandwidth: 10MHz
- Excellent DC Accuracy Performance
- Flexible Serial Interface
- Low Power:
 - 90mW (Full-Power) and 5mW (NAP Mode)
- Standby Mode: 1 μ A max
- Internal +2.5V Reference
- Full-Scale Overrange Indication

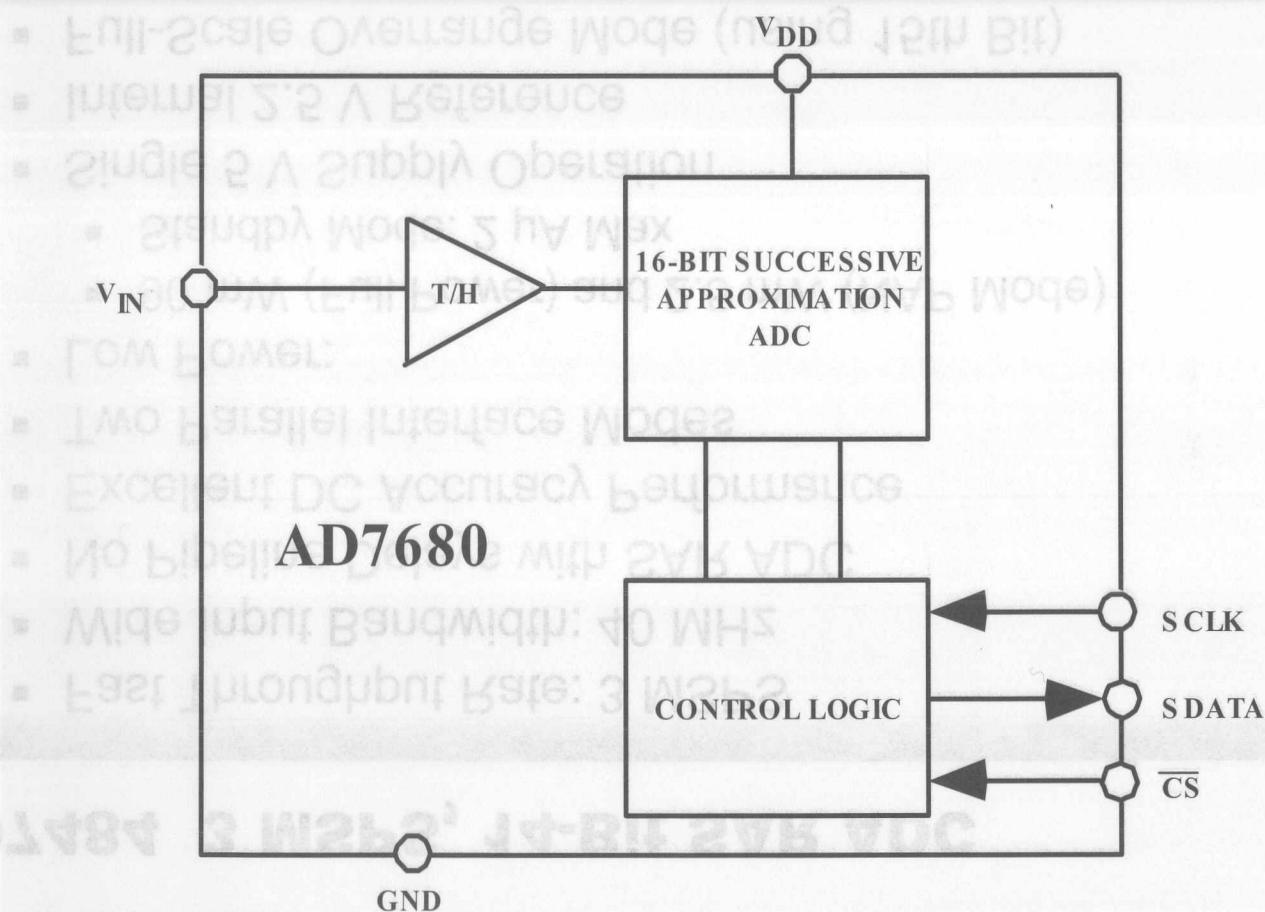
AD7484 3 MSPS, 14-Bit SAR ADC



AD7484 3 MSPS, 14-Bit SAR ADC

- Fast Throughput Rate: 3 MSPS
- Wide Input Bandwidth: 40 MHz
- No Pipeline Delays with SAR ADC
- Excellent DC Accuracy Performance
- Two Parallel Interface Modes
- Low Power:
 - 90 mW (Full Power) and 2.5 mW (NAP Mode)
 - Standby Mode: 2 μ A Max
- Single 5 V Supply Operation
- Internal 2.5 V Reference
- Full-Scale Overrange Mode (using 15th Bit)
- System Offset Removal via User Access Offset Register
- Nominal 0 V to 2.5 V Input with Shifted Range Capability
- Pin-Compatible Upgrade of 12-Bit AD7482

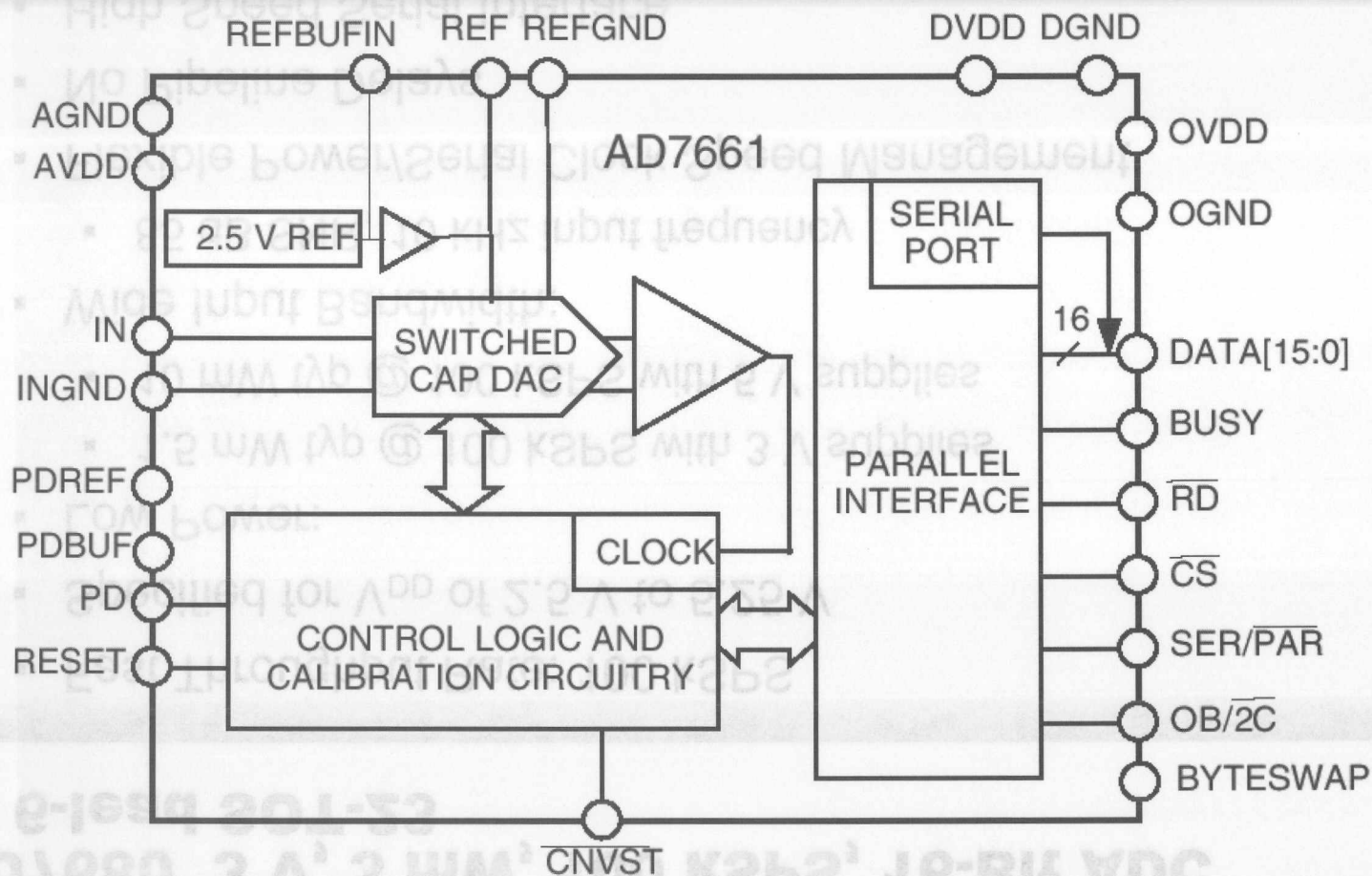
AD7680 3 V, 3 mW, 100 kSPS, 16-Bit ADC in 6-lead SOT-23



AD7680 3 V, 3 mW, 100 kSPS, 16-Bit ADC in 6-lead SOT-23

- Fast Throughput Rate: 100 kSPS
- Specified for V_{DD} of 2.5 V to 5.25 V
- Low Power:
 - 1.5 mW typ @ 100 kSPS with 3 V supplies
 - 10 mW typ @ 100 kSPS with 5 V supplies
- Wide Input Bandwidth:
 - 85 dB SNR, 10 kHz input frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Standby Mode 0.5 μ W Max
- 6-Lead SOT-23 Package, uSOIC Package

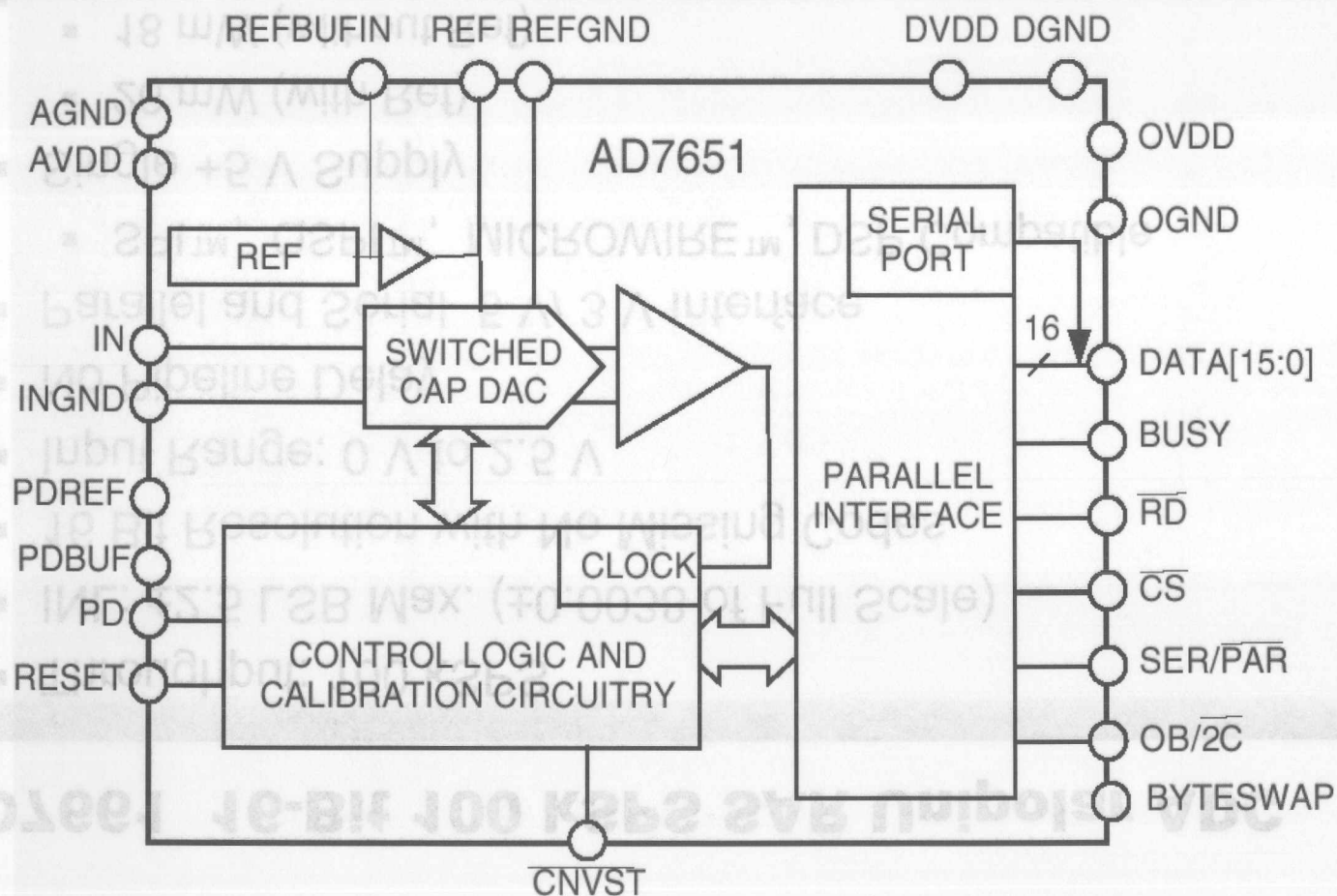
AD7661 16-Bit 100 kSPS SAR Unipolar ADC



AD7661 16-Bit 100 kSPS SAR Unipolar ADC

- Throughput: 100 kSPS
- INL: ± 2.5 LSB Max. (± 0.0038 of Full Scale)
- 16 Bit Resolution with No Missing Codes
- Input Range: 0 V to 2.5 V
- No Pipeline Delay
- Parallel and Serial 5 V/ 3 V Interface
 - SPI™, QSPI™, MICROWIRE™, DSP Compatible
- Single +5 V Supply
 - 26 mW (with Ref)
 - 18 mW (without Ref)
 - 15 μ W @ 100 SPS
 - 7 μ W in Power Down Mode
- Pin-to-Pin Compatible with PulSAR ADCs

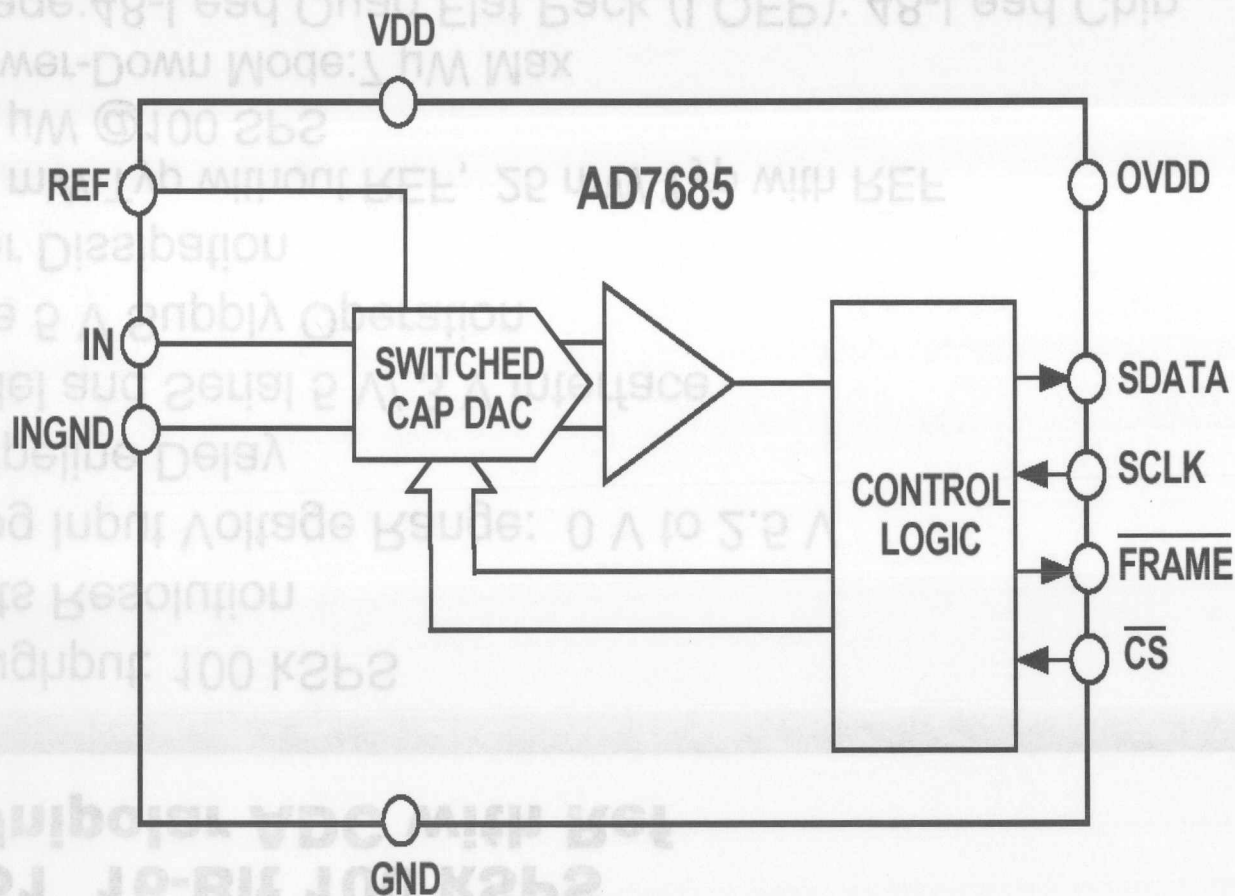
AD7651 16-Bit 100 kSPS SAR Unipolar ADC with Ref



AD7651 16-Bit 100 kSPS SAR Unipolar ADC with Ref

- Throughput: 100 kSPS
- 16-Bits Resolution
- Analog Input Voltage Range: 0 V to 2.5 V
- No Pipeline Delay
- Parallel and Serial 5 V/ 3 V Interface
- Single 5 V Supply Operation
- Power Dissipation
 - 15 mW Typ without REF, 25 mW Typ with REF
 - 15 μ W @100 SPS
 - Power-Down Mode: 7 μ W Max
- Package: 48-Lead Quad Flat Pack (LQFP); 48-Lead Chip Scale Package (LFCSP)
- Pin-to-Pin Compatible with PulSAR ADCs

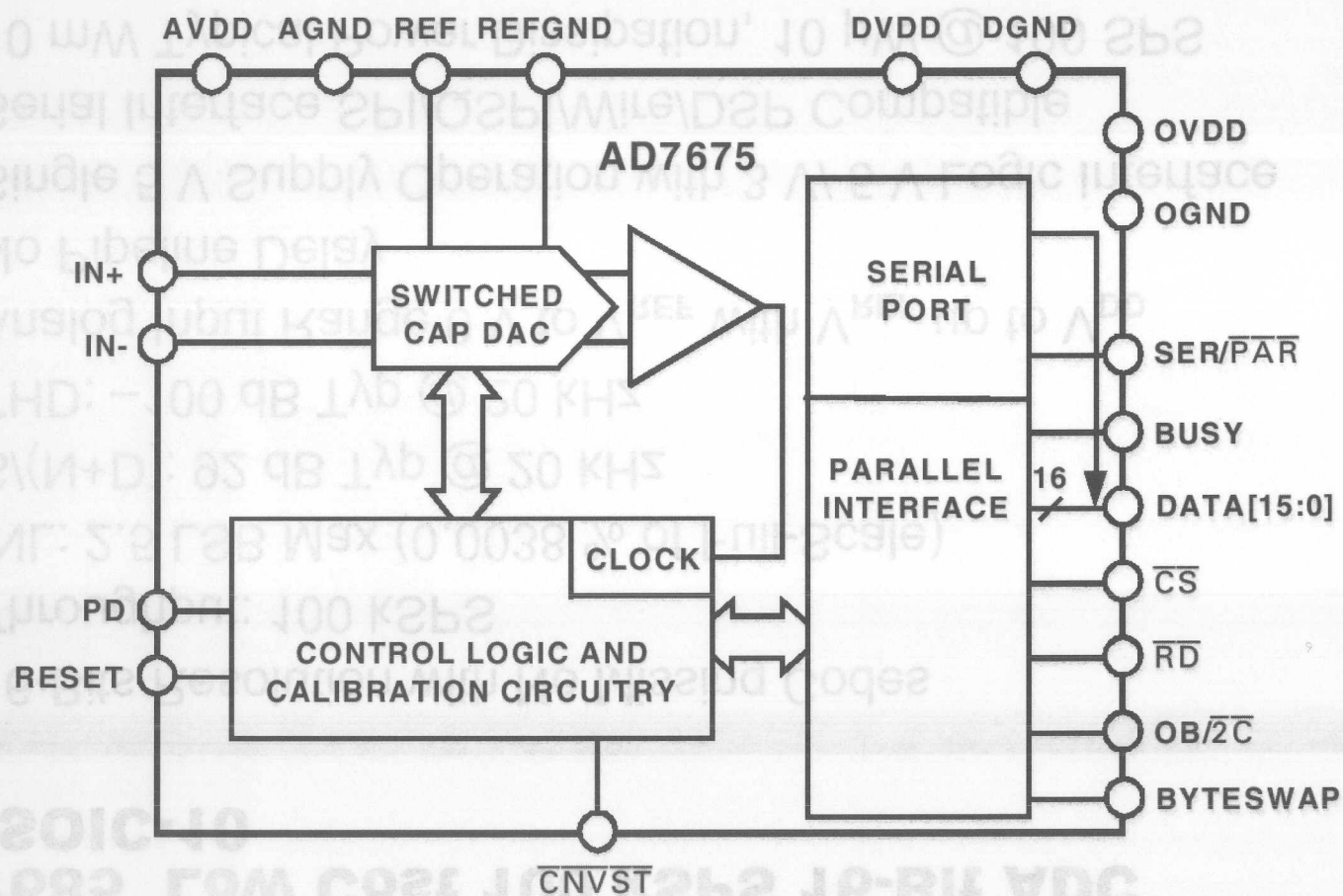
AD7685 Low Cost 100 kSPS 16-Bit ADC in μ SOIC-10



AD7685 Low Cost 100 kSPS 16-Bit ADC in μ SOIC-10

- 16-Bits Resolution with No Missing Codes
- Throughput: 100 kSPS
- INL: 2.5 LSB Max (0.0038 % of Full-Scale)
- S/(N+D): 92 dB Typ @ 20 kHz
- THD: -100 dB Typ @ 20 kHz
- Analog Input Range 0 V to V_{REF} with V_{REF} up to V_{DD}
- No Pipeline Delay
- Single 5 V Supply Operation with 3 V/ 5 V Logic Interface
- Serial Interface SPI/QSPI/Wire/DSP Compatible
- 10 mW Typical Power Dissipation, 10 μ W @ 100 SPS
 - Stand by current: 1 μ A max
- 10-Pin μ SOIC Package
- Pin-to-Pin Compatible with the AD7686

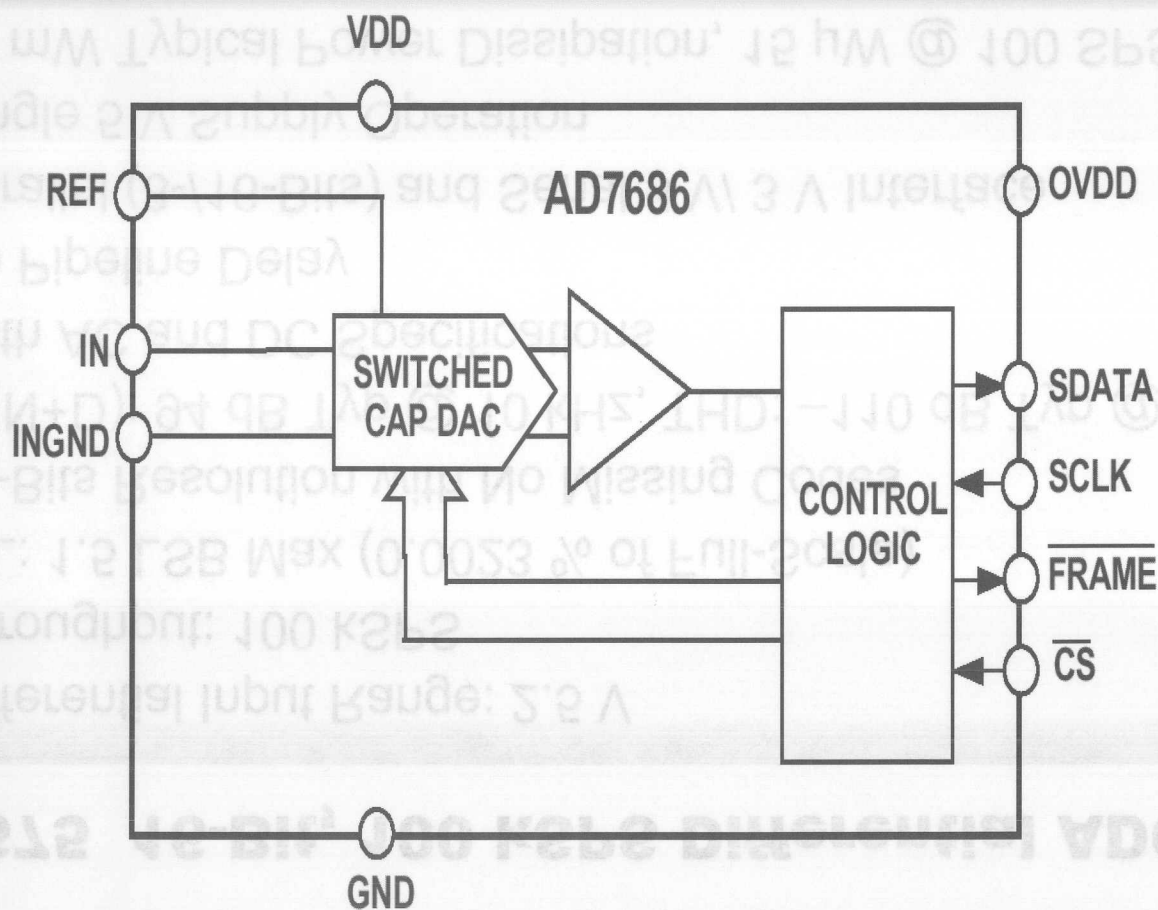
AD7675 16-Bit, 100 kSPS Differential ADC



AD7675 16-Bit, 100 kSPS Differential ADC

- Differential Input Range: 2.5 V
- Throughput: 100 kSPS
- INL: 1.5 LSB Max (0.0023 % of Full-Scale)
- 16-Bits Resolution with No Missing Codes
- S/(N+D): 94 dB Typ @ 10 kHz, THD: -110 dB Typ @ 10 kHz
- Both AC and DC Specifications
- No Pipeline Delay
- Parallel (8-/16-Bits) and Serial 5 V/ 3 V Interface
- Single 5 V Supply Operation
- 15 mW Typical Power Dissipation, 15 μ W @ 100 SPS
- Power-Down Mode: 7 μ W Max
- Package: 48-Lead Quad Flat Pack (LQFP)
- Pin-to-Pin Compatible with the AD7660

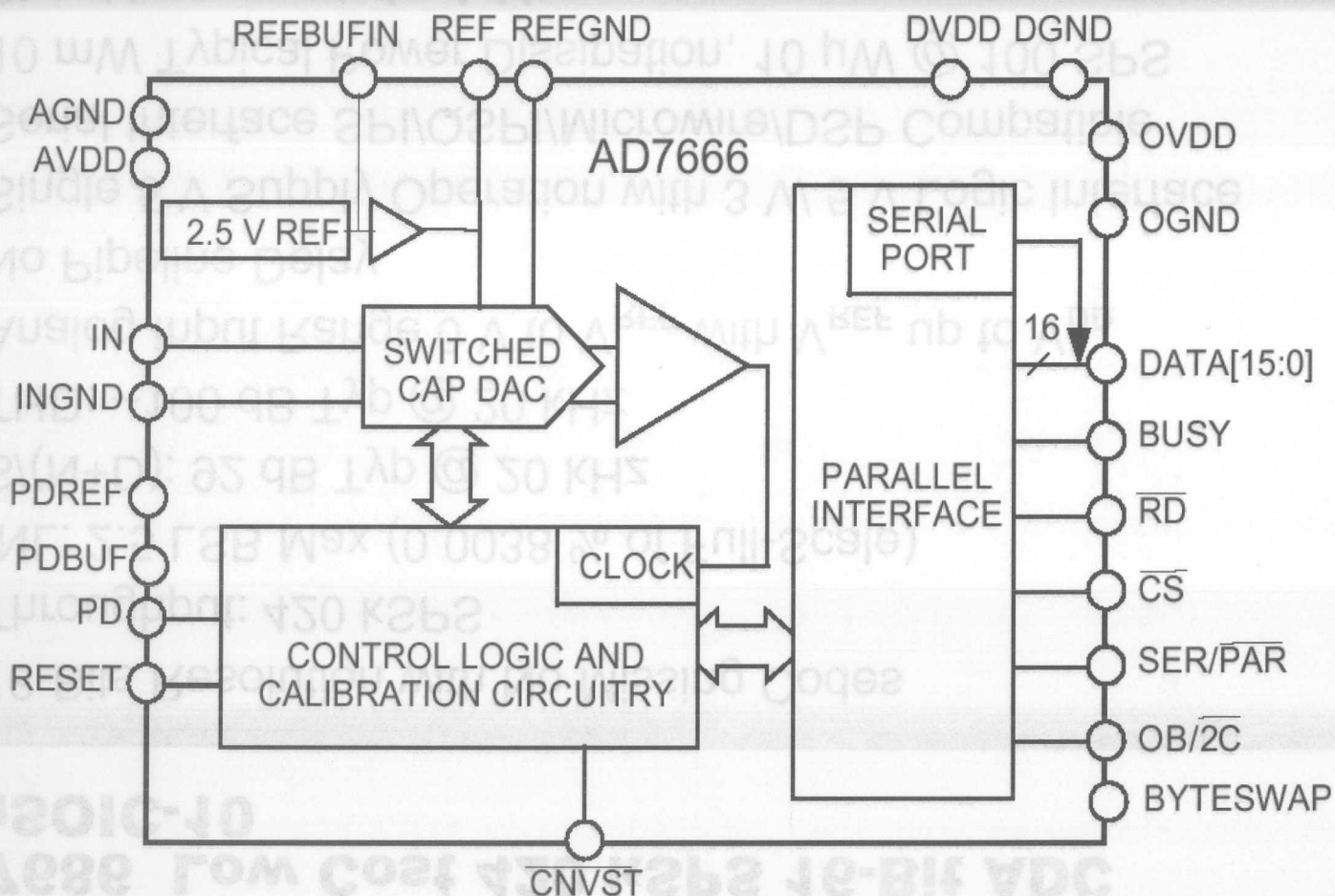
AD7686 Low Cost 420 kSPS 16-Bit ADC in μ SOIC-10



AD7686 Low Cost 420 kSPS 16-Bit ADC in μ SOIC-10

- 16-Bits Resolution with No Missing Codes
- Throughput: 420 kSPS
- INL: 2.5 LSB Max (0.0038 % of Full-Scale)
- S/(N+D): 92 dB Typ @ 20 kHz
- THD: -100 dB Typ @ 20 kHz
- Analog Input Range 0 V to V_{REF} with V_{REF} up to V_{DD}
- No Pipeline Delay
- Single 5 V Supply Operation with 3 V/ 5 V Logic Interface
- Serial Interface SPI/QSPI/Microwire/DSP Compatible
- 10 mW Typical Power Dissipation, 10 μ W @ 100 SPS
- Stand by current: 1 μ A Max
- 10-Pin μ SOIC Package
- Pin-to-Pin Compatible Upgrade of the AD7685

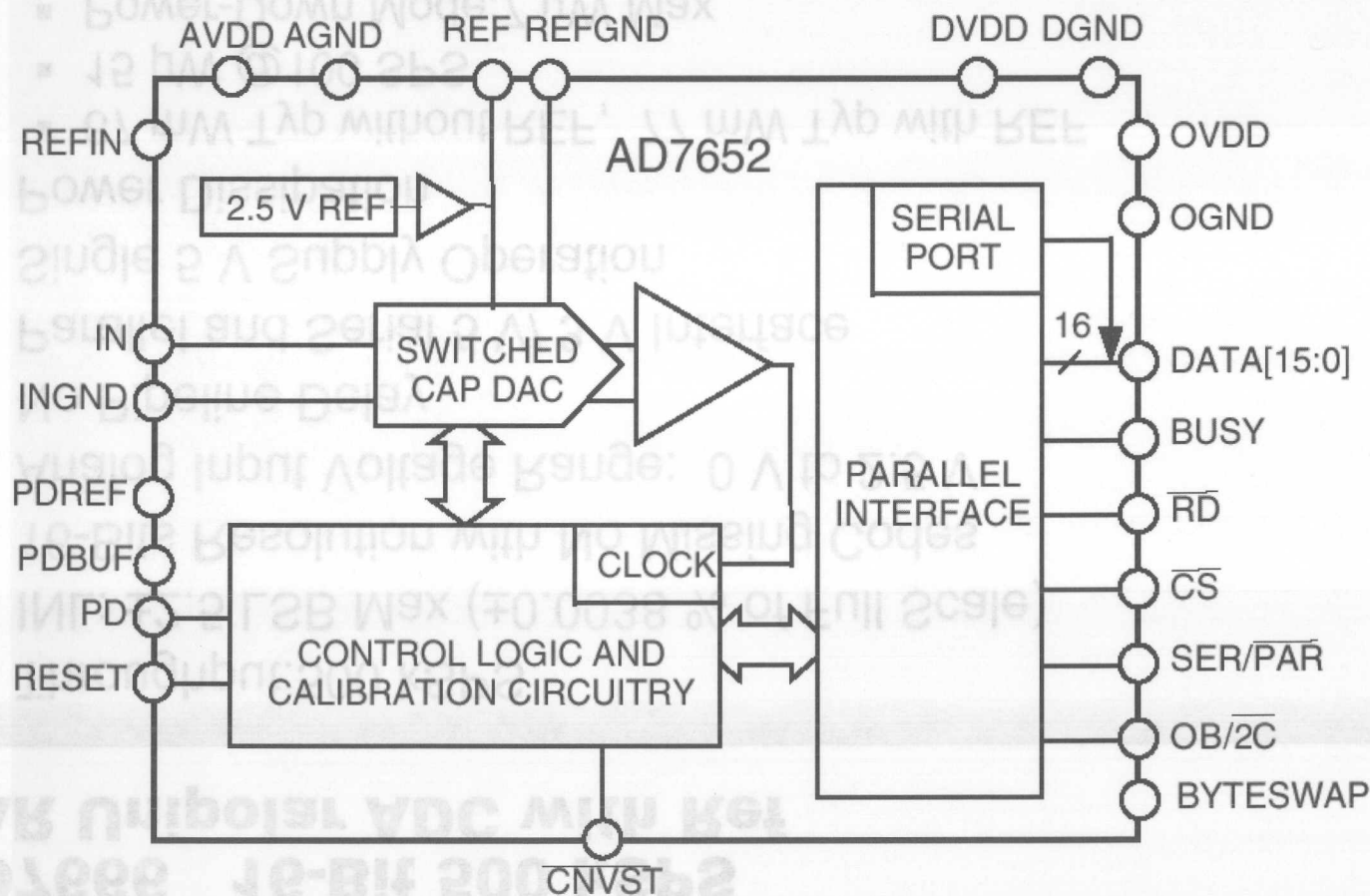
AD7666 16-Bit 500 kSPS SAR Unipolar ADC with Ref



AD7666 16-Bit 500 kSPS SAR Unipolar ADC with Ref

- Throughput: 500 kSPS
- INL: ± 2.5 LSB Max (± 0.0038 % of Full Scale)
- 16-Bits Resolution with No Missing Codes
- Analog Input Voltage Range: 0 V to 2.5 V
- No Pipeline Delay
- Parallel and Serial 5 V/ 3 V Interface
- Single 5 V Supply Operation
- Power Dissipation
 - 67 mW Typ without REF, 77 mW Typ with REF
 - 15 μ W @100 SPS
 - Power-Down Mode: 7 μ W Max
- Package: 48-Lead Quad Flat Pack (LQFP); 48-Lead Chip Scale Package (LFCSP)
- Pin-to-Pin Compatible with PulSAR ADCs

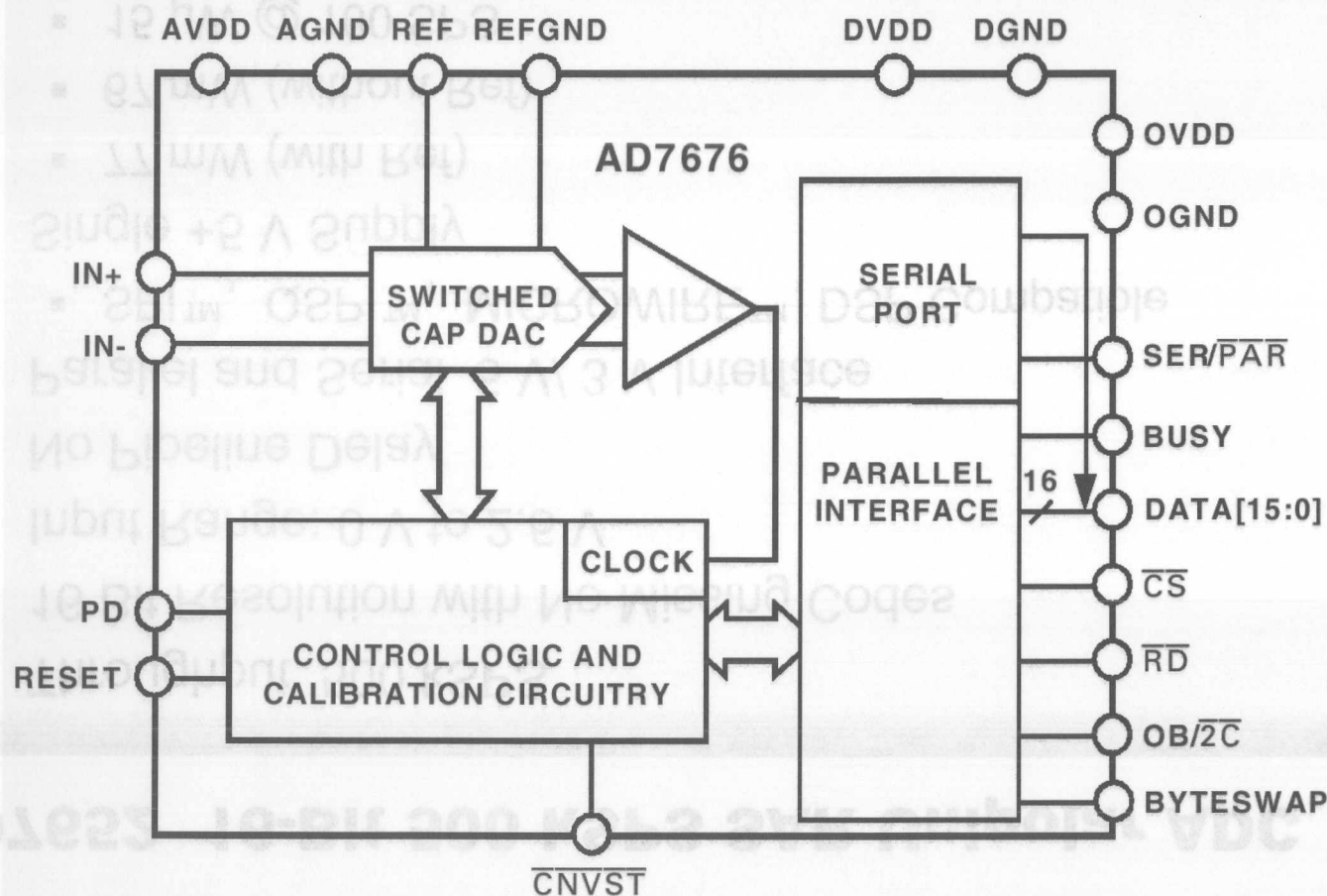
AD7652 16-Bit 500 kSPS SAR Unipolar ADC



AD7652 16-Bit 500 kSPS SAR Unipolar ADC

- Throughput: 500 kSPS
- 16 Bit Resolution with No Missing Codes
- Input Range: 0 V to 2.5 V
- No Pipeline Delay
- Parallel and Serial 5 V/ 3 V Interface
 - SPI™, QSPI™, MICROWIRE™, DSP Compatible
- Single +5 V Supply
 - 77 mW (with Ref)
 - 67 mW (without Ref)
 - 15 μ W @ 100 SPS
 - 7 μ W in Power Down Mode
- Pin-to-Pin Compatible with PulSAR ADCs

AD7676 16-Bit, 500 kSPS, 1 LSB INL, Differential ADC

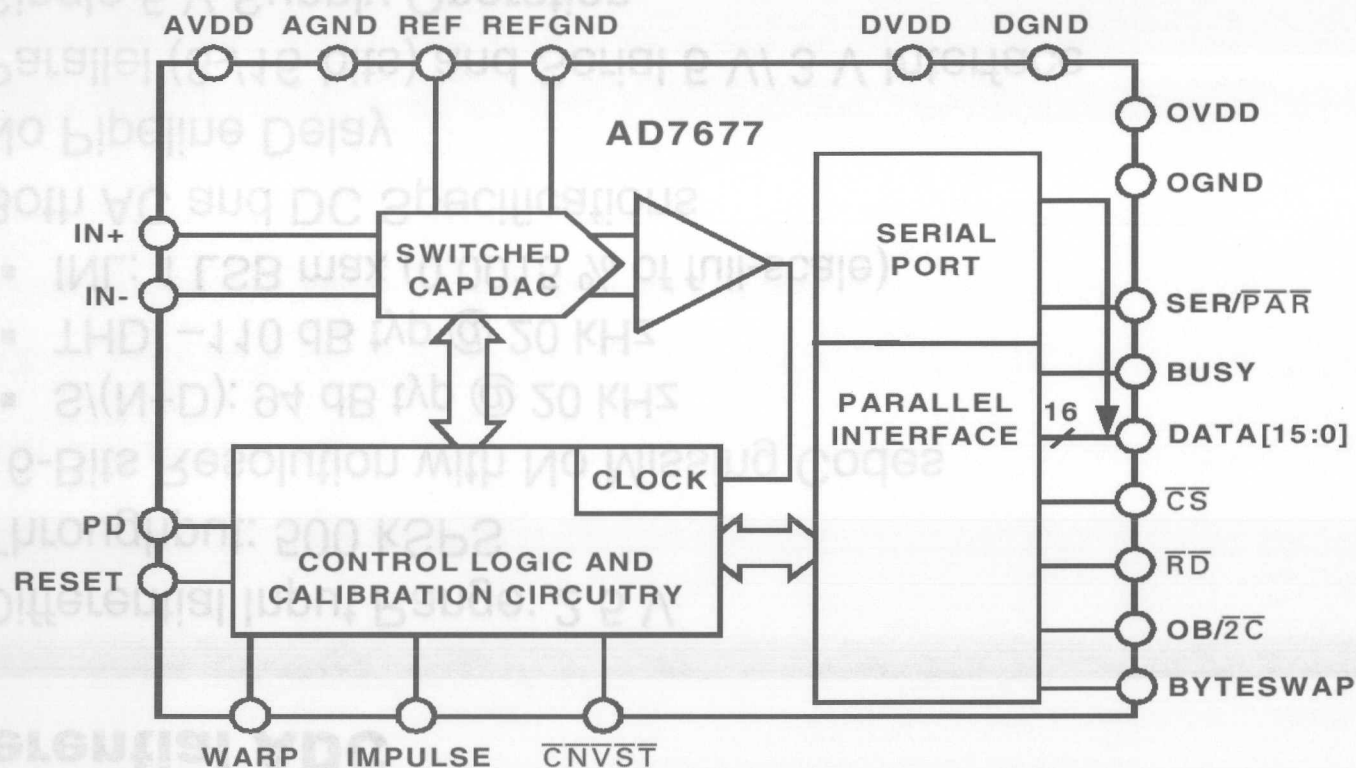


AD7676 16-Bit, 500 kSPS, 1 LSB INL, Differential ADC

- Differential Input Range: 2.5 V
- Throughput: 500 kSPS
- 16-Bits Resolution with No Missing Codes
 - S/(N+D): 94 dB typ @ 20 kHz
 - THD: -110 dB typ @ 20 kHz
 - INL: 1 LSB max (0.0015 % of full-scale)
- Both AC and DC Specifications
- No Pipeline Delay
- Parallel (8-/16-bits) and Serial 5 V/ 3 V Interface
- Single 5 V Supply Operation
 - 60 mW typical power dissipation, 12 μ W @ 100 SPS
 - Power-down mode: 7 μ W max
- Package: 48-Lead Quad Flat Pack (LQFP)
- Pin-to-Pin Compatible Upgrade of the AD7675

AD7677 16-Bit, 1 MSPS, 1 LSB INL, Differential ADC

- Pin-to-Pin Compatible Upgrade of the AD7674/AD7675/AD7676

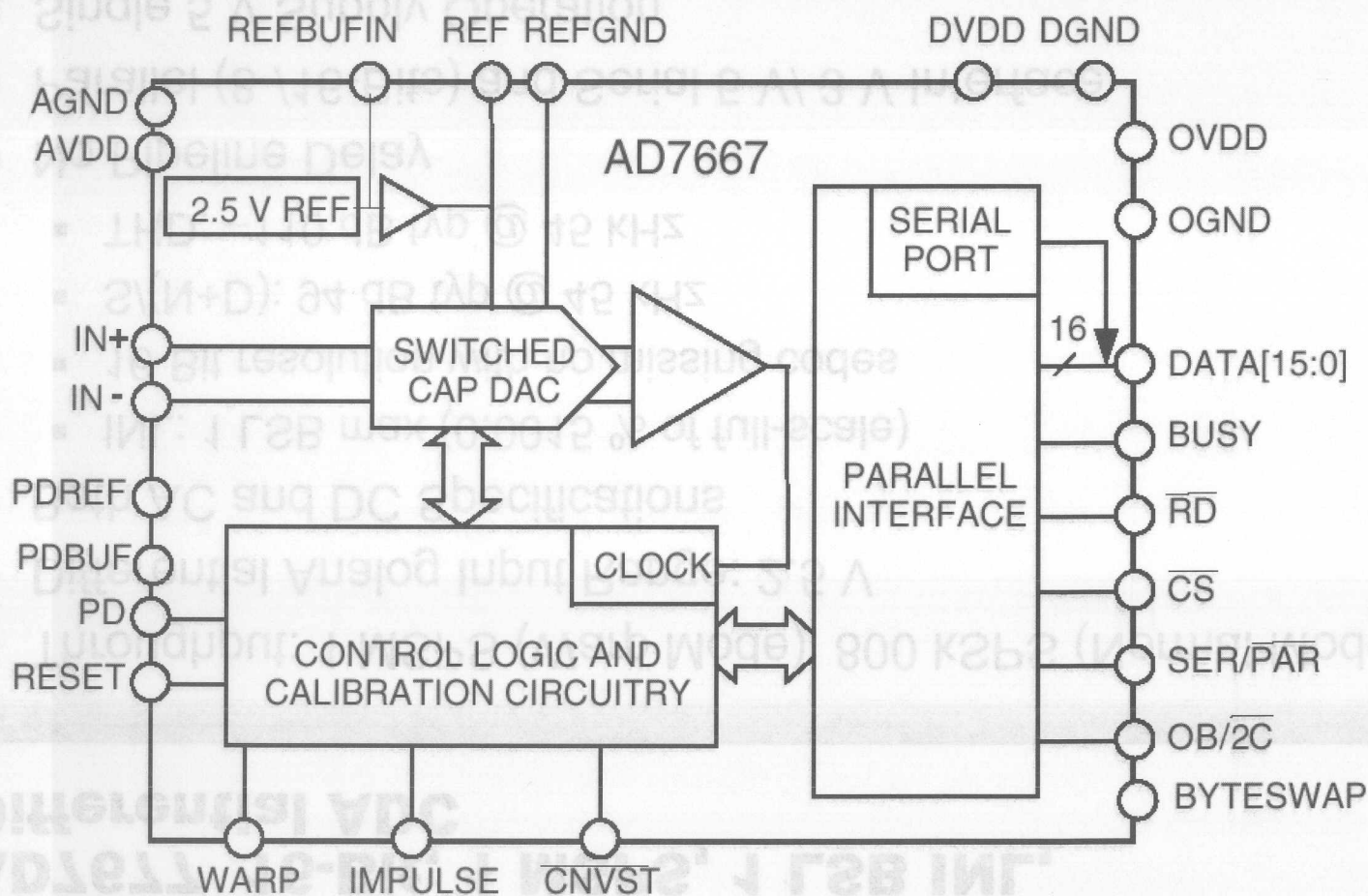


Package: 48-Lead Quad Flat Pack (LQFP)

AD7677 16-Bit, 1 MSPS, 1 LSB INL, Differential ADC

- Throughput: 1 MSPS (Warp Mode); 800 kSPS (Normal Mode)
- Differential Analog Input Range: 2.5 V
- Both AC and DC Specifications
 - INL: 1 LSB max (0.0015 % of full-scale)
 - 16-Bit resolution with no missing codes
 - S/(N+D): 94 dB typ @ 45 kHz
 - THD: -110 dB typ @ 45 kHz
- No Pipeline Delay
- Parallel (8-/16-Bits) and Serial 5 V/ 3 V Interface
- Single 5 V Supply Operation
 - 120 mW typical, 15 μ W @ 100 SPS
 - Power-down mode: 7 μ W max

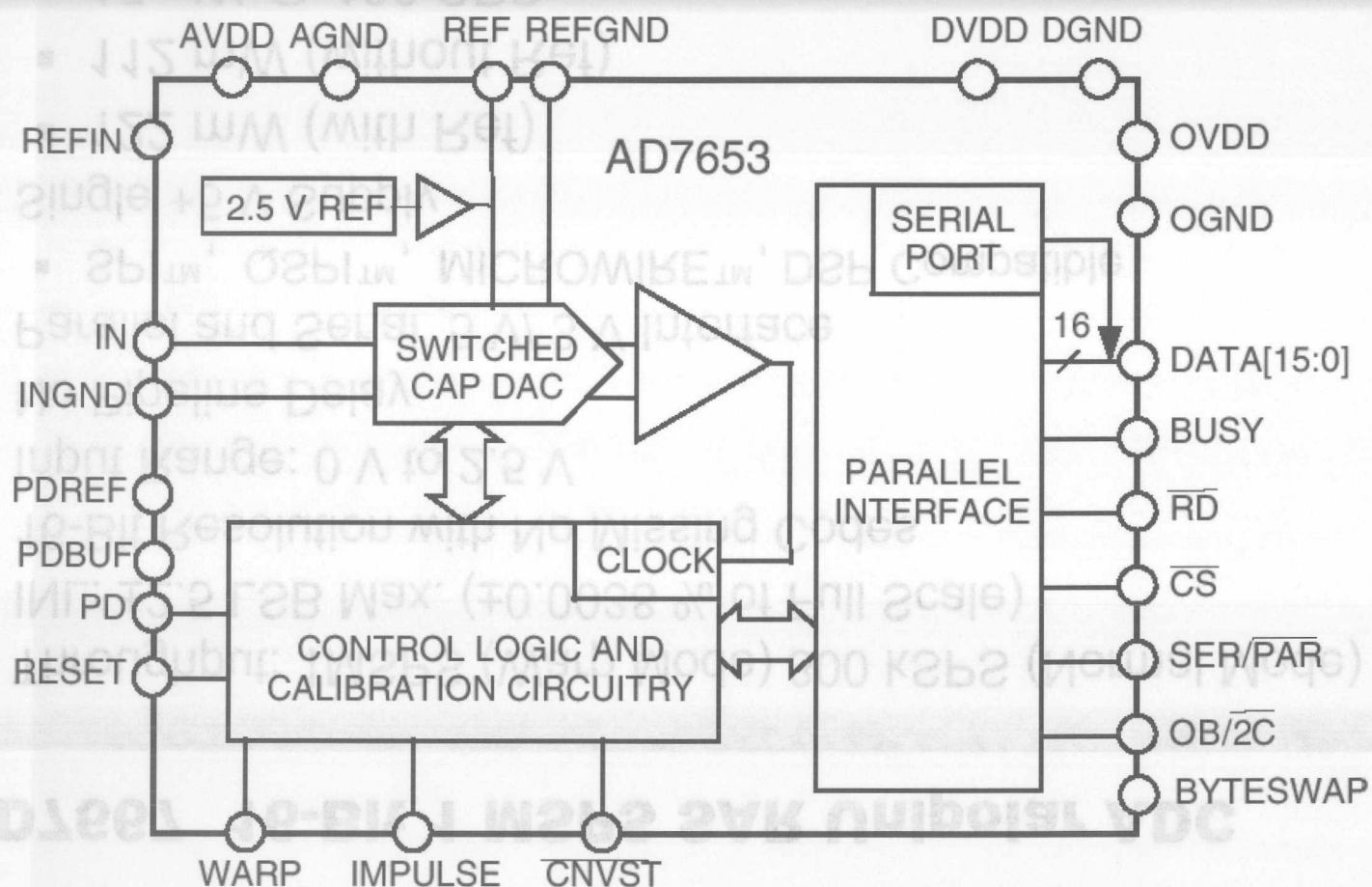
AD7667 16-Bit 1 MSPS SAR Unipolar ADC



AD7667 16-Bit 1 MSPS SAR Unipolar ADC

- Throughput: 1MSPS (Warp Mode) 800 kSPS (Normal Mode)
- INL: ± 2.5 LSB Max. (± 0.0038 % of Full Scale)
- 16-Bit Resolution with No Missing Codes
- Input Range: 0 V to 2.5 V
- No Pipeline Delay
- Parallel and Serial 5 V/ 3 V Interface
 - SPI™, QSPI™, MICROWIRE™, DSP Compatible
- Single +5 V Supply
 - 122 mW (with Ref)
 - 112 mW (without Ref)
 - 15 μ W @ 100 SPS
 - 7 μ W in Power Down Mode
- Pin-to-Pin Compatible with PulSAR ADCs

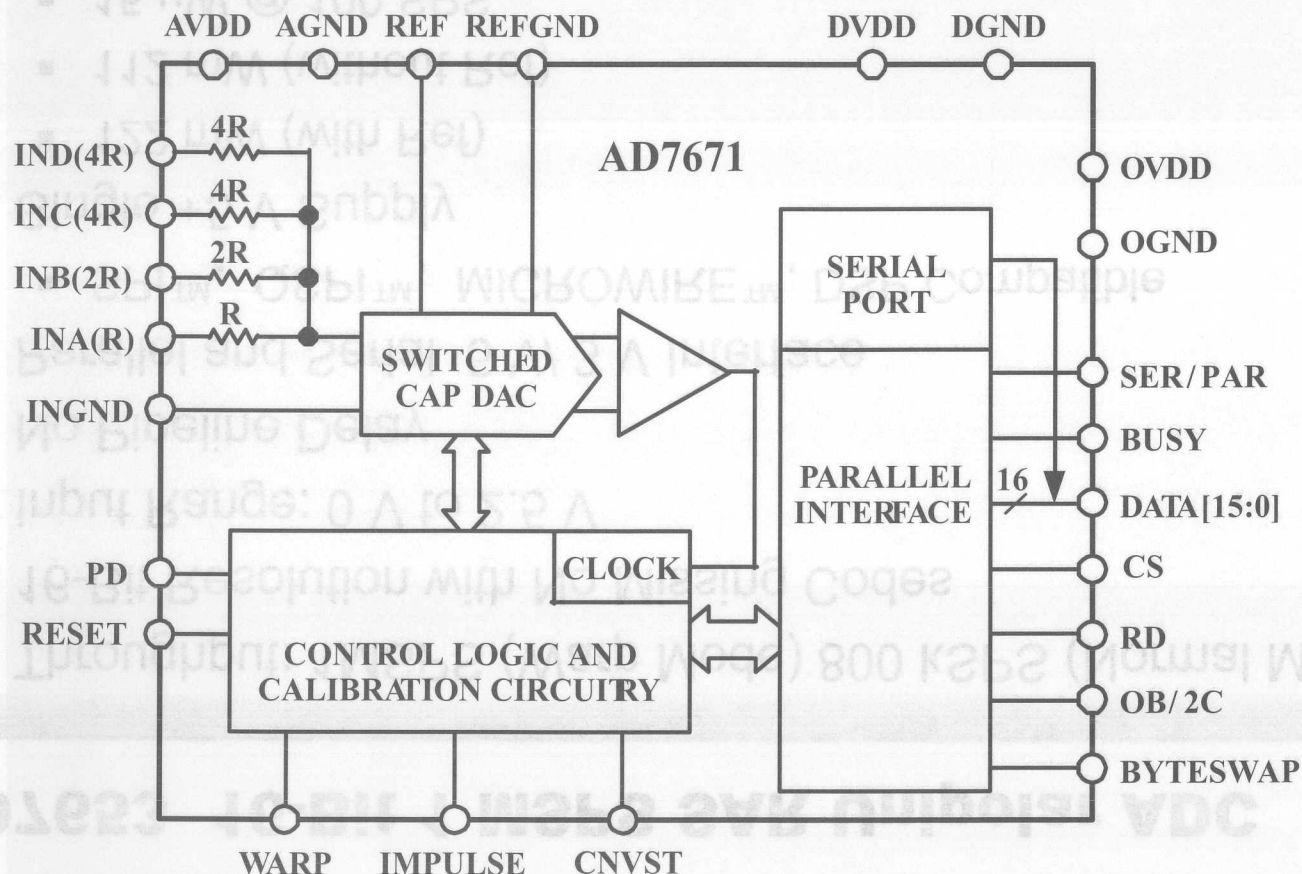
AD7653 16-Bit 1 MSPS SAR Unipolar ADC



AD7653 16-Bit 1 MSPS SAR Unipolar ADC

- Throughput: 1MSPS (Warp Mode) 800 kSPS (Normal Mode)
- 16-Bit Resolution with No Missing Codes
- Input Range: 0 V to 2.5 V
- No Pipeline Delay
- Parallel and Serial 5 V/ 3 V Interface
 - SPI™, QSPI™, MICROWIRE™, DSP Compatible
- Single +5 V Supply
 - 122 mW (with Ref)
 - 112 mW (without Ref)
 - 15 μ W @ 100 SPS
 - 7 μ W in Power Down Mode
- Pin-to-Pin Compatible with PulSAR ADCs

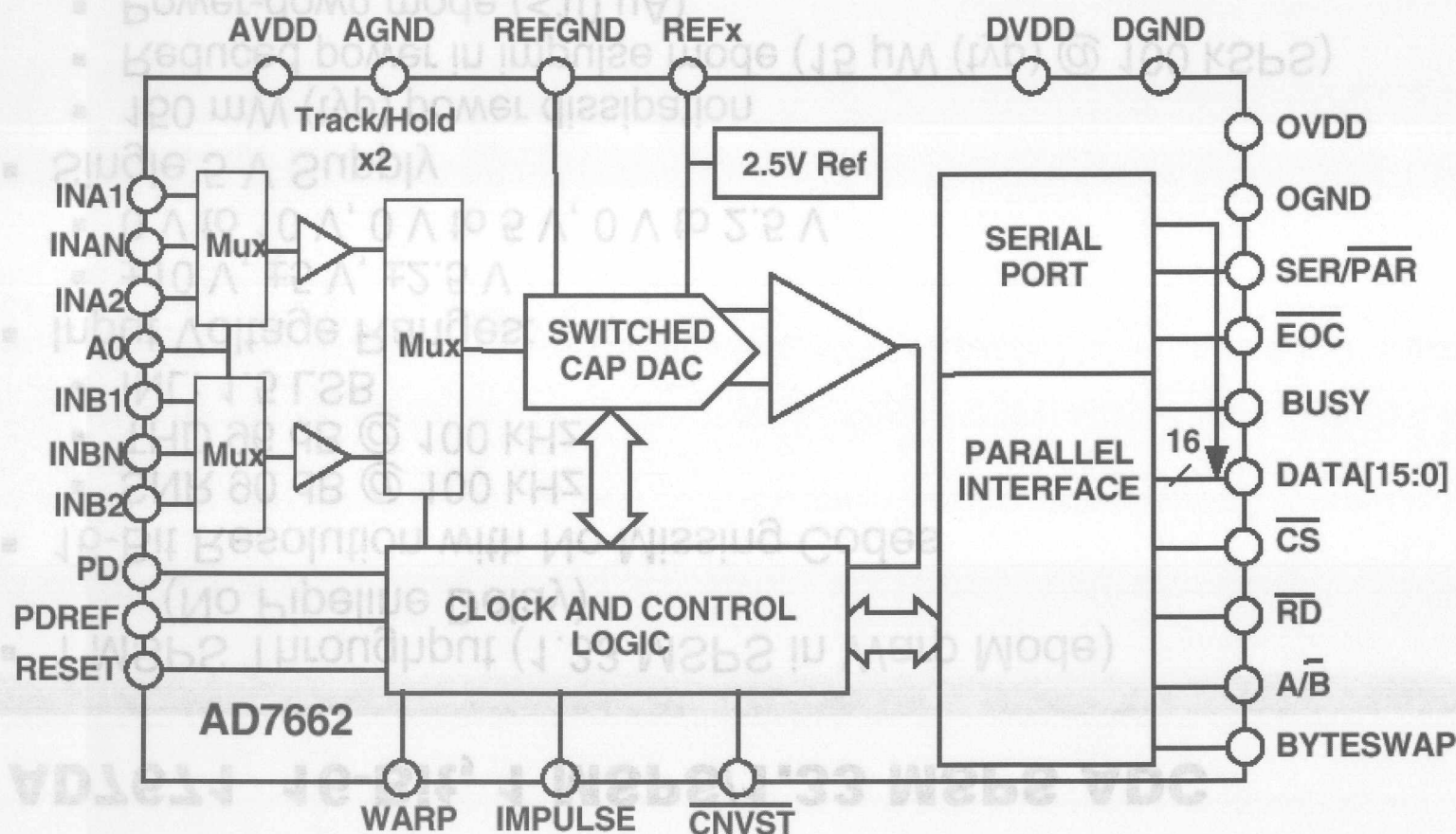
AD7671 16-Bit, 1 MSPS/1.33 MSPS ADC



AD7671 16-Bit, 1 MSPS/1.33 MSPS ADC

- 1 MSPS Throughput (1.33 MSPS in Warp Mode)
(No Pipeline Delay)
- 16-Bit Resolution with No Missing Codes
 - SNR 90 dB @ 100 kHz
 - THD 96 dB @ 100 kHz
 - INL: 1.5 LSB
- Input Voltage Ranges:
 - ± 10 V, ± 5 V, ± 2.5 V
 - 0 V to 10 V, 0 V to 5 V, 0 V to 2.5 V
- Single 5 V Supply
 - 150 mW (typ) power dissipation
 - Reduced power in impulse mode (15 μ W (typ) @ 100 kSPS)
 - Power-down mode (<10 μ A)
- Parallel and Serial (3 V/ 5 V) Interfaces
(Separate Output Power Pin)
- 48-Lead Thin Quad Flat Pack (TQFP)

AD7662 Dual 2-Channel 500 kSPS Simultaneous Sampling SAR 16-Bit ADC



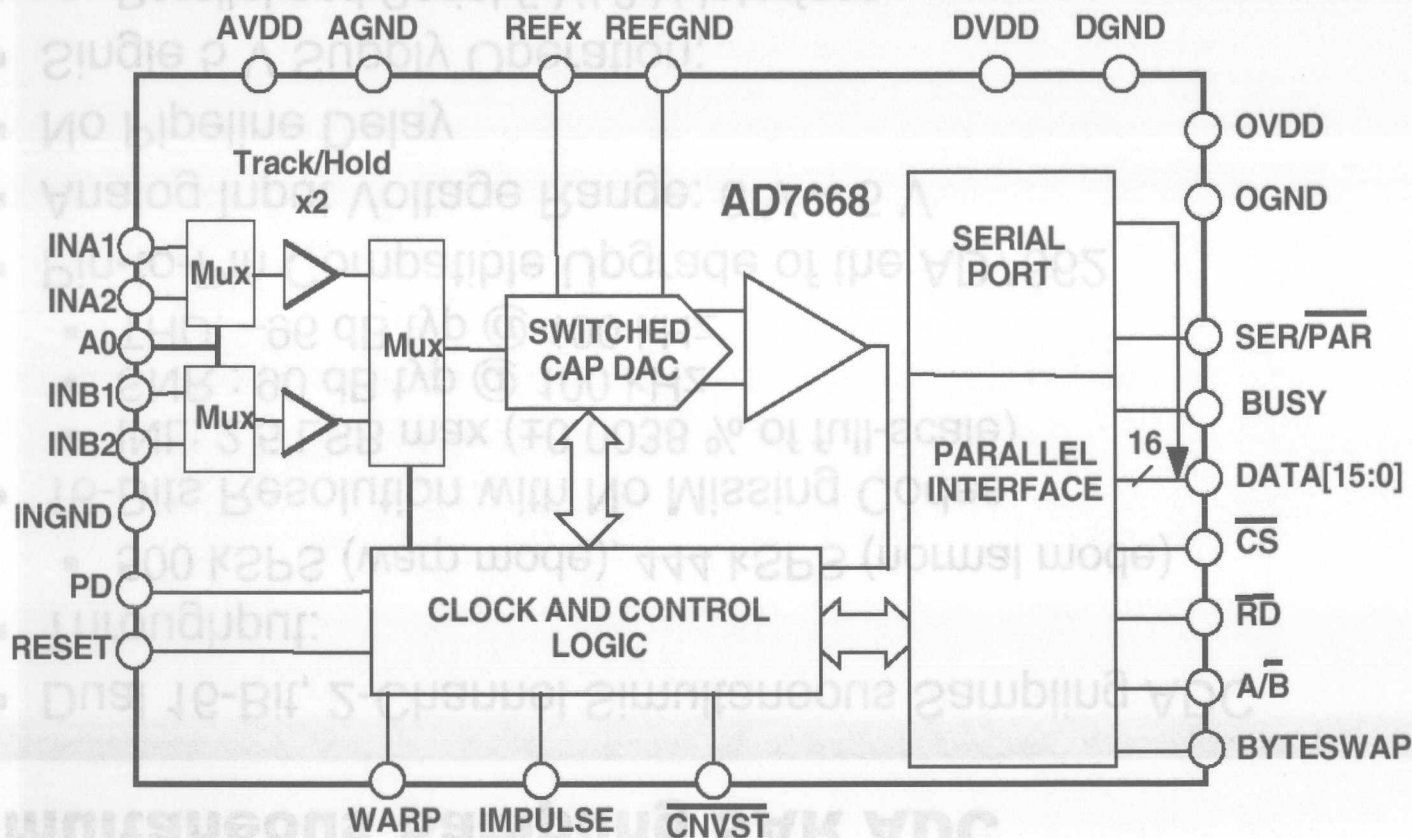
AD7662 Dual 2-Channel 500 kSPS Simultaneous Sampling SAR 16-Bit ADC

- Dual 16-Bit 2-channel Simultaneous Sampling ADC
- Throughput: 500 kSPS (Warp Mode) 444 kSPS (Normal Mode)
- INL: 6 LSB Max (± 0.0092 % of Full-Scale)
- 16-Bits Resolution with No Missing Codes
- SNR : 90 dB Typ @ 100 kHz
- THD: -92 dB Typ @ 100 kHz
- Analog Input Voltage Range: 0 V to 5 V
- Choice of Internal or External Reference
- No Pipeline Delay

AD7662 Dual 2-Channel 500 kSPS Simultaneous Sampling SAR 16-Bit ADC

- Parallel and Serial 5 V/ 3 V Interface
 - SPI™/ QSPI™/ MICROWIRE™/ DSP Compatible
- Single 5 V Supply Operation
- Power Dissipation
 - 120 mW Typical,
 - 15 W @ 100 SPS
 - 7 W Max Power-Down Mode
- Pin-to-Pin compatible with the AD7668
- Low Cost

AD7668 Dual 2-Channel 16-Bit 500 kSPS Simultaneous Sampling SAR ADC

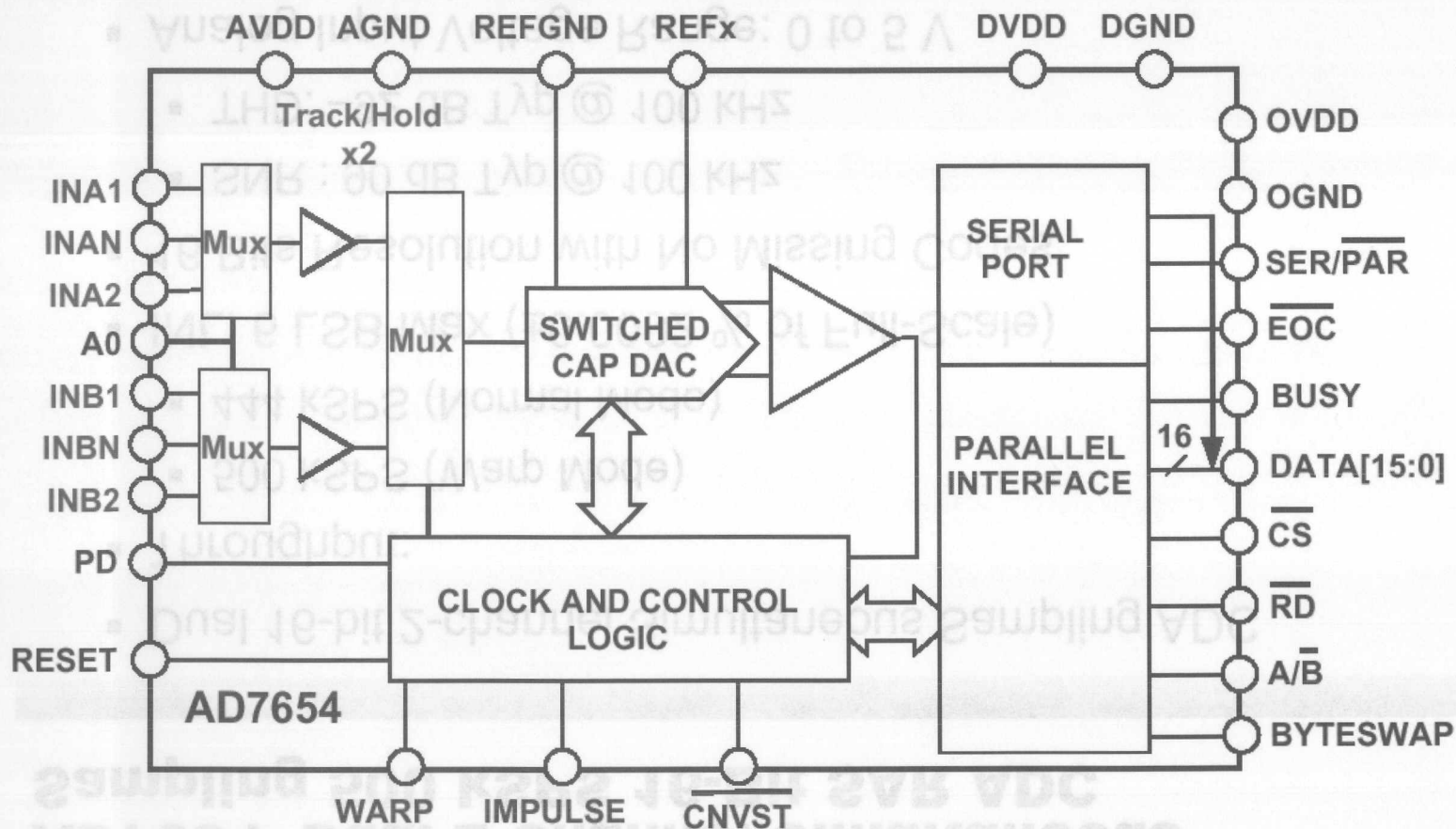


■ Package: 48-Lead Quad Flat Pack (LQFP)

AD7668 Dual 2-Channel 16-Bit 500 kSPS Simultaneous Sampling SAR ADC

- Dual 16-Bit, 2-Channel Simultaneous Sampling ADC
- Throughput:
 - 500 kSPS (warp mode), 444 kSPS (normal mode)
- 16-Bits Resolution with No Missing Codes
 - INL: 2.5 LSB max (± 0.0038 % of full-scale)
 - SNR : 90 dB typ @ 100 kHz
 - THD: -96 dB typ @ 100 kHz
- Pin-to-Pin Compatible Upgrade of the AD7662
- Analog Input Voltage Range: 0 V – 5 V
- No Pipeline Delay
- Single 5 V Supply Operation;
 - Parallel and Serial 5 V/ 3 V Interface
- Power Dissipation
 - 120 mW typical, 15 μ W @ 100 SPS
 - Power-down mode: 7 μ W max

AD7654 Dual 2-Channel Simultaneous Sampling 500 kSPS 16-Bit SAR ADC



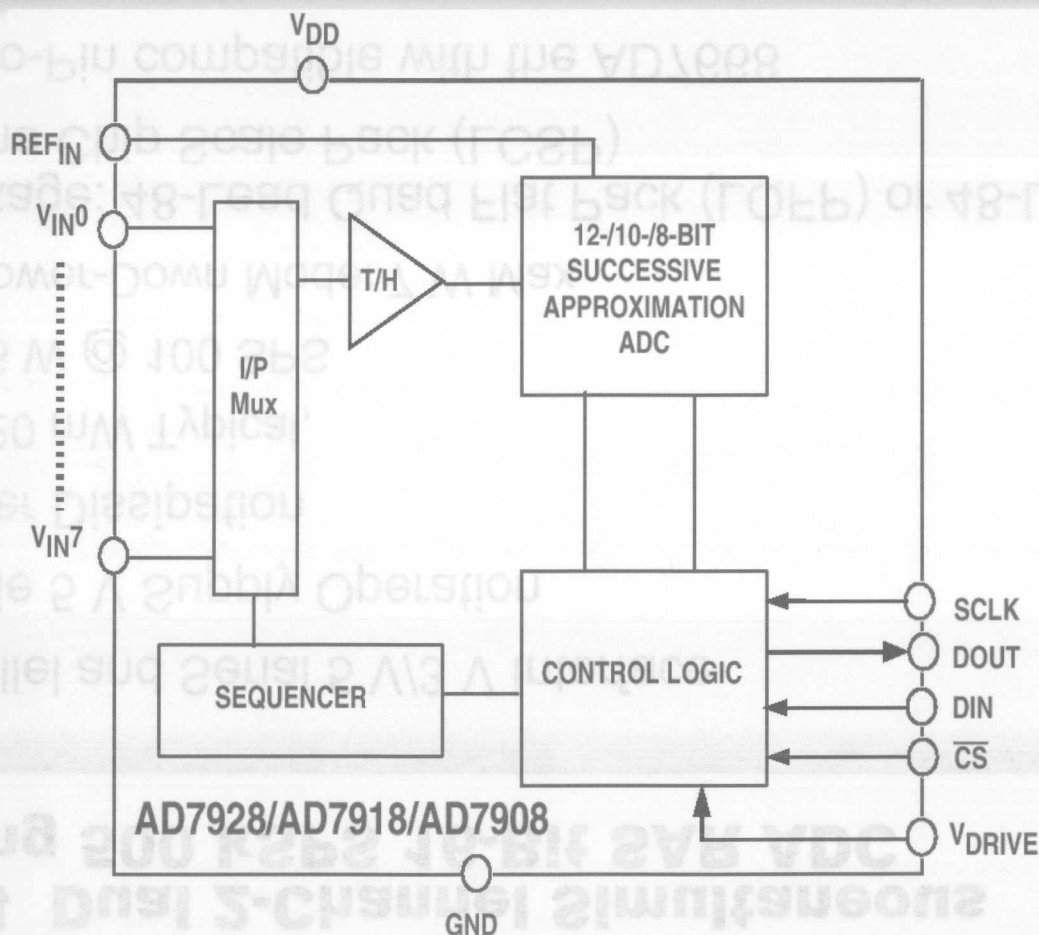
AD7654 Dual 2-Channel Simultaneous Sampling 500 kSPS 16-Bit SAR ADC

- Dual 16-bit 2-channel Simultaneous Sampling ADC
- Throughput:
 - 500 kSPS (Warp Mode)
 - 444 kSPS (Normal Mode)
- INL: 6 LSB Max ($\pm 0.0092\%$ of Full-Scale)
- 16 Bits Resolution with No Missing Codes
 - SNR : 90 dB Typ @ 100 kHz
 - THD: -92 dB Typ @ 100 kHz
- Analog Input Voltage Range: 0 to 5 V
- Choice of Internal or External Reference
- No Pipeline Delay

AD7654 Dual 2-Channel Simultaneous Sampling 500 kSPS 16-Bit SAR ADC

- Parallel and Serial 5 V/3 V Interface
- Single 5 V Supply Operation
- Power Dissipation
 - 120 mW Typical,
 - 15 W @ 100 SPS
 - Power-Down Mode: 7 W Max
- Package: 48-Lead Quad Flat Pack (LQFP) or 48-Lead Frame Chip Scale Pack (LCSP)
- Pin-to-Pin compatible with the AD7668
- Low Cost

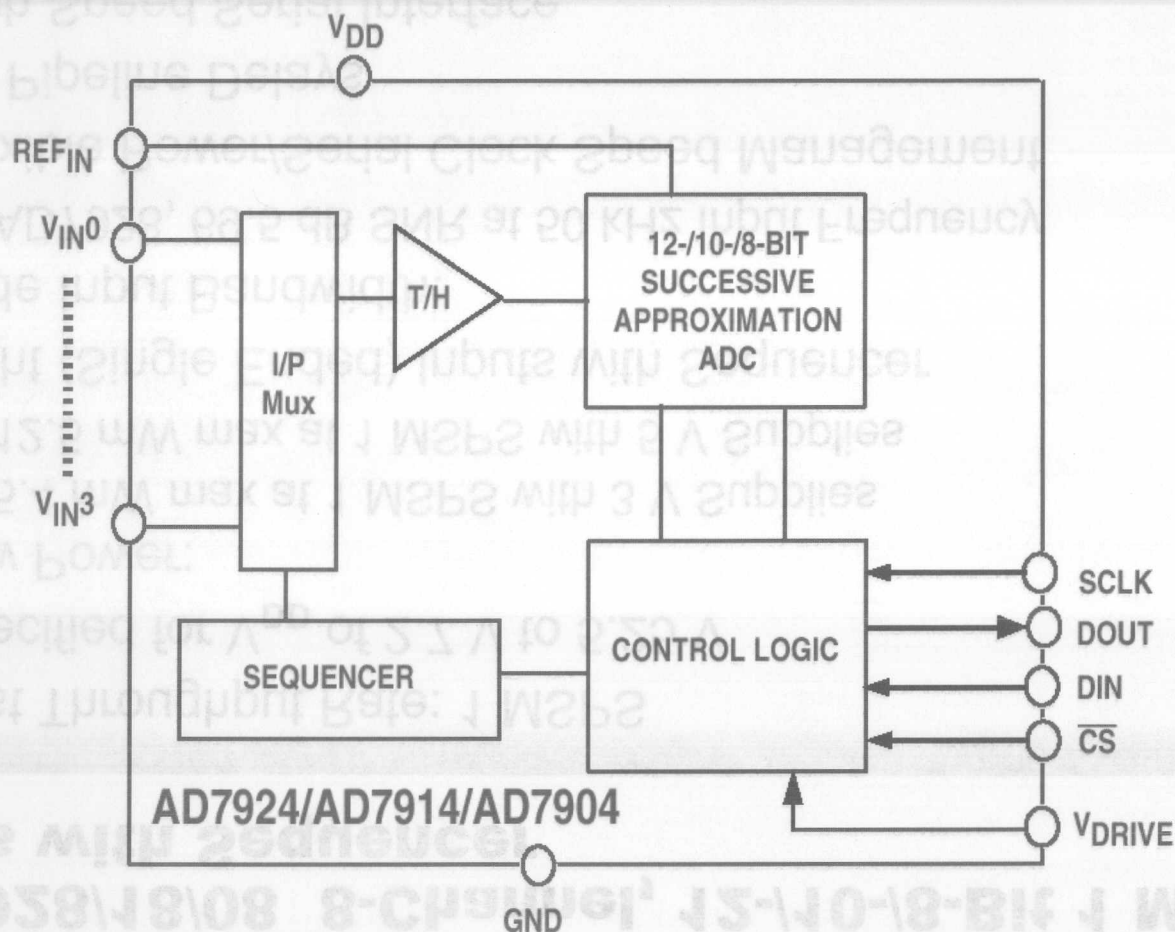
AD7928/18/08 8-Channel, 12-/10-/8-Bit 1 MSPS, ADCs with Sequencer



AD7928/18/08 8-Channel, 12-/10-/8-Bit 1 MSPS, ADCs with Sequencer

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power:
 - 5.4 mW max at 1 MSPS with 3 V Supplies
 - 12.5 mW max at 1 MSPS with 5 V Supplies
- Eight (Single Ended) Inputs with Sequencer
- Wide Input Bandwidth:
 - AD7928, 69.5 dB SNR at 50 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Shutdown Mode: 0.5 μ A max
- 20-Pin TSSOP Package

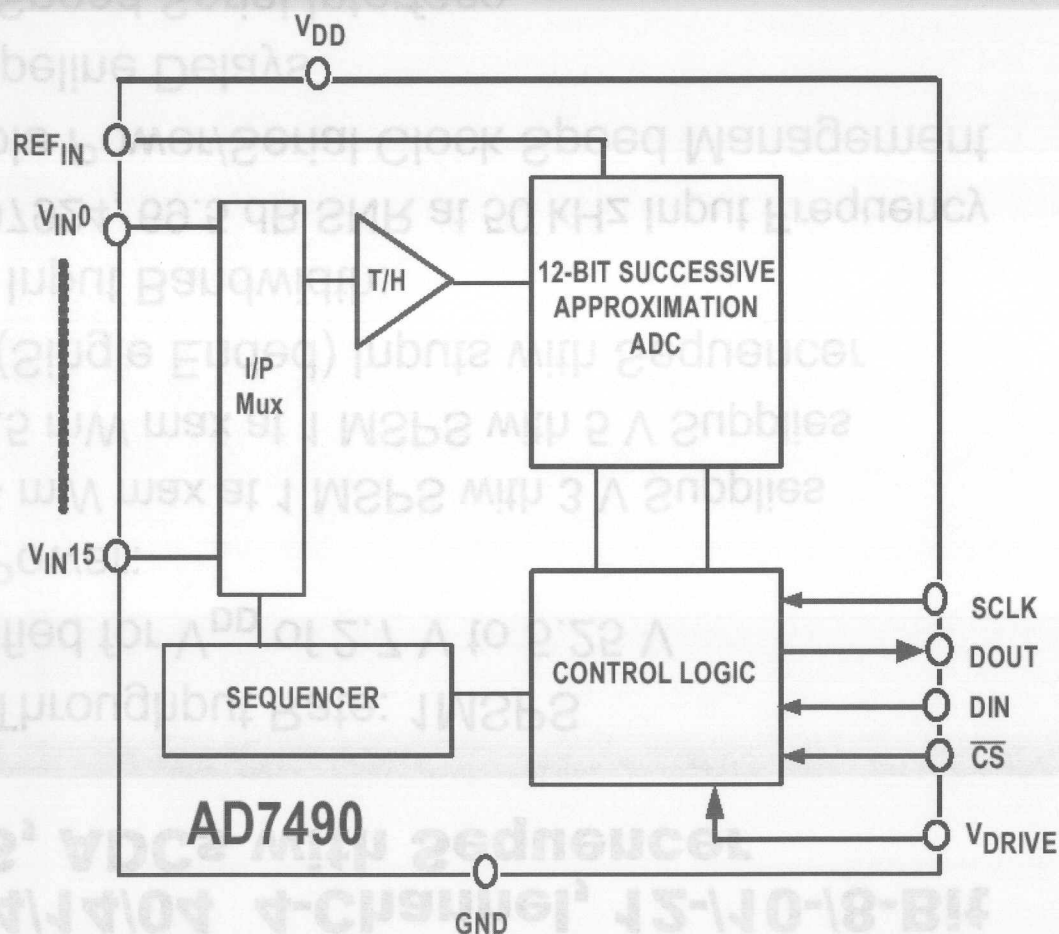
AD7924/14/04 4-Channel, 12-/10-/8-Bit 1 MSPS, ADCs with Sequencer



AD7924/14/04 4-Channel, 12-/10-/8-Bit 1 MSPS, ADCs with Sequencer

- Fast Throughput Rate: 1MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power:
 - 5.4 mW max at 1 MSPS with 3 V Supplies
 - 12.5 mW max at 1 MSPS with 5 V Supplies
- Four (Single Ended) Inputs with Sequencer
- Wide Input Bandwidth:
 - AD7924, 69.5 dB SNR at 50 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Shutdown Mode: 0.5 μ A max
- 16-Pin TSSOP Package

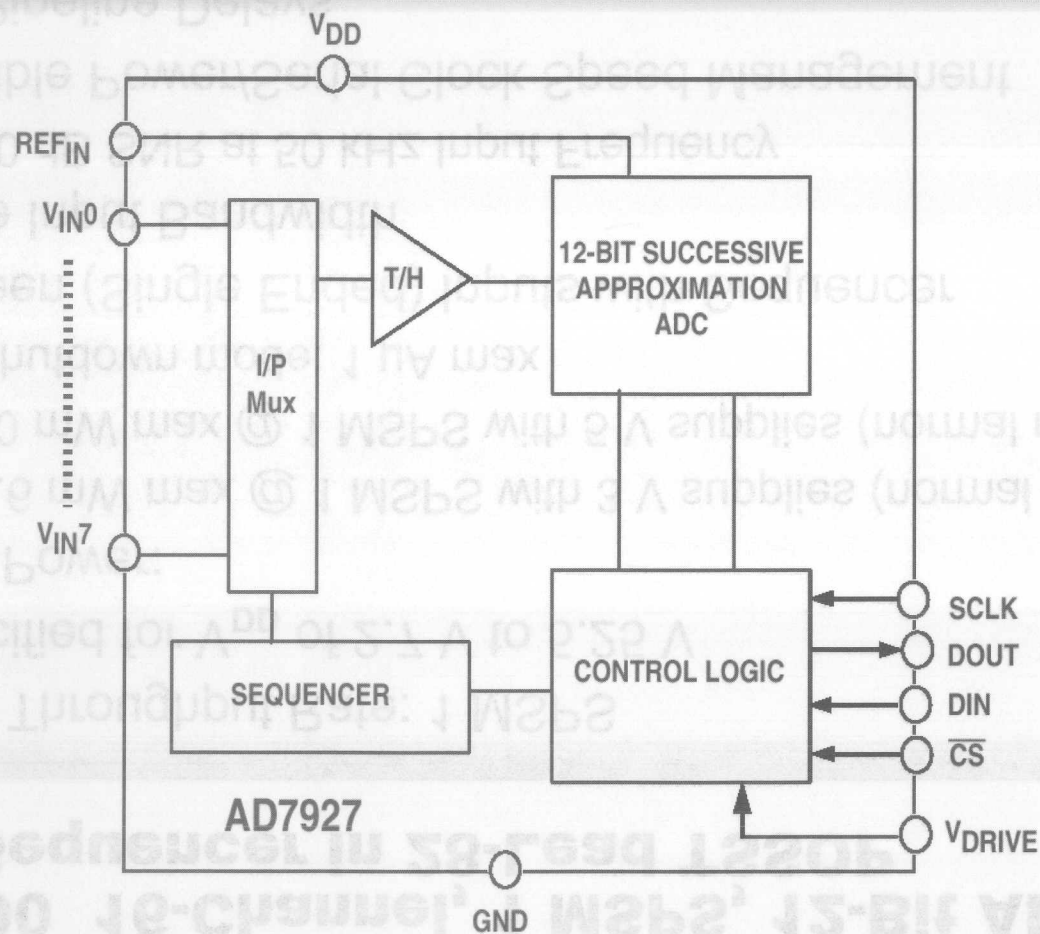
AD7490 16-Channel, 1 MSPS, 12-Bit ADC with Sequencer in 28-Lead TSSOP



AD7490 16-Channel, 1 MSPS, 12-Bit ADC with Sequencer in 28-Lead TSSOP

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power:
 - 3.6 mW max @ 1 MSPS with 3 V supplies (normal mode)
 - 10 mW max @ 1 MSPS with 5 V supplies (normal mode)
 - Shutdown mode: 1 μ A max
- Sixteen (Single Ended) Inputs with Sequencer
- Wide Input Bandwidth
 - 70 dB SNR at 50 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface SPI/QSPI/ μ Wire/DSPCompatible
- 28-Pin TSSOP and 32-Pin LFCSP Packages

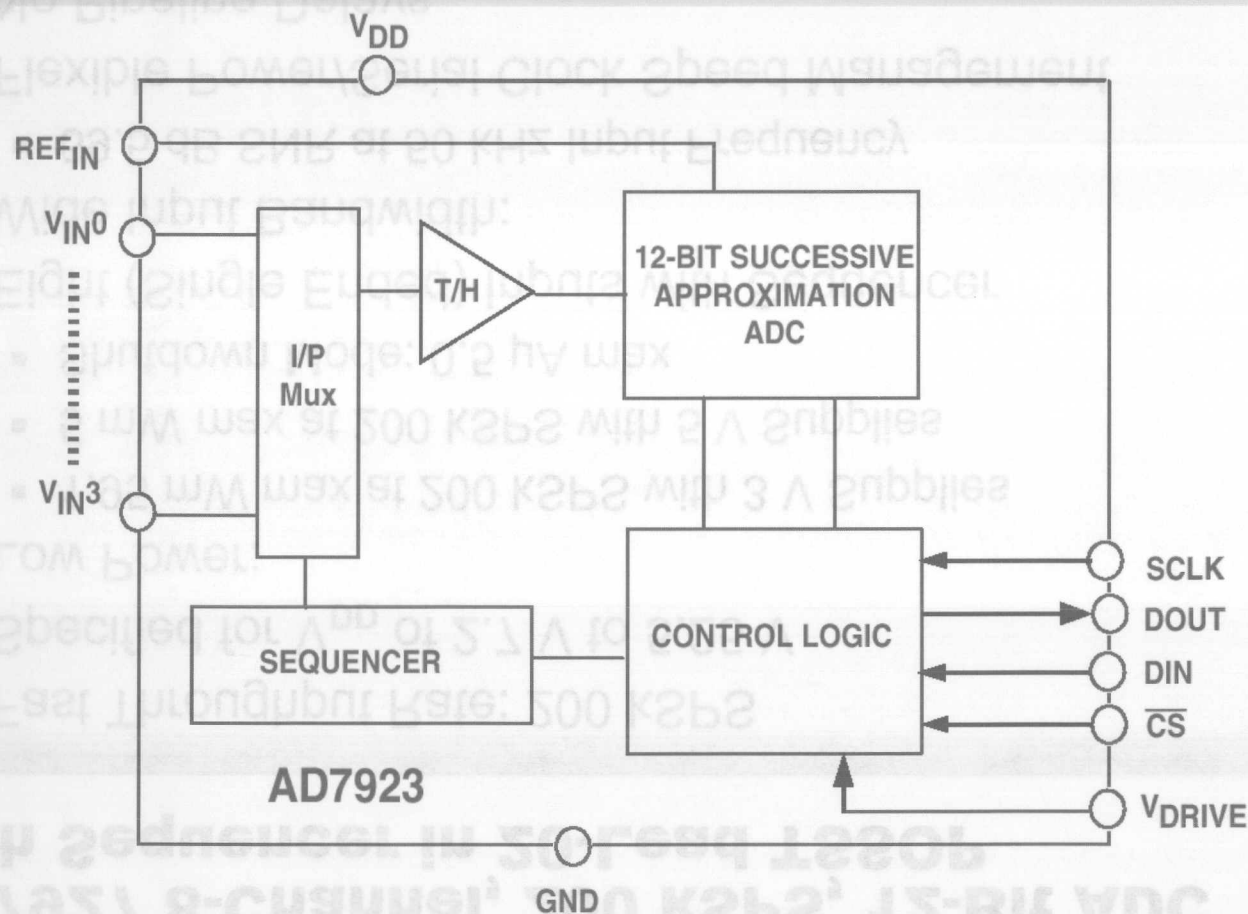
AD7927 8-Channel, 200 kSPS, 12-Bit ADC with Sequencer in 20-Lead TSSOP



AD7927 8-Channel, 200 kSPS, 12-Bit ADC with Sequencer in 20-Lead TSSOP

- Fast Throughput Rate: 200 kSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power:
 - 1.95 mW max at 200 kSPS with 3 V Supplies
 - 5 mW max at 200 kSPS with 5 V Supplies
 - Shutdown Mode: 0.5 μ A max
- Eight (Single Ended) Inputs with Sequencer
- Wide Input Bandwidth:
 - 69.5 dB SNR at 50 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- 20-Pin TSSOP Package

AD7923 4-Channel, 200 kSPS, 12-Bit ADC with Sequencer in 16-Lead TSSOP



AD7923 4-Channel, 200 kSPS, 12-Bit ADC with Sequencer in 16-Lead TSSOP

- Fast Throughput Rate: 200 kSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power:
 - 1.95 mW max at 200 kSPS with 3 V Supplies
 - 5 mW max at 200 kSPS with 5 V Supplies
- Four (Single Ended) Inputs with Sequencer
- Wide Input Bandwidth:
 - 69.5 dB SNR at 50 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
- Shutdown Mode: 0.5 μ A max
- 16-Pin TSSOP Package

- 10-bit 1250b Package
- Shutdown Mode: 0.2 μ A max

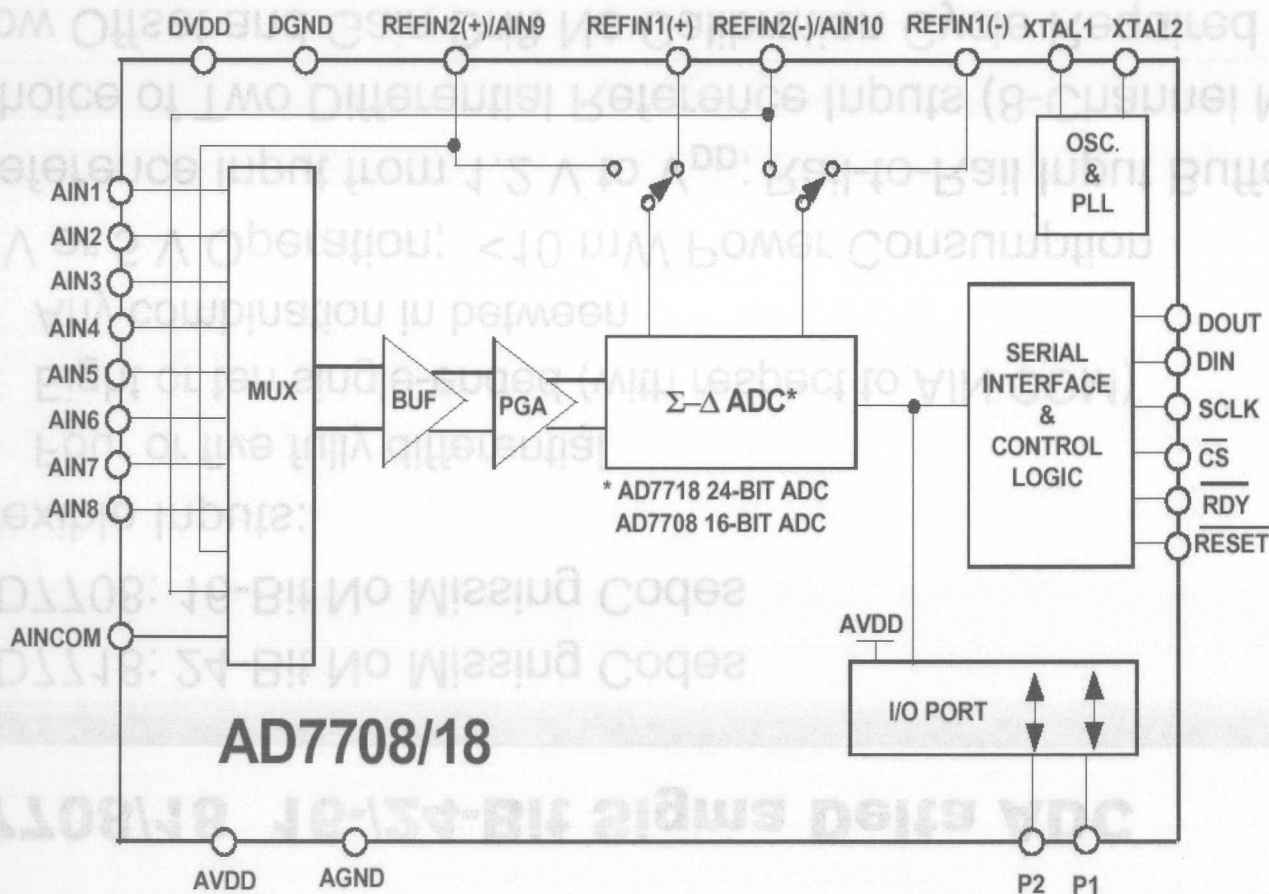
- High Speed Serial Interface
- No Pipeline Delays
- Flexible Power/Sleep Clock Speed Management
 - 10.2 dB SNR at 20 kHz Input Frequency
- Wide Input Range
- Low (Single Ended) Input Impedance
 - 2 mV max at 500 kSPS with 2 V supplies
 - 1.82 mV max at 500 kSPS with 3 V supplies
- Low Power

- Specified for V_{DD} of 5 V, 10, 2.5 V
- Fast Throughput Rate: 500 kSPS

Sigma-Delta ADCs

with 200msec in 10-sec 1250b
AD1253 4-Channel, 500 kSPS, 15-Bit VDC

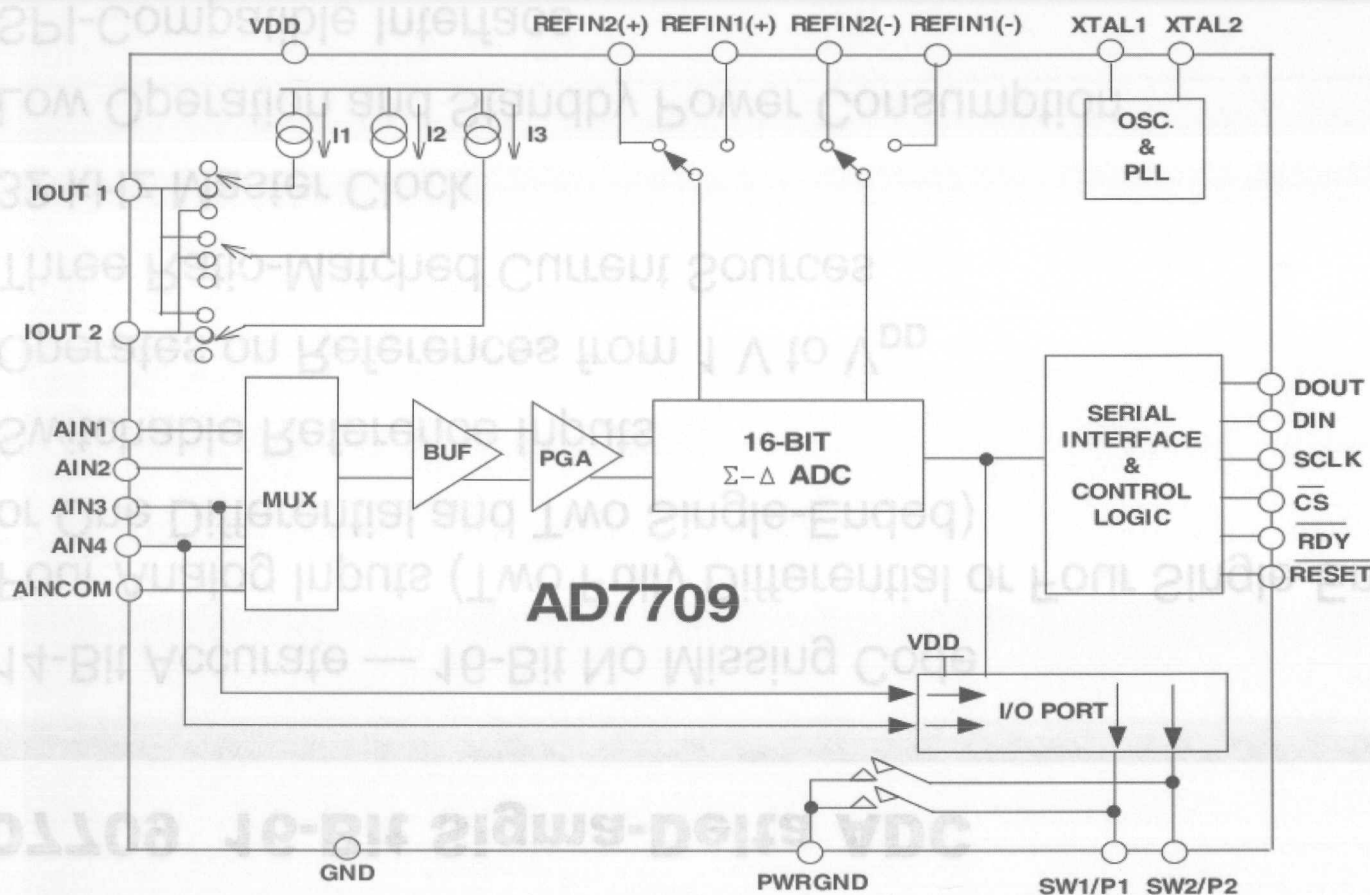
AD7708/18 16-/24-Bit Sigma Delta ADC



AD7708/18 16-/24-Bit Sigma Delta ADC

- AD7718: 24-Bit No Missing Codes
- AD7708: 16-Bit No Missing Codes
- Flexible Inputs:
 - Four or five fully differential
 - Eight or ten single-ended (with respect to AIN COM)
 - Any combination in between
- 3 V or 5 V Operation; <10 mW Power Consumption
- Reference Input from 1.2 V to V_{DD} ; Rail-to-Rail Input Buffer
- Choice of Two Differential Reference Inputs (8-Channel Mode)
- Low Offset and Gain Drift No Calibration Cycle Required
- 32 kHz Master Clock
- 2-Pin I/O Port
- Register and Pin Compatible

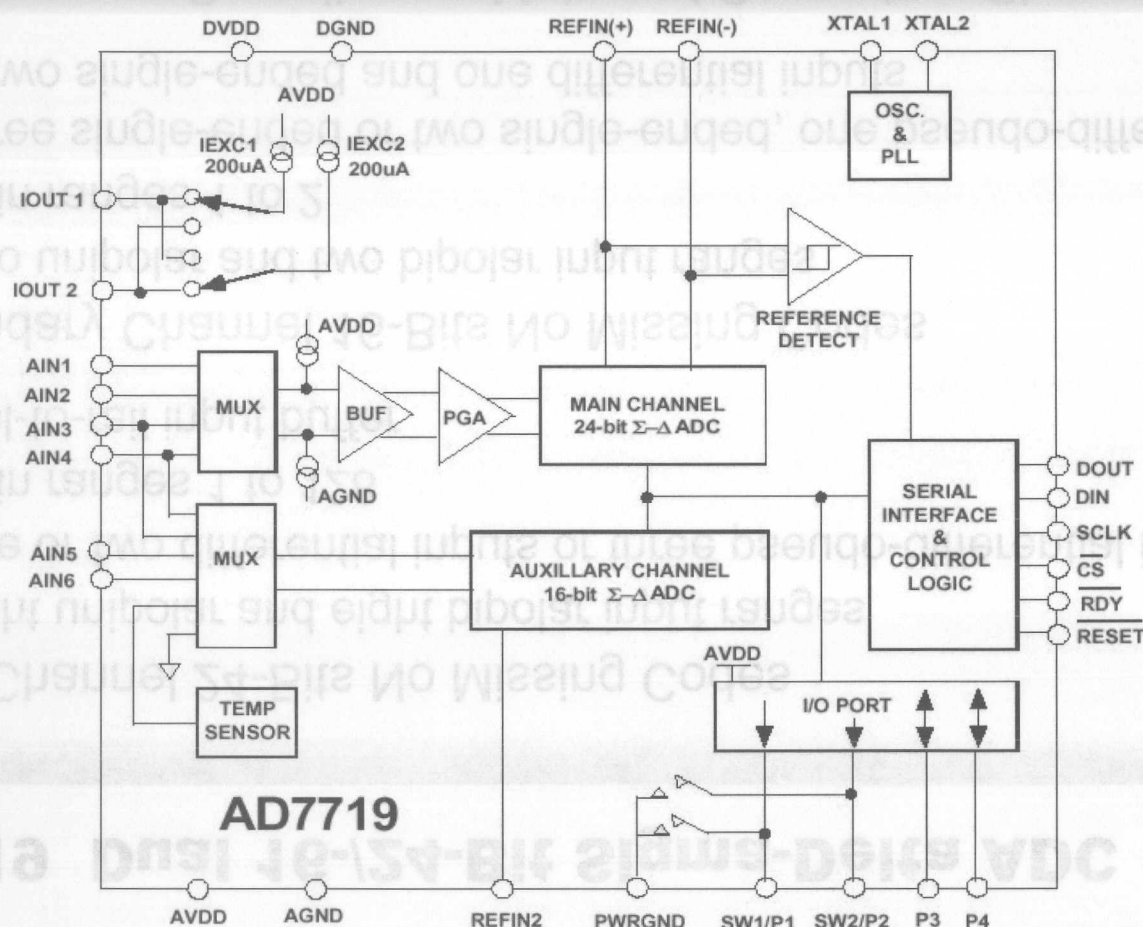
AD7709 16-Bit Sigma-Delta ADC



AD7709 16-Bit Sigma-Delta ADC

- 14-Bit Accurate — 16-Bit No Missing Code
- Four Analog Inputs (Two Fully Differential or Four Single-Ended, or One Differential and Two Single-Ended)
- Switchable Reference Inputs
- Operates on References from 1 V to V_{DD}
- Three Ratio-Matched Current Sources
- 32 kHz Master Clock
- Low Operation and Standby Power Consumption
- SPI-Compatible Interface
- Two Digital Inputs and Two Digital Outputs: Two Low Side Power Switches

AD7719 Dual 16-/24-Bit Sigma-Delta ADC



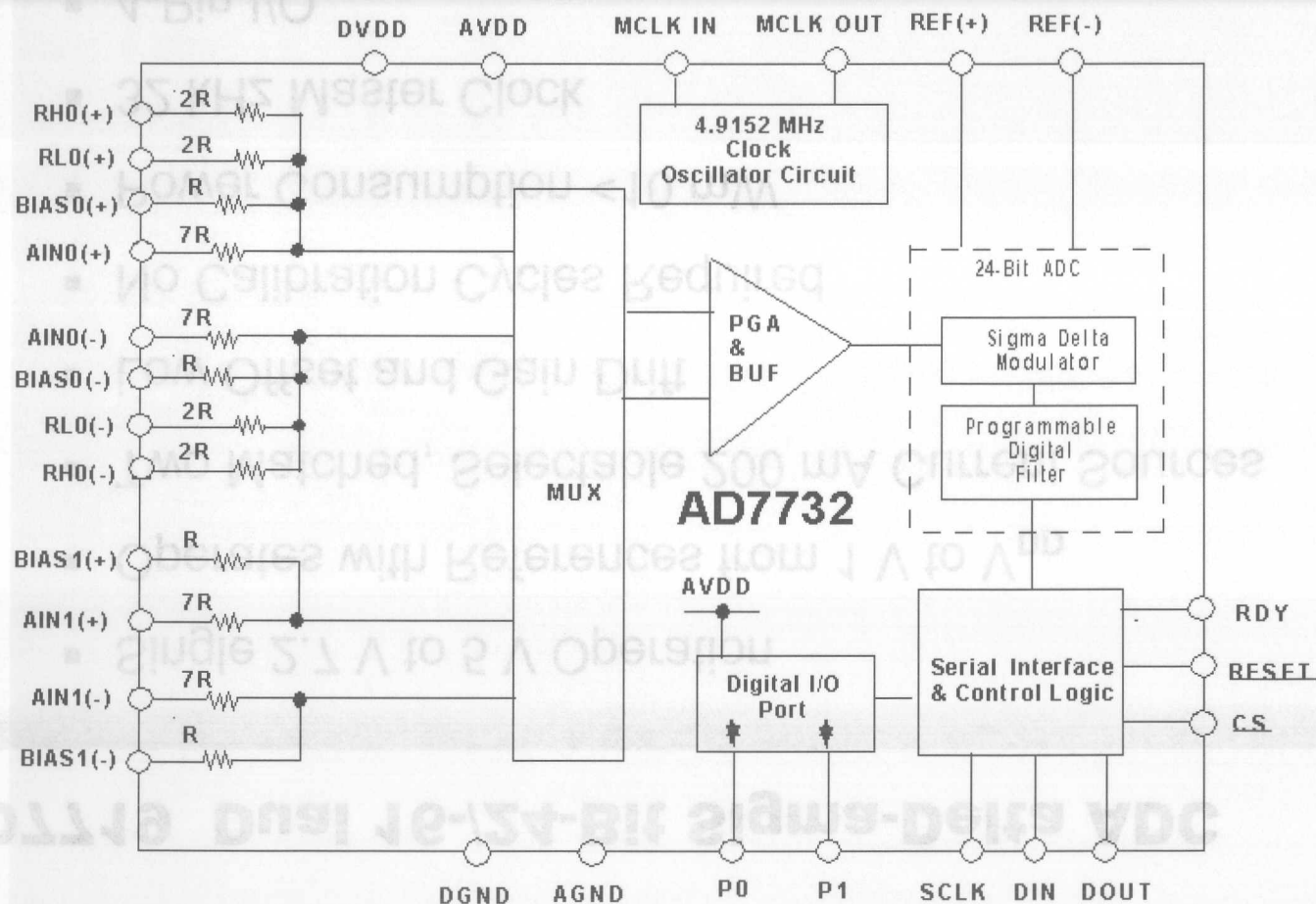
AD7719 Dual 16-/24-Bit Sigma-Delta ADC

- Main Channel 24-Bits No Missing Codes
 - Eight unipolar and eight bipolar input ranges
 - One or two differential inputs or three pseudo-differential inputs
 - Gain ranges 1 to 128
 - Rail-to-rail input buffer
- Secondary Channel 16-Bits No Missing Codes
 - Two unipolar and two bipolar input ranges
 - Gain ranges 1 to 2
 - Three single-ended or two single-ended, one pseudo-differential or two single-ended and one differential inputs
- Simultaneous Sampling on Main and Secondary Channels

AD7719 Dual 16-/24-Bit Sigma-Delta ADC

- Single 2.7 V to 5 V Operation
- Operates with References from 1 V to V_{DD}
- Two Matched, Selectable 200 mA Current Sources
- Low Offset and Gain Drift
- No Calibration Cycles Required
- Power Consumption <10 mW
- 32 kHz Master Clock
- 4-Pin I/O
- 28-Lead SOIC and TSSOP Packages

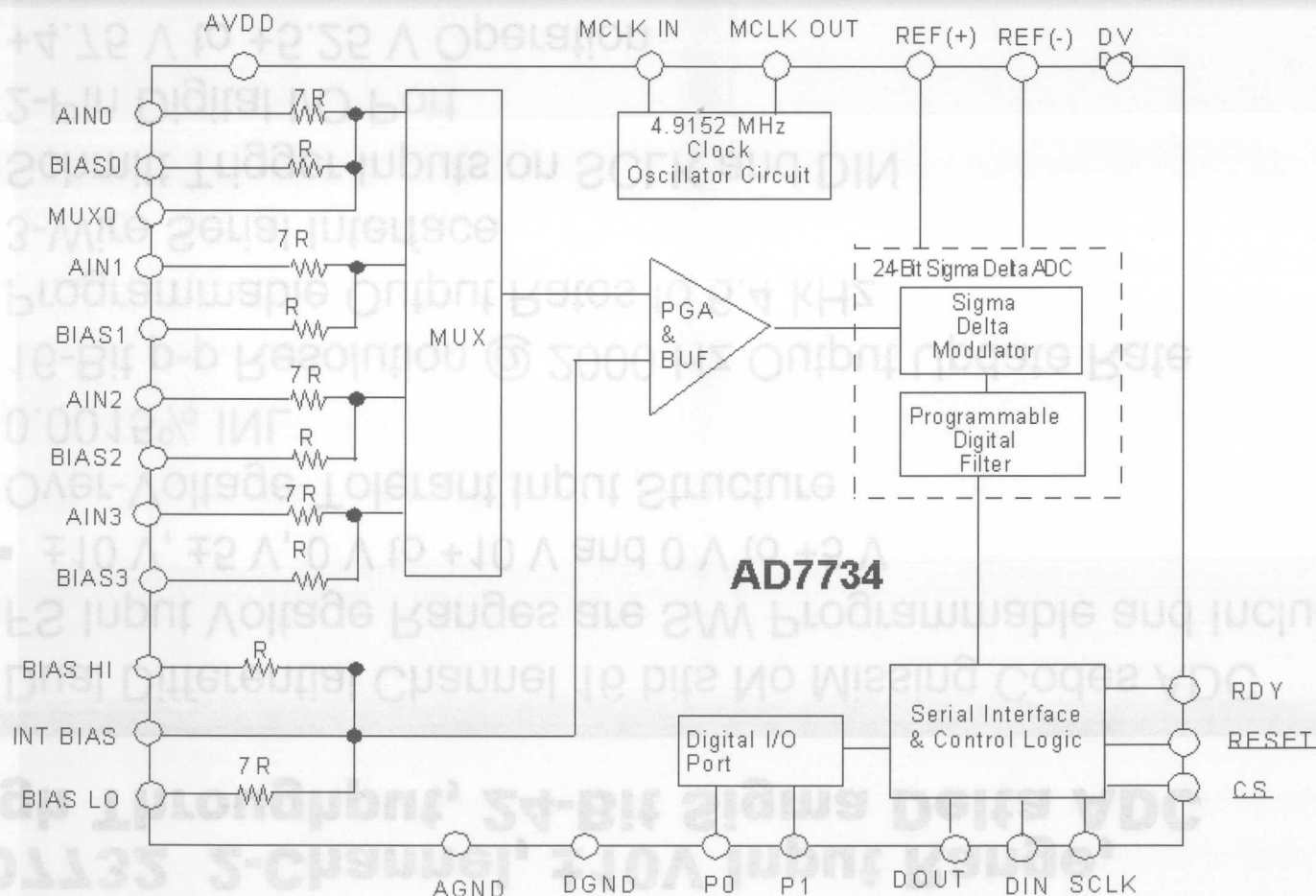
AD7732 2-Channel, $\pm 10\text{V}$ Input Range, High Throughput, 24-Bit Sigma Delta ADC



AD7732 2-Channel, $\pm 10\text{V}$ Input Range, High Throughput, 24-Bit Sigma Delta ADC

- Dual Differential Channel 16 bits No Missing Codes ADC
- FS Input Voltage Ranges are S/W Programmable and Include:
 - $\pm 10\text{ V}$, $\pm 5\text{ V}$, 0 V to $+10\text{ V}$ and 0 V to $+5\text{ V}$
- Over-Voltage-Tolerant Input Structure
- 0.0015% INL
- 16-Bit p-p Resolution @ 2000 Hz Output Update Rate
- Programmable Output Rates to 6.4 kHz
- 3-Wire Serial Interface
- Schmitt Trigger Inputs on SCLK and DIN
- 2-Pin Digital I/O Port
- $+4.75\text{ V}$ to $+5.25\text{ V}$ Operation
- 4.9152 MHz Operation Allowing Low Cost SM Crystals
- Operates with Reference Voltage of $+2.5\text{ V}$
- Either Channel Can Be Externally Trimmed to Improve CMR

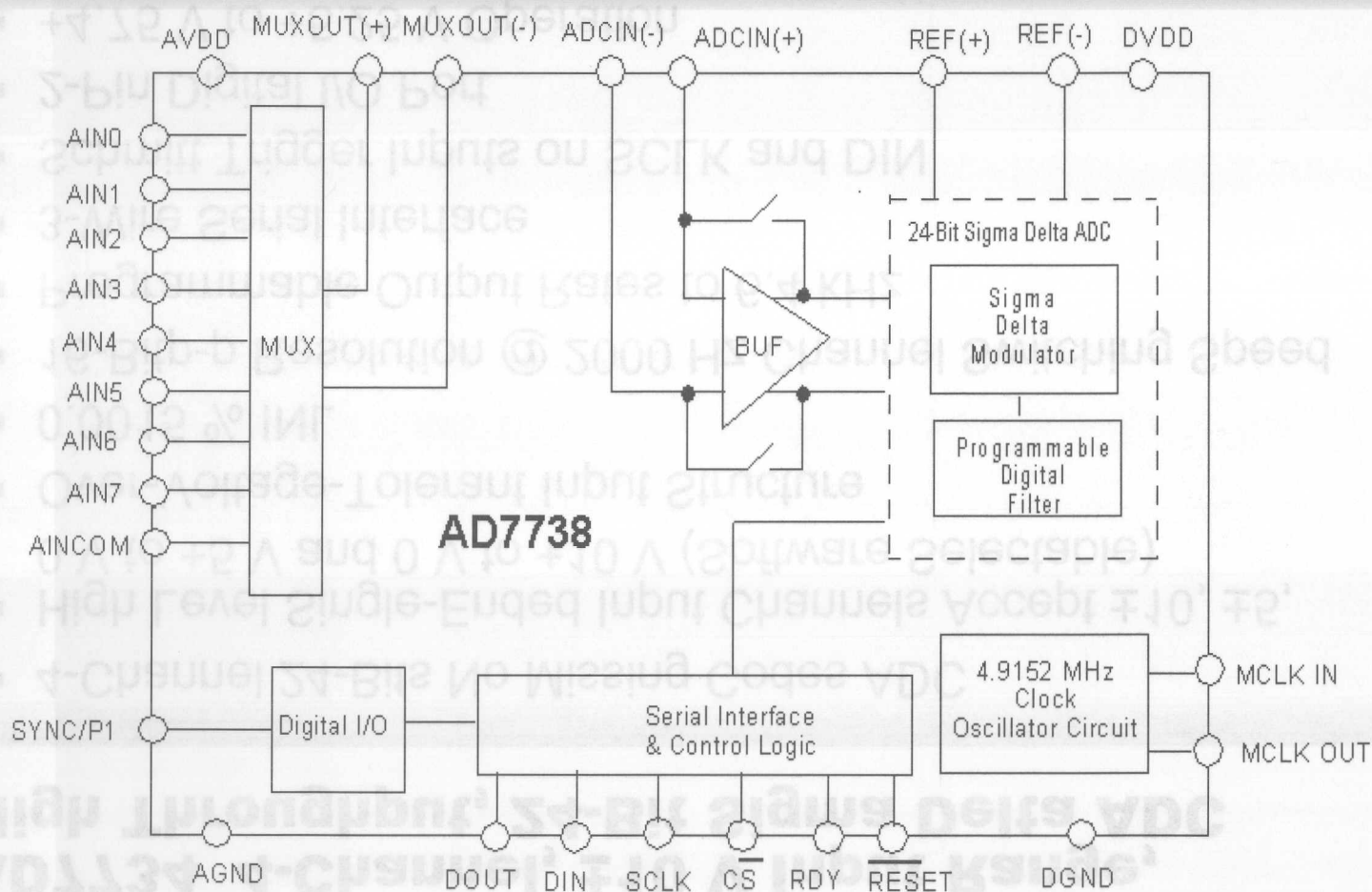
AD7734 4-Channel, ± 10 V Input Range, High Throughput, 24-Bit Sigma Delta ADC



AD7734 4-Channel, ± 10 V Input Range, High Throughput, 24-Bit Sigma Delta ADC

- 4-Channel 24-Bits No Missing Codes ADC
- High Level Single-Ended Input Channels Accept ± 10 , ± 5 , 0 V to +5 V and 0 V to +10 V (Software Selectable)
- Over-Voltage-Tolerant Input Structure
- 0.0015 % INL
- 16-Bitp-p Resolution @ 2000 Hz Channel Switching Speed
- Programmable Output Rates to 6.4 kHz
- 3-Wire Serial Interface
- Schmitt Trigger Inputs on SCLK and DIN
- 2-Pin Digital I/O Port
- +4.75 V to +5.25 V Operation
- 4.9152 MHz Operation Allowing Low Cost SM Crystals
- Operates with Reference Voltage of +2.5 V

AD7738 8-Channel, High Throughput, 24-Bit Sigma-Delta ADC



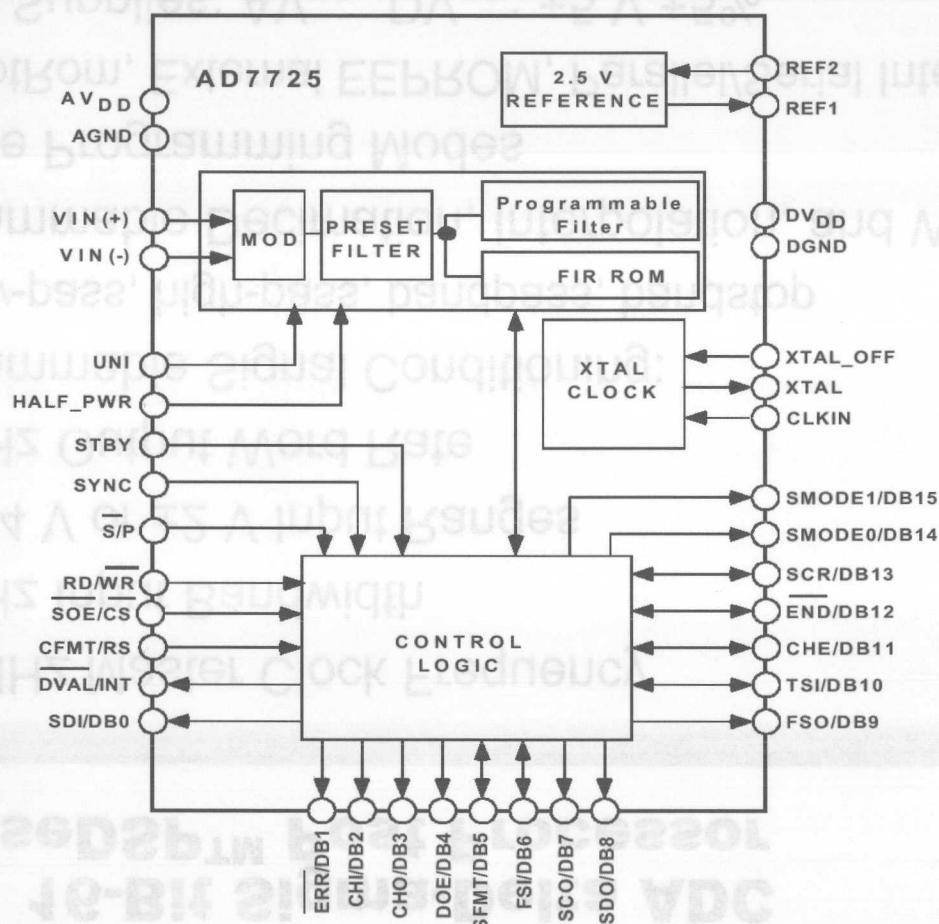
AD7738 8-Channel, High Throughput, 24-Bit Sigma-Delta ADC

- 24-Bits No Missing Codes ADC
- Eight Analog Inputs which Can Be Configured as Follows:
 - Four Fully differential inputs
 - Eight Single-ended I/Ps with respect to $A_{IN COM}$
 - Or any combination in between
- Bipolar/Unipolar 1.25 V and 0.625 V Inputs
- 0.0015 % INL
- 16-Bitp-p Resolution @ 2000 Hz Channel Switching Speed with 500 μ s Settling Time
- Programmable Output Rates to 6.4 kHz
- Input Voltage Range of $\pm V_{REF}/2$

AD7738 8-Channel, High Throughput, 24-Bit Sigma-Delta ADC

- 3-Wire Serial Interface
- MUXOUT/ADCIN Facility Allows External Preamp
- +4.75 V to +5.25 V Operation
- 4.9152 MHz Operation Allowing Low Cost SM Crystals
- Operates with Reference Voltage of +2.5 V
- 28-Lead TSSOP
- Schmitt Trigger Inputs on SCLK and DIN

AD7725 16-Bit Sigma-Delta ADC with PulseDSP™ Post Processor

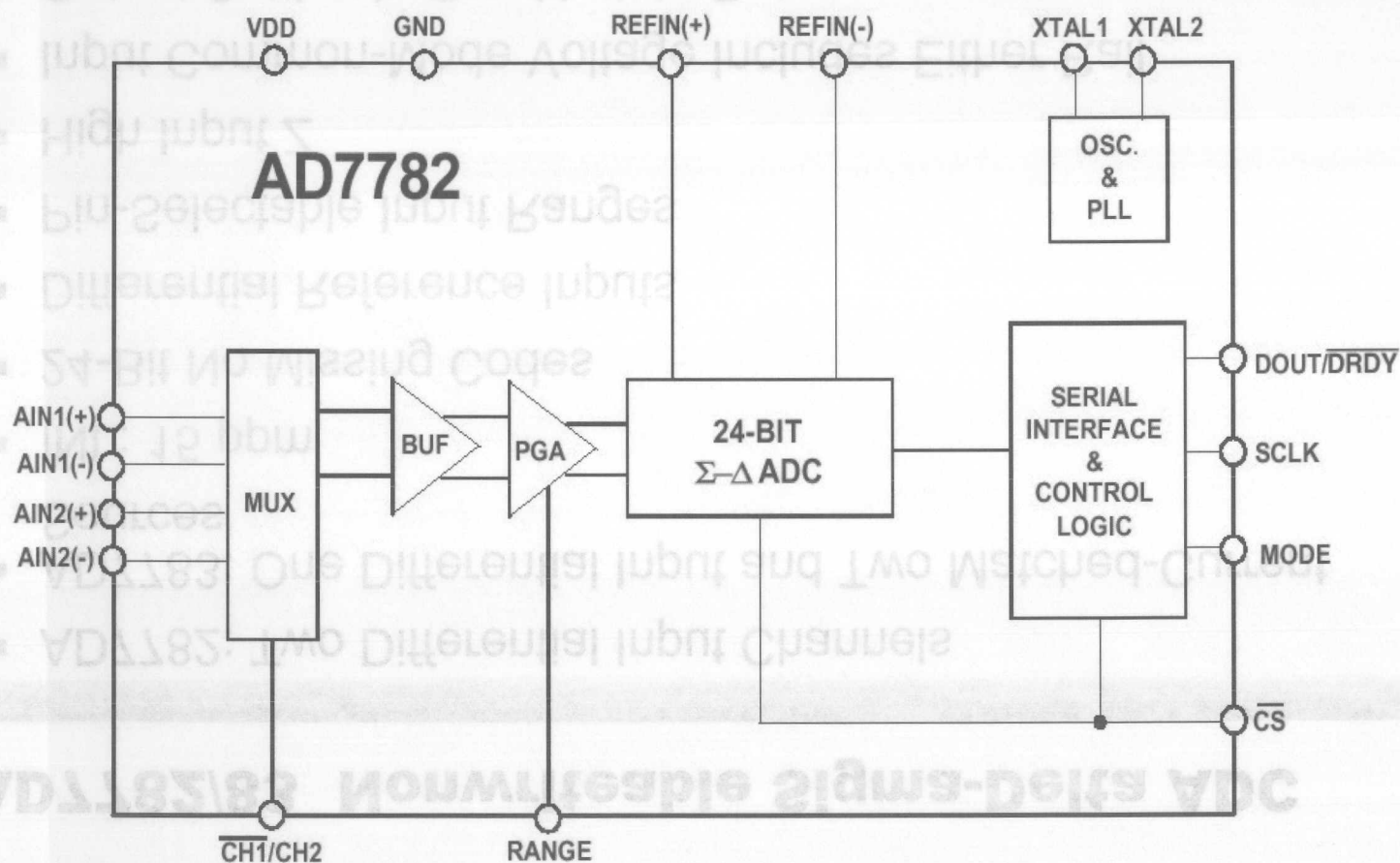


AD7725 16-Bit Sigma-Delta ADC with PulseDSP™ Post Processor

- 19.2 MHz Master Clock Frequency
- 460 kHz Input Bandwidth
- 0 V to 4 V or ± 2 V Input Ranges
- 1.2 MHz Output Word Rate
- Programmable Signal Conditioning:
 - Low-pass, high-pass, bandpass, bandstop
- Programmable Decimation, Interpolation, and Word Rate
- Flexible Programming Modes
 - BootRom, External EEPROM, Parallel/Serial Interface
- Power Supplies: AV_{DD} , DV_{DD} : +5 V $\pm 5\%$
- On-Chip 2.5 V Voltage Reference
- 44-Pin PQFP

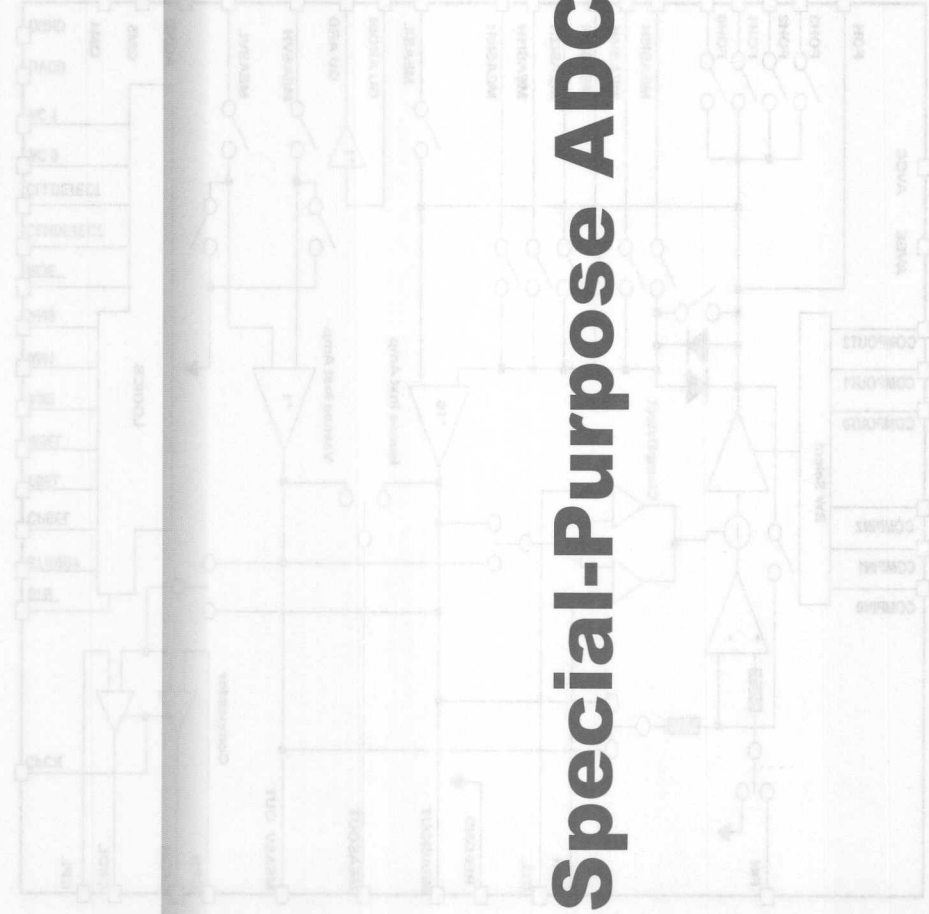
PulseDSP is a trademark of Systolix

AD7782/83 Nonwriteable Sigma-Delta ADC



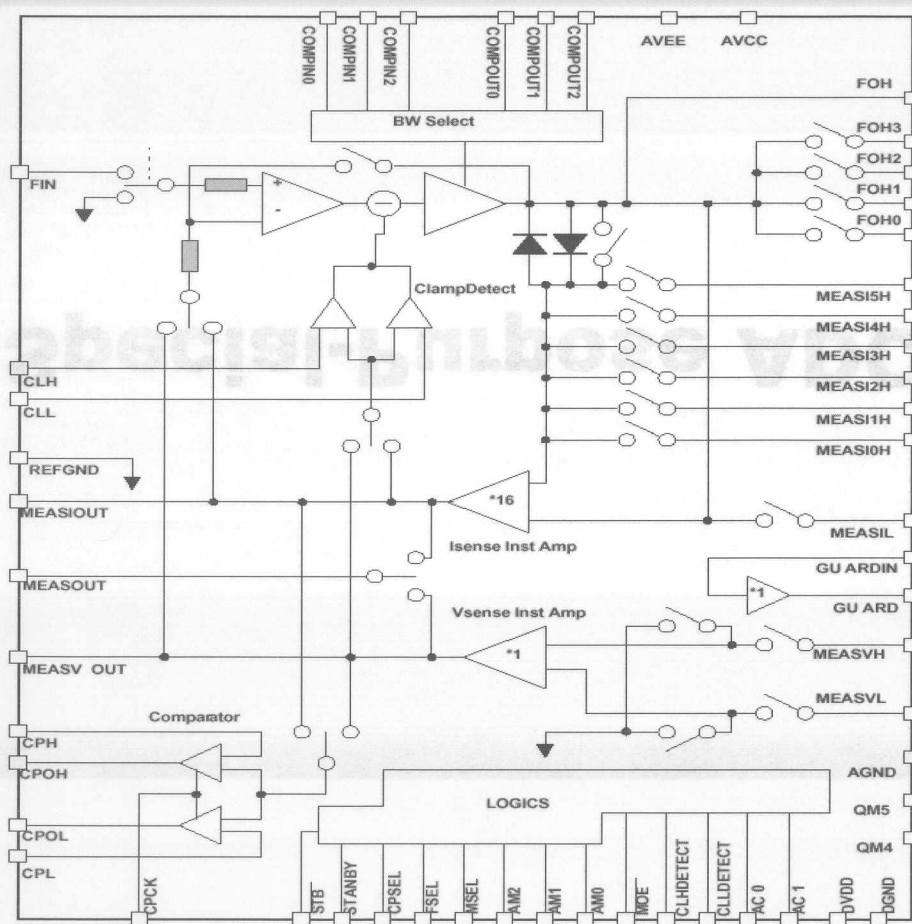
AD7782/83 Nonwriteable Sigma-Delta ADC

- AD7782: Two Differential Input Channels
- AD7783: One Differential Input and Two Matched-Current Sources
- INL: 15 ppm
- 24-Bit No Missing Codes
- Differential Reference Inputs
- Pin-Selectable Input Ranges
- High Input Z
- Input Common-Mode Voltage Includes Either Rail
- Output Settles in One Update Rate
- Simultaneous 50 Hz and 60 Hz Common-Mode Rejection
- Read Only Operation



Special-Purpose ADCs

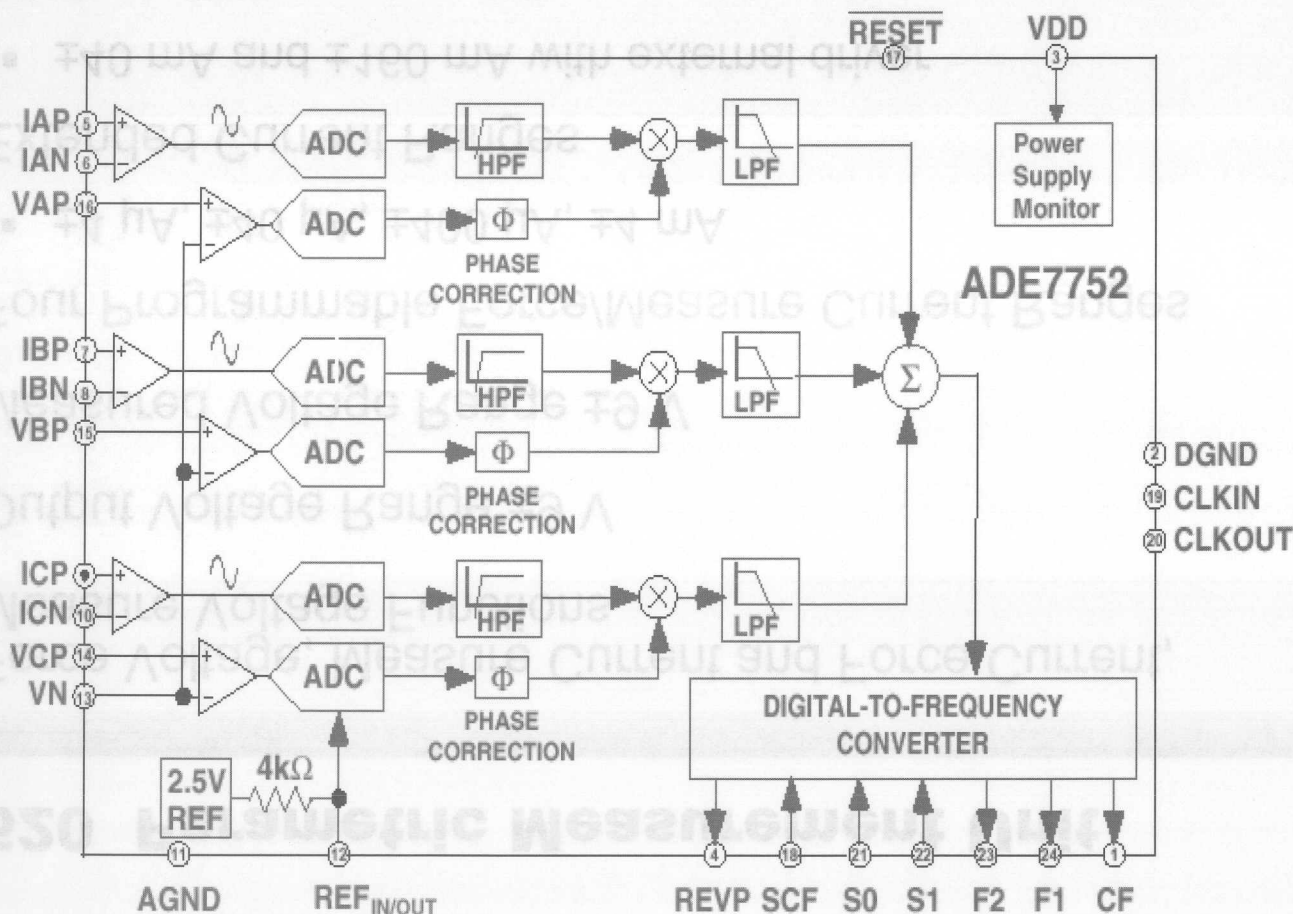
AD5520 Parametric Measurement Unit



AD5520 Parametric Measurement Unit

- Force Voltage, Measure Current and Force Current, Measure Voltage Functions
- Output Voltage Range ± 9 V
- Measured Voltage Range ± 9 V
- Four Programmable Force/Measure Current Ranges
 - ± 4 μ A, ± 40 μ A, ± 400 μ A, ± 4 mA
- Extended Current Ranges
 - ± 40 mA and ± 160 mA with external driver
- 64-Pin LQFP

ADE7752 3-Phase Energy Metering IC with Pulse Output



ADE7752 3-Phase Energy Metering IC with Pulse Output

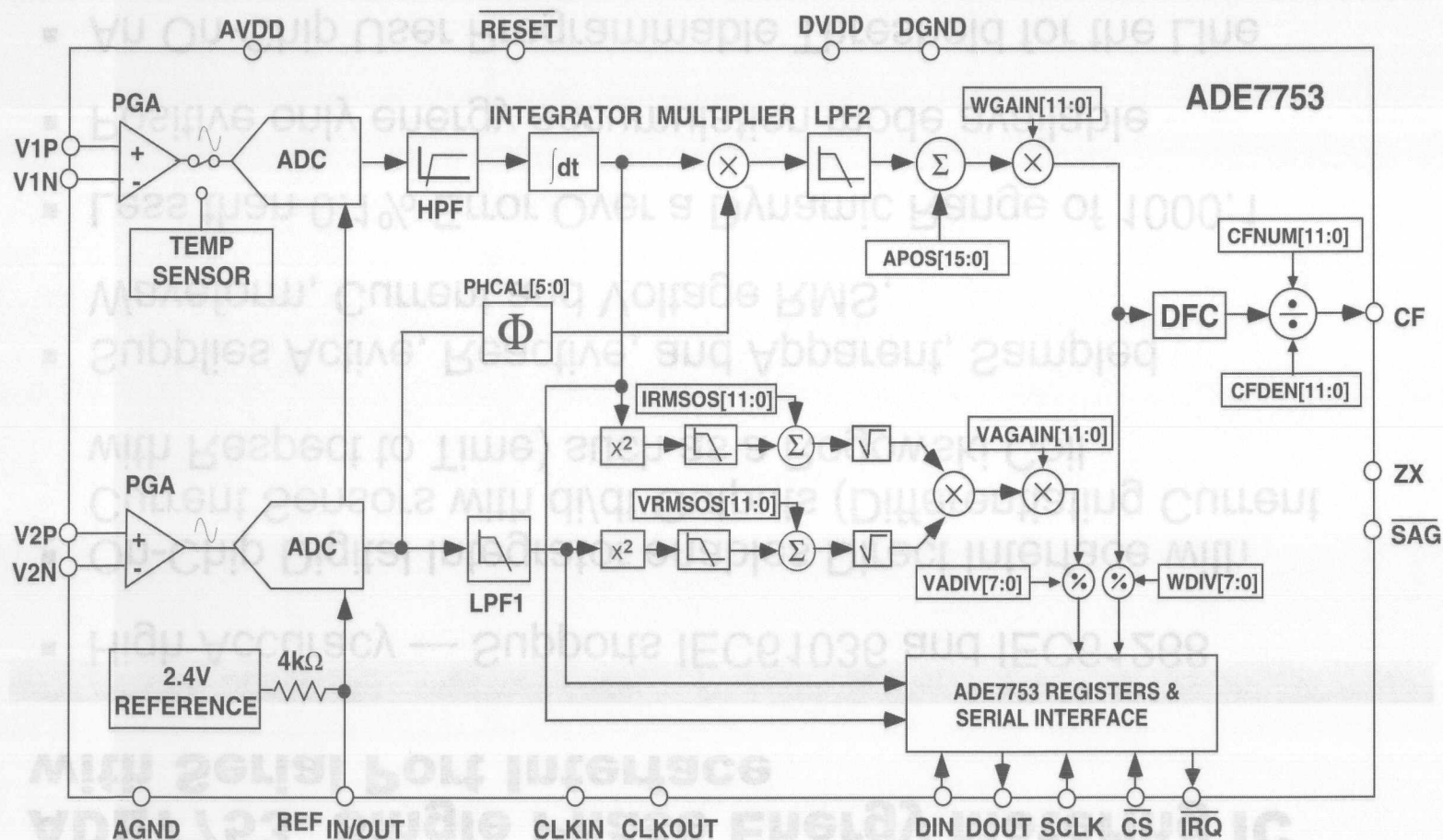
- High Accuracy, Supports 50 Hz/60 Hz IEC 687/1036
- Less than 0.1% Error Over a Dynamic Range of 500 to 1
- Compatible with 3-Phase / 3-Wire and 3-Phase / 4-Wire Configurations
- The ADE7752 Supplies Average Real Power on the Frequency Outputs F1 and F2
- The High Frequency Output CF Is Intended for Calibration and Supplies Instantaneous Real Power
- The Logic Output REVP indicates a Potential Miswiring or Negative Power for Each Phase
- Direct Drive for Electromechanical Counters and 2-Phase Stepper Motors (F1 and F2)



ADE7752 3-Phase Energy Metering IC with Pulse Output

- Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
- On-Chip Power Supply Monitoring
- On-Chip Creep Protection (No Load Threshold)
- On-Chip Reference $2.5\text{ V} \pm 8\%$ (30 ppm/°C Typical) with External Overdrive Capability
- Single 5 V Supply, Low Power (15 mW Typical)
- 24-Lead SOIC Package

ADE7753 Single Phase Energy Metering IC with Serial Port Interface



ADE7753 Single Phase Energy Metering IC with Serial Port Interface

- High Accuracy — Supports IEC61036 and IEC61268
- On-Chip Digital Integrator enables Direct Interface with Current Sensors with di/dt Outputs (Differentiating Current with Respect to Time) such as a Rogowski Coil
- Supplies Active, Reactive, and Apparent, Sampled Waveform, Current and Voltage RMS,
- Less than 0.1% Error Over a Dynamic Range of 1000:1
- Positive only energy accumulation mode available
- An On-Chip User Programmable Threshold for the Line Voltage surge and SAG, and PSU supervisory
- Digital Power, Phase & Input Offset Calibration

ADE7753 Single Phase Energy Metering IC with Serial Port Interface

- On-Chip Temperature Sensor ($\pm 3^{\circ}\text{C}$ (Typ) after Calibration)
- A SPI-Compatible Serial Interface
- A Pulse Output with Programmable Frequency
- An Interrupt Request pin (IRQ) and Status Register
- Proprietary ADCs and DSP Provide High Accuracy Over Large Variations in Environmental Conditions and Time
- On-Chip Reference $2.4\text{ V} \pm 8\%$ (30 ppm/ $^{\circ}\text{C}$ Typical) with External Overdrive Capability
- Single 5 V Supply, Low Power 25 mW (Typ)
- 20-Lead SSOP Package

With Serial Port Interface



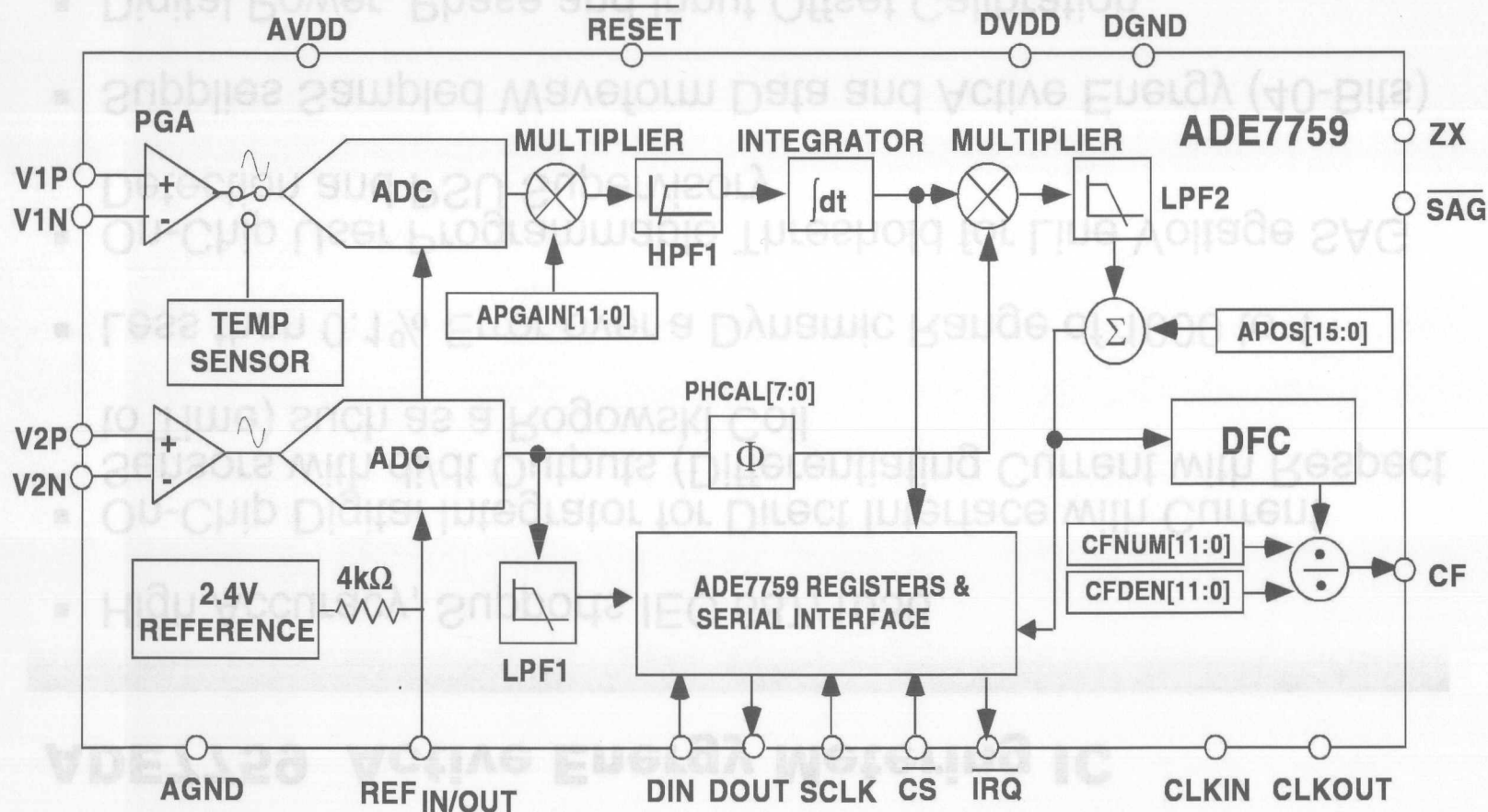
ADE7754 3-Phase Energy Metering IC with Serial Port Interface

- High Accuracy — Supports IEC 687/1036
- Compatible with 3-Phase / 3-Wire or 3-Phase / 4-Wire Configurations and any Type of 3-Phase Services
- < 0.1 % Error Over a 500:1 Dynamic Range
- Supplies Active Energy, Apparent Energy, Voltage RMS, Current RMS, Sign of Reactive Energy, Sampled Waveform Data
- On-Chip Programmable Threshold for the Line Voltage SAG and Overdrive (PEAK) Detections
- Line Period
- Digital Power, Phase, and Input Offset Calibration

ADE7754 3-Phase Energy Metering IC with Serial Port Interface

- Pulse Output with Programmable Frequency
- On-Chip Temperature Sensor ($\pm 3^{\circ}$ C (Typ) after Calibration)
- SPI-Compatible Serial Interface
- IRQ and Status Register Provide Early Warning of Register Overflow
- Proprietary ADCs and DSP Provide High Accuracy Over Large Variations in Environmental Conditions and Time
- Single 5 V Supply, Low Power 15 mW (Typ)
- 24-Lead SOIC Package

ADE7759 Active Energy Metering IC



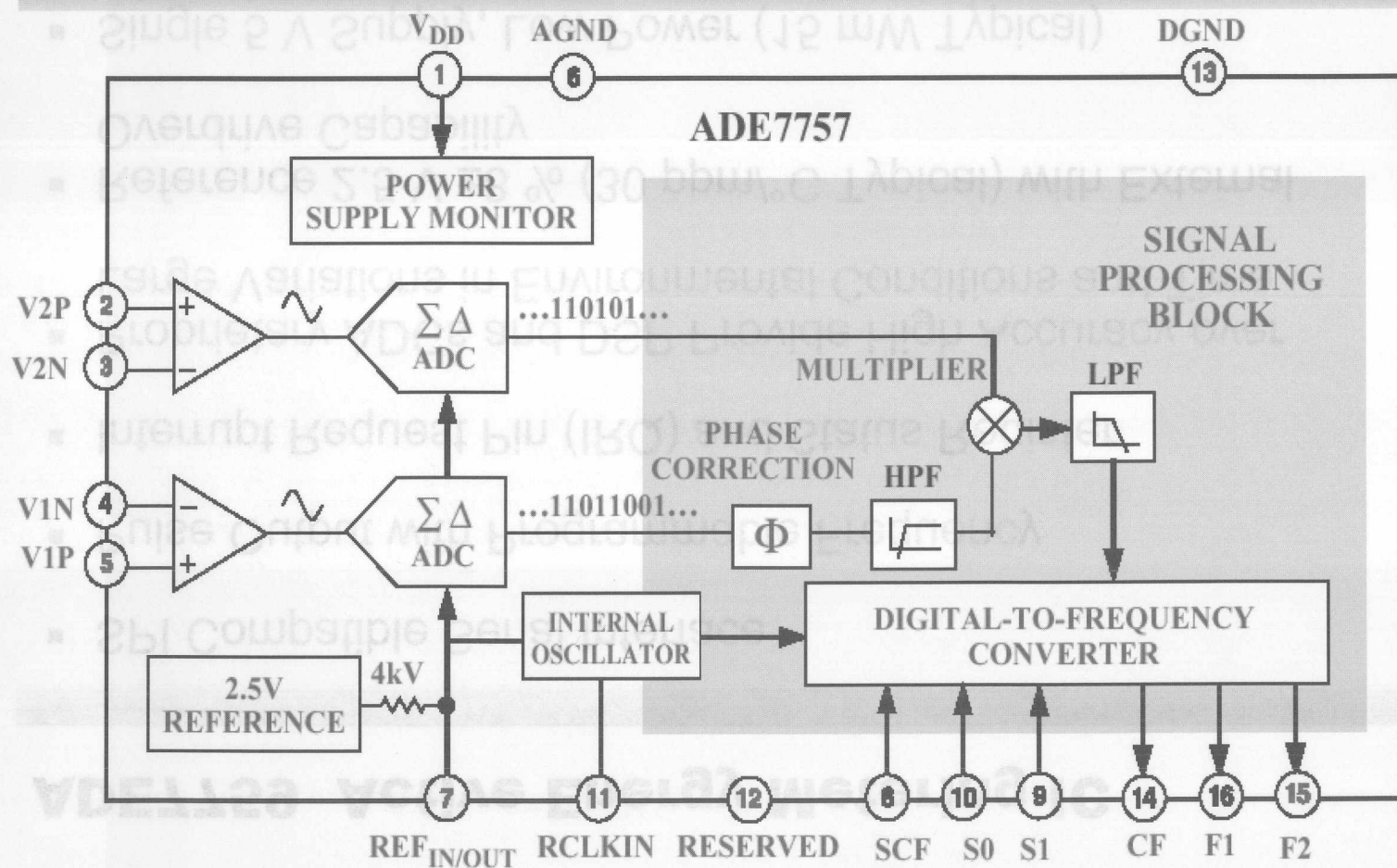
ADE7759 Active Energy Metering IC

- High Accuracy, Supports IEC 687/1036
- On-Chip Digital Integrator for Direct Interface with Current Sensors with di/dt Outputs (Differentiating Current with Respect to Time) such as a Rogowski Coil
- Less than 0.1% Error over a Dynamic Range of 1000 to 1
- On-Chip User Programmable Threshold for Line Voltage SAG Detection and PSU Supervisory
- Supplies Sampled Waveform Data and Active Energy (40-Bits)
- Digital Power, Phase and Input Offset Calibration.
- On-Chip Temperature Sensor ($\pm 3^{\circ}\text{C}$ Typical after Calibration)

ADE7759 Active Energy Metering IC

- SPI Compatible Serial Interface
- Pulse Output with Programmable Frequency
- Interrupt Request Pin (IRQ) and Status Register
- Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
- Reference $2.5\text{ V} \pm 8\%$ (30 ppm/°C Typical) with External Overdrive Capability
- Single 5 V Supply, Low Power (15 mW Typical)
- 20-Lead SSOP Package

ADE7757 Energy Metering IC with Integrated Oscillator



ADE7757 Energy Metering IC with Integrated Oscillator

- On Chip Oscillator as clock source
- High Accuracy, Supports 50 Hz/ 60 Hz IEC 521/1036
- Less than 0.1 % Error Over a Dynamic Range of 500:1
- The ADE7757 Supplies Average Real Power on the Frequency Outputs F1 and F2
- The High Frequency Output CF Is Intended for Calibration and Supplies Instantaneous Real Power
- Direct Drive for Electromechanical Counters and Two Phase Stepper Motors (F1 and F2)
- Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time

ADE7757 Energy Metering IC with Integrated Oscillator

- On-Chip Power Supply Monitoring
- On-Chip Creep Protection (No Load Threshold)
- On-Chip Reference 2.5 V 8 % (30 ppm Typical) with External Overdrive Capability
- Single 5 V Supply, Low Power
- Low Cost CMOS Process
- AC Input only
- Pin Reduction Version of the ADE7755
 - With Clock Oscillator Enhancement

Energy Metering Products Selection Guide

Analog Front End and Fixed Function ICs						
Applications		Analog Calibration	Analog Cal + Anti-tamper	Analog Cal + Internal Oscillator	Digital Calibration	Digital Cal + di/dt Integrator
3-Phase	Programmable processor-based meter					ADE7754
	Single Chip with Stepper Counter Display	ADE7752				
1-Phase	Programmable processor-based meter				ADE7756	ADE7759 ADE7753
	Single Chip with Stepper Counter Display	ADE7755	ADE7751	ADE7757	ADE7735	

Products available today

New Products sampling or available in 2002

Processor	VDE1122	VDE1121	VDE1120	VDE1119	VDE1118	VDE1117	VDE1116	VDE1115	VDE1114	VDE1113	VDE1112	VDE1111	VDE1110	VDE1109	VDE1108	VDE1107	VDE1106	VDE1105	VDE1104	VDE1103	VDE1102	VDE1101	VDE1100	VDE1099	VDE1098	VDE1097	VDE1096	VDE1095	VDE1094	VDE1093	VDE1092	VDE1091	VDE1090	VDE1089	VDE1088	VDE1087	VDE1086	VDE1085	VDE1084	VDE1083	VDE1082	VDE1081	VDE1080	VDE1079	VDE1078	VDE1077	VDE1076	VDE1075	VDE1074	VDE1073	VDE1072	VDE1071	VDE1070	VDE1069	VDE1068	VDE1067	VDE1066	VDE1065	VDE1064	VDE1063	VDE1062	VDE1061	VDE1060	VDE1059	VDE1058	VDE1057	VDE1056	VDE1055	VDE1054	VDE1053	VDE1052	VDE1051	VDE1050	VDE1049	VDE1048	VDE1047	VDE1046	VDE1045	VDE1044	VDE1043	VDE1042	VDE1041	VDE1040	VDE1039	VDE1038	VDE1037	VDE1036	VDE1035	VDE1034	VDE1033	VDE1032	VDE1031	VDE1030	VDE1029	VDE1028	VDE1027	VDE1026	VDE1025	VDE1024	VDE1023	VDE1022	VDE1021	VDE1020	VDE1019	VDE1018	VDE1017	VDE1016	VDE1015	VDE1014	VDE1013	VDE1012	VDE1011	VDE1010	VDE1009	VDE1008	VDE1007	VDE1006	VDE1005	VDE1004	VDE1003	VDE1002	VDE1001	VDE1000	VDE999	VDE998	VDE997	VDE996	VDE995	VDE994	VDE993	VDE992	VDE991	VDE990	VDE989	VDE988	VDE987	VDE986	VDE985	VDE984	VDE983	VDE982	VDE981	VDE980	VDE979	VDE978	VDE977	VDE976	VDE975	VDE974	VDE973	VDE972	VDE971	VDE970	VDE969	VDE968	VDE967	VDE966	VDE965	VDE964	VDE963	VDE962	VDE961	VDE960	VDE959	VDE958	VDE957	VDE956	VDE955	VDE954	VDE953	VDE952	VDE951	VDE950	VDE949	VDE948	VDE947	VDE946	VDE945	VDE944	VDE943	VDE942	VDE941	VDE940	VDE939	VDE938	VDE937	VDE936	VDE935	VDE934	VDE933	VDE932	VDE931	VDE930	VDE929	VDE928	VDE927	VDE926	VDE925	VDE924	VDE923	VDE922	VDE921	VDE920	VDE919	VDE918	VDE917	VDE916	VDE915	VDE914	VDE913	VDE912	VDE911	VDE910	VDE909	VDE908	VDE907	VDE906	VDE905	VDE904	VDE903	VDE902	VDE901	VDE900	VDE899	VDE898	VDE897	VDE896	VDE895	VDE894	VDE893	VDE892	VDE891	VDE890	VDE889	VDE888	VDE887	VDE886	VDE885	VDE884	VDE883	VDE882	VDE881	VDE880	VDE879	VDE878	VDE877	VDE876	VDE875	VDE874	VDE873	VDE872	VDE871	VDE870	VDE869	VDE868	VDE867	VDE866	VDE865	VDE864	VDE863	VDE862	VDE861	VDE860	VDE859	VDE858	VDE857	VDE856	VDE855	VDE854	VDE853	VDE852	VDE851	VDE850	VDE849	VDE848	VDE847	VDE846	VDE845	VDE844	VDE843	VDE842	VDE841	VDE840	VDE839	VDE838	VDE837	VDE836	VDE835	VDE834	VDE833	VDE832	VDE831	VDE830	VDE829	VDE828	VDE827	VDE826	VDE825	VDE824	VDE823	VDE822	VDE821	VDE820	VDE819	VDE818	VDE817	VDE816	VDE815	VDE814	VDE813	VDE812	VDE811	VDE810	VDE809	VDE808	VDE807	VDE806	VDE805	VDE804	VDE803	VDE802	VDE801	VDE800	VDE799	VDE798	VDE797	VDE796	VDE795	VDE794	VDE793	VDE792	VDE791	VDE790	VDE789	VDE788	VDE787	VDE786	VDE785	VDE784	VDE783	VDE782	VDE781	VDE780	VDE779	VDE778	VDE777	VDE776	VDE775	VDE774	VDE773	VDE772	VDE771	VDE770	VDE769	VDE768	VDE767	VDE766	VDE765	VDE764	VDE763	VDE762	VDE761	VDE760	VDE759	VDE758	VDE757	VDE756	VDE755	VDE754	VDE753	VDE752	VDE751	VDE750	VDE749	VDE748	VDE747	VDE746	VDE745	VDE744	VDE743	VDE742	VDE741	VDE740	VDE739	VDE738	VDE737	VDE736	VDE735	VDE734	VDE733	VDE732	VDE731	VDE730	VDE729	VDE728	VDE727	VDE726	VDE725	VDE724	VDE723	VDE722	VDE721	VDE720	VDE719	VDE718	VDE717	VDE716	VDE715	VDE714	VDE713	VDE712	VDE711	VDE710	VDE709	VDE708	VDE707	VDE706	VDE705	VDE704	VDE703	VDE702	VDE701	VDE700	VDE699	VDE698	VDE697	VDE696	VDE695	VDE694	VDE693	VDE692	VDE691	VDE690	VDE689	VDE688	VDE687	VDE686	VDE685	VDE684	VDE683	VDE682	VDE681	VDE680	VDE679	VDE678	VDE677	VDE676	VDE675	VDE674	VDE673	VDE672	VDE671	VDE670	VDE669	VDE668	VDE667	VDE666	VDE665	VDE664	VDE663	VDE662	VDE661	VDE660	VDE659	VDE658	VDE657	VDE656	VDE655	VDE654	VDE653	VDE652	VDE651	VDE650	VDE649	VDE648	VDE647	VDE646	VDE645	VDE644	VDE643	VDE642	VDE641	VDE640	VDE639	VDE638	VDE637	VDE636	VDE635	VDE634	VDE633	VDE632	VDE631	VDE630	VDE629	VDE628	VDE627	VDE626	VDE625	VDE624	VDE623	VDE622	VDE621	VDE620	VDE619	VDE618	VDE617	VDE616	VDE615	VDE614	VDE613	VDE612	VDE611	VDE610	VDE609	VDE608	VDE607	VDE606	VDE605	VDE604	VDE603	VDE602	VDE601	VDE600	VDE599	VDE598	VDE597	VDE596	VDE595	VDE594	VDE593	VDE592	VDE591	VDE590	VDE589	VDE588	VDE587	VDE586	VDE585	VDE584	VDE583	VDE582	VDE581	VDE580	VDE579	VDE578	VDE577	VDE576	VDE575	VDE574	VDE573	VDE572	VDE571	VDE570	VDE569	VDE568	VDE567	VDE566	VDE565	VDE564	VDE563	VDE562	VDE561	VDE560	VDE559	VDE558	VDE557	VDE556	VDE555	VDE554	VDE553	VDE552	VDE551	VDE550	VDE549	VDE548	VDE547	VDE546	VDE545	VDE544	VDE543	VDE542	VDE541	VDE540	VDE539	VDE538	VDE537	VDE536	VDE535	VDE534	VDE533	VDE532	VDE531	VDE530	VDE529	VDE528	VDE527	VDE526	VDE525	VDE524	VDE523	VDE522	VDE521	VDE520	VDE519	VDE518	VDE517	VDE516	VDE515	VDE514	VDE513	VDE512	VDE511	VDE510	VDE509	VDE508	VDE507	VDE506	VDE505	VDE504	VDE503	VDE502	VDE501	VDE500	VDE499	VDE498	VDE497	VDE496	VDE495	VDE494	VDE493	VDE492	VDE491	VDE490	VDE489	VDE488	VDE487	VDE486	VDE485	VDE484	VDE483	VDE482	VDE481	VDE480	VDE479	VDE478	VDE477	VDE476	VDE475	VDE474	VDE473	VDE472	VDE471	VDE470	VDE469	VDE468	VDE467	VDE466	VDE465	VDE464	VDE463	VDE462	VDE461	VDE460	VDE459	VDE458	VDE457	VDE456	VDE455	VDE454	VDE453	VDE452	VDE451	VDE450	VDE449	VDE448	VDE447	VDE446	VDE445	VDE444	VDE443	VDE442	VDE441	VDE440	VDE439	VDE438	VDE437	VDE436	VDE435	VDE434	VDE433	VDE432	VDE431	VDE430	VDE429	VDE428	VDE427	VDE426	VDE425	VDE424	VDE423	VDE422	VDE421	VDE420	VDE419	VDE418	VDE417	VDE416	VDE415	VDE414	VDE413	VDE412	VDE411	VDE410	VDE409	VDE408	VDE407	VDE406	VDE405	VDE404	VDE403	VDE402	VDE401	VDE400	VDE399	VDE398	VDE397	VDE396	VDE395	VDE394	VDE393	VDE392	VDE391	VDE390	VDE389	VDE388	VDE387	VDE386	VDE385	VDE384	VDE383	VDE382	VDE381	VDE380	VDE379	VDE378	VDE377	VDE376	VDE375	VDE374	VDE373	VDE372	VDE371	VDE370	VDE369	VDE368	VDE367	VDE366	VDE365	VDE364	VDE363	VDE362	VDE361	VDE360	VDE359	VDE358	VDE357	VDE356	VDE355	VDE354	VDE353	VDE352	VDE351	VDE350	VDE349	VDE348	VDE347	VDE346	VDE345	VDE344	VDE343	VDE342	VDE341	VDE340	VDE339	VDE338	VDE337	VDE336	VDE335	VDE334	VDE333	VDE332	VDE331	VDE330	VDE329	VDE328	VDE327	VDE326	VDE325	VDE324	VDE323	VDE322	VDE321	VDE320	VDE319	VDE318	VDE317	VDE316	VDE315	VDE314	VDE313	VDE312	VDE311	VDE310	VDE309	VDE308	VDE307	VDE306	VDE305	VDE304	VDE303	VDE302	VDE301	VDE300	VDE299	VDE298	VDE297	VDE296	VDE295	VDE294	VDE293	VDE292	VDE291	VDE290	VDE289	VDE288	VDE287	VDE286	VDE285	VDE284	VDE283	VDE282	VDE281	VDE280	VDE279	VDE278	VDE277	VDE276	VDE275	VDE274	VDE273	VDE272	VDE271	VDE270	VDE269	VDE268	VDE267	VDE266	VDE265	VDE264	VDE263	VDE262	VDE261	VDE260	VDE259	VDE258	VDE257	VDE256	VDE255	VDE254	VDE253	VDE252	VDE251	VDE250	VDE249	VDE248	VDE247	VDE246	VDE245	VDE244	VDE243	VDE242	VDE241	VDE240	VDE239	VDE238	VDE237	VDE236	VDE235	VDE234	VDE233	VDE232	VDE231	VDE230	VDE229	VDE228	VDE227	VDE226	VDE225	VDE224	VDE223	VDE222	VDE221	VDE220	VDE219	VDE218	VDE217	VDE216	VDE215	VDE214	VDE213	VDE212	VDE211	VDE210	VDE209	VDE208	VDE207	VDE206	VDE205	VDE204	VDE203	VDE202	VDE201	VDE200	VDE199	VDE198	VDE197	VDE196	VDE195	VDE194	VDE193	VDE192	VDE191	VDE190	VDE189	VDE188	VDE187	VDE186	VDE185	VDE184	VDE183	VDE182	VDE181	VDE180	VDE179	VDE178	VDE177	VDE176	VDE175	VDE174	VDE173	VDE172	VDE171	VDE170	VDE169	VDE168	VDE167	VDE166	VDE165	VDE164	VDE163	VDE162	VDE161	VDE160	VDE159	VDE158	VDE157	VDE156	VDE155	VDE154	VDE153	VDE152	VDE151	VDE150	VDE149	VDE148	VDE147	VDE146	VDE145	VDE144	VDE143	VDE142	VDE141	VDE140	VDE139	VDE138	VDE137	VDE136	VDE135	VDE134	VDE133	VDE132	VDE131	VDE130	VDE129	VDE128	VDE127	VDE126	VDE125	VDE124	VDE123	VDE122	VDE121	VDE120	VDE119	VDE118	VDE117	VDE116	VDE115	VDE114	VDE113	VDE112	VDE111	VDE110	VDE109	VDE108	VDE107	VDE106	VDE105	VDE104	VDE103	VDE102	VDE101	VDE100	VDE99	VDE98	VDE97	VDE96	VDE95	VDE94	VDE93	VDE92	VDE91	VDE90	VDE89	VDE88	VDE87	VDE86	VDE85	VDE84	VDE83	VDE82	VDE81	VDE80	VDE79	VDE78	VDE77	VDE76	VDE75	VDE74	VDE73	VDE72	VDE71	VDE70	VDE69	VDE68	VDE67	VDE66	VDE65	VDE64	VDE63	VDE62	VDE61	VDE60	VDE59	VDE58	VDE57	VDE56	VDE55	VDE54	VDE53	VDE52	VDE51	VDE50	VDE49	VDE48	VDE47	VDE46	VDE45	VDE44	VDE43	VDE42	VDE41	VDE40	VDE39	VDE38	VDE37	VDE36	VDE35	VDE34	VDE33	VDE32	VDE31	VDE30	VDE29	VDE28	VDE27	VDE26	VDE25	VDE24	VDE23	VDE22	VDE21	VDE20	VDE19	VDE18	VDE17	VDE16	VDE15	VDE14	VDE13	VDE12	VDE11	VDE10	VDE9	VDE8	VDE7	VDE6	VDE5	VDE4	VDE3	VDE2	VDE1	VDE0
Processor	VDE1122	VDE1121	VDE1120	VDE1119	VDE1118	VDE1117	VDE1116	VDE1115	VDE1114	VDE1113	VDE1112	VDE1111	VDE1110	VDE1109	VDE1108	VDE1107	VDE1106	VDE1105	VDE1104	VDE1103	VDE1102	VDE1101	VDE1100	VDE1099	VDE1098	VDE1097	VDE1096	VDE1095	VDE1094	VDE1093	VDE1092	VDE1091	VDE1090	VDE1089	VDE1088	VDE1087	VDE1086	VDE1085	VDE1084	VDE1083	VDE1082	VDE1081	VDE1080	VDE1079	VDE1078	VDE1077	VDE1076	VDE1075	VDE1074	VDE1073	VDE1072	VDE1071	VDE1070	VDE1069	VDE1068	VDE1067	VDE1066	VDE1065	VDE1064	VDE1063	VDE1062	VDE1061	VDE1060	VDE1059	VDE1058	VDE1057	VDE1056	VDE1055	VDE1054	VDE1053	VDE1052	VDE1051	VDE1050	VDE1049	VDE1048	VDE1047	VDE1046	VDE1045	VDE1044	VDE1043	VDE1042	VDE1041	VDE1040	VDE1039	VDE1038	VDE1037	VDE1036	VDE1035	VDE1034	VDE1033	VDE1032	VDE1031	VDE1030	VDE1029	VDE1028	VDE1027	VDE1026	VDE1025	VDE1024	VDE1023	VDE1022	VDE1021	VDE1020	VDE1019	VDE1018	VDE1017	VDE1016	VDE1015	VDE1014	VDE1013	VDE1012	VDE1011	VDE1010	VDE1009	VDE1008	VDE1007	VDE1006	VDE1005	VDE1004	VDE1003	VDE1002	VDE1001	VDE1000	VDE999	VDE998	VDE997	VDE996	VDE995	VDE994	VDE993	VDE992	VDE991	VDE990	VDE989	VDE988	VDE987	VDE986	VDE985	VDE984	VDE983	VDE982	VDE981	VDE980	VDE979	VDE978	VDE977	VDE976	VDE975	VDE974	VDE973	VDE972	VDE971	VDE970	VDE969	VDE968	VDE967	VDE966	VDE965	VDE964	VDE963	VDE962	VDE961	VDE960	VDE959	VDE958	VDE957	VDE956	VDE955	VDE954	VDE953	VDE952	VDE951	VDE950	VDE949	VDE948	VDE947	VDE946	VDE945	VDE944	VDE943	VDE942	VDE941	VDE940	VDE939	VDE938	VDE937	VDE936	VDE935	VDE934	VDE933	VDE932	VDE931	VDE930	VDE929	VDE928	VDE927	VDE926	VDE925	VDE924	VDE923	VDE922	VDE921	VDE920	VDE919	VDE918	VDE917	VDE916	VDE915	VDE914	VDE913	VDE912	VDE911	VDE910	VDE909	VDE908	VDE907	VDE906	VDE905	VDE904	VDE903	VDE902	VDE901	VDE900	VDE899	VDE898	VDE897	VDE896	VDE895	VDE894	VDE893	VDE892	VDE891	VDE890	VDE889	VDE888	VDE887																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							

SECTION 3

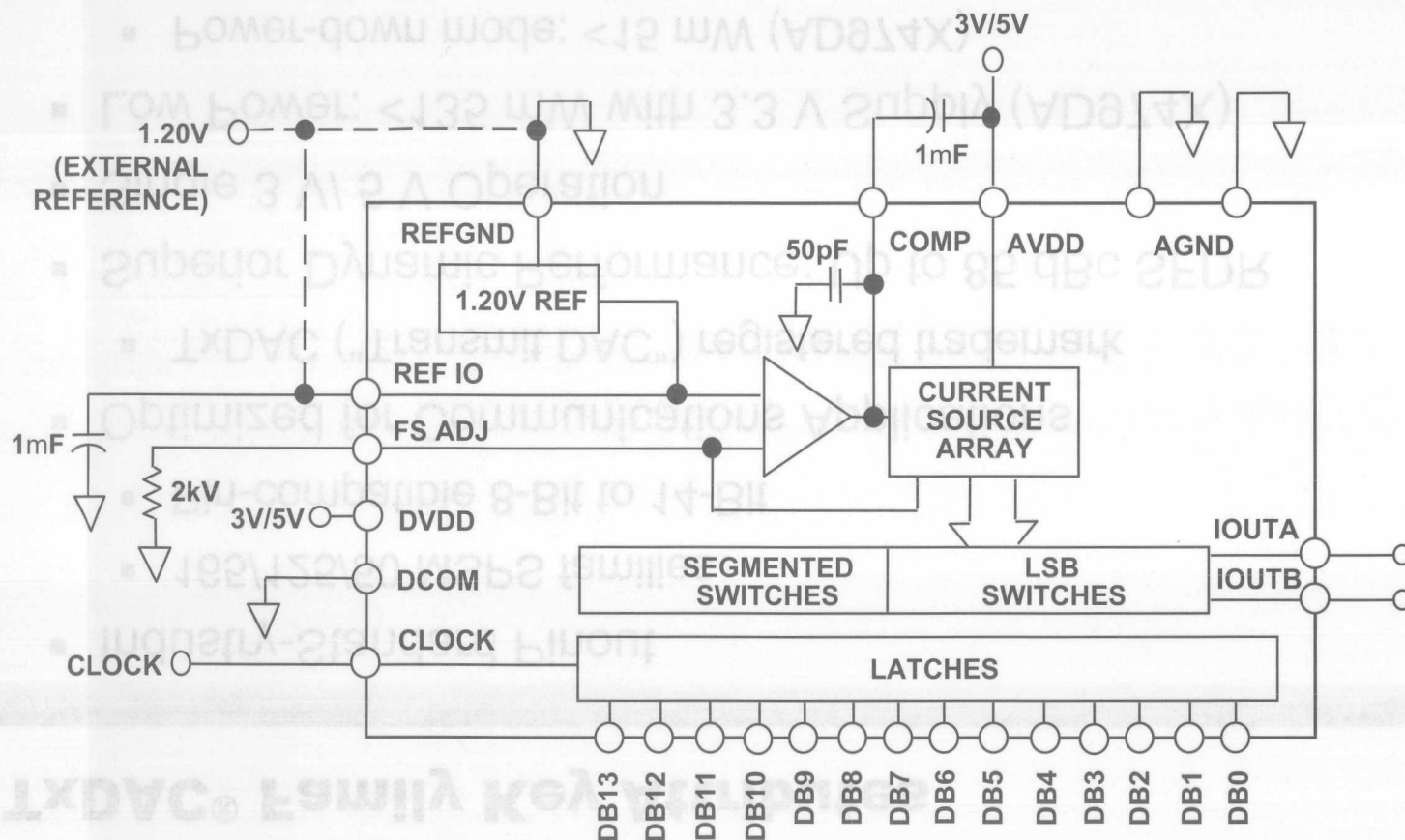
Digital-to-Analog Converters

High-Speed DACs
General-Purpose DACs
Digital Potentiometers

High-Speed DACs

SECTION 3

TxDAC[®] Family



TxDAC® Family Key Attributes

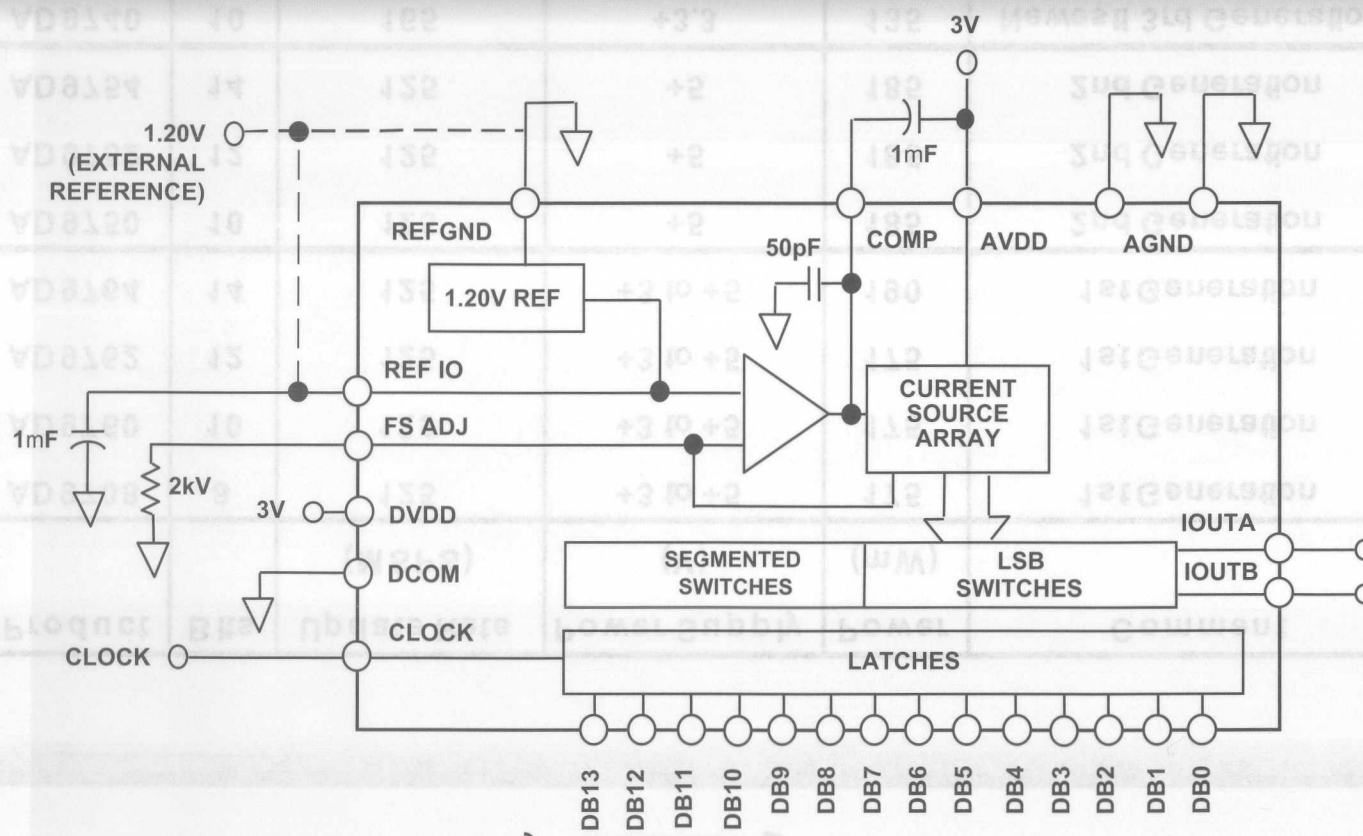
- Industry-Standard Pinout
 - 165/125/50 MSPS families
 - Pin-compatible 8-Bit to 14-Bit
- Optimized for Communications Applications
 - TxDAC (“Transmit DAC”) registered trademark
- Superior Dynamic Performance: Up to 85 dBc SFDR
- Single 3 V/ 5 V Operation
- Low Power: <135 mW with 3.3 V Supply (AD974X)
 - Power-down mode: <15 mW (AD974X)
- Small 28-Lead SOIC/TSSOP Packaging

The “Transmit DAC” Family at a Glance...

Product	Bits	Update Rate (MSPS)	Power Supply (V)	Power (mW)	Comment
AD9708	8	125	+3 to +5	175	1st Generation
AD9760	10	125	+3 to +5	175	1st Generation
AD9762	12	125	+3 to +5	175	1st Generation
AD9764	14	125	+3 to +5	190	1st Generation
AD9750	10	125	+5	185	2nd Generation
AD9752	12	125	+5	185	2nd Generation
AD9754	14	125	+5	185	2nd Generation
AD9740	10	165	+3.3	135	Newest! 3rd Generation
AD9742	12	165	+3.3	135	Newest! 3rd Generation
AD9744	14	165	+3.3	135	Newest! 3rd Generation

AD9740/42/44

10-/12-/14-Bit 165 MSPS TxDAC DAC



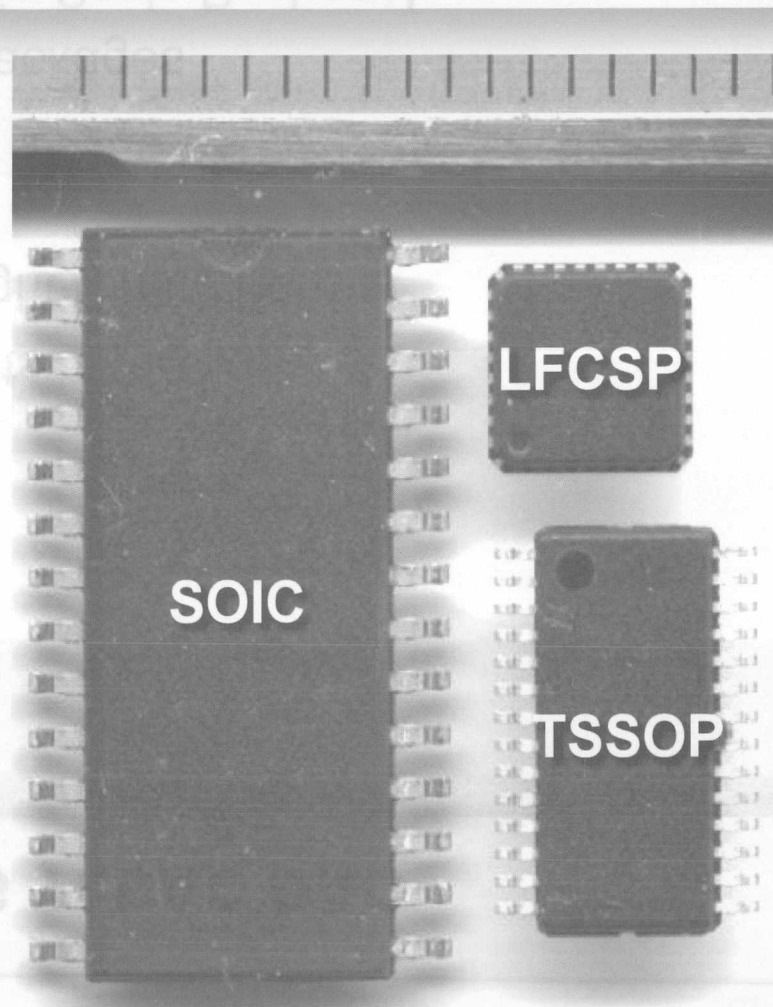
AD9740 – 10-BIT
AD9742 – 12-BIT
AD9744 – 14-BIT

AD9740/42/44 10-/12-/14-Bit 165 MSPS TxDAC DAC

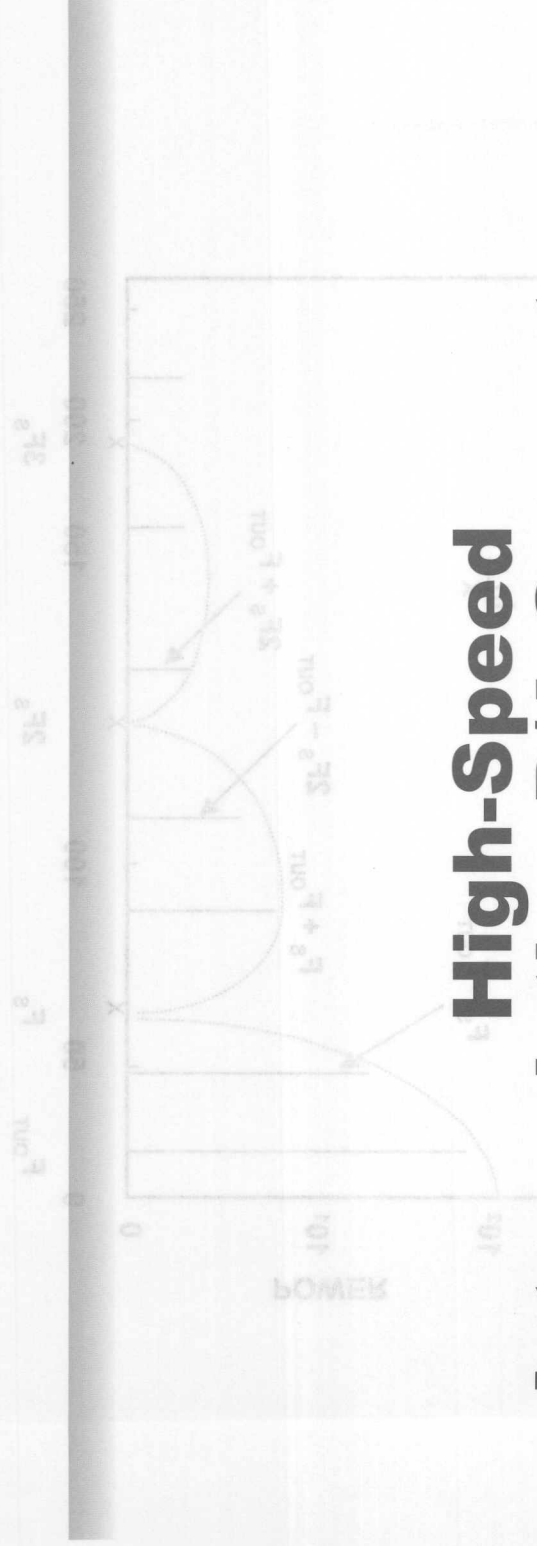
- SFDR Up to 40 MHz:
 - 67 dBc (AD9740)
 - 70 dBc (AD9742)
 - 73 dBc (AD9744)
- Single-Ended Clock Input
- 3 V-Compatible CMOS Inputs
- Two's Complement or Straight Binary Format
- Single 3.3 V Supply
- 135 mW Power Dissipation
- 28-Lead SOIC or TSSOP Packages
- **Coming Soon: 32-Lead Chip-Scale Package!**

TxDAC Family in 32-Lead Chip-Scale Package (LFCSP)

- SOIC
 - 192.77 mm²
- TSSOP
 - 63.7 mm²
 - 67% Smaller than SOIC
- LFCSP
 - 5.00 mm x 5.00 mm = 25 mm²
 - 60% Smaller than TSSOP!
 - 87% Smaller than SOIC!!



In the above example, $F_{out} = 0.353 F_s$



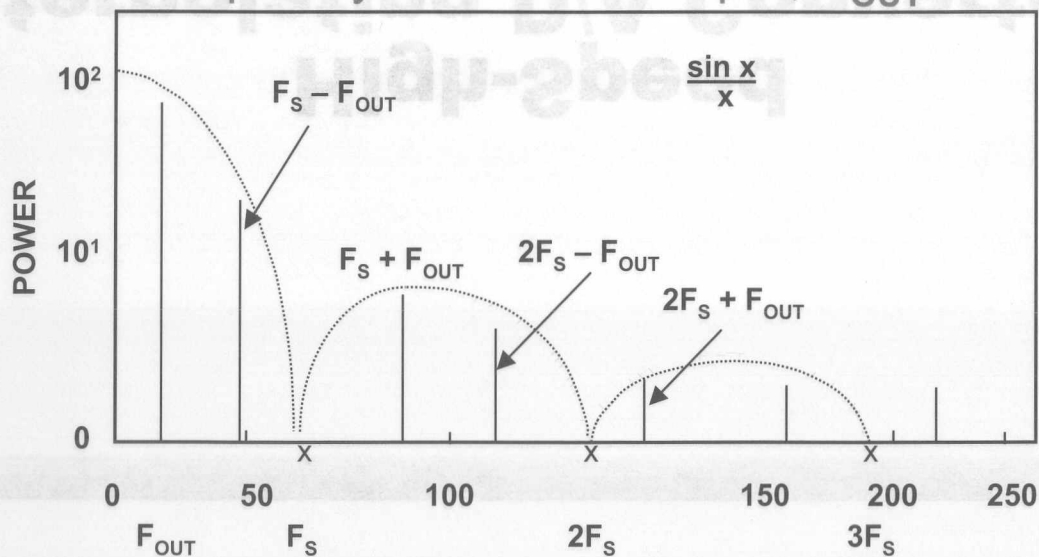
High-Speed Interpolating D/A Converters

Theory that are multiples of the clock or sampling (similar to "aliasing" in an ADC) remember Nyquist The output of a reconstruction DAC contains "images."

DAC images

DAC Images

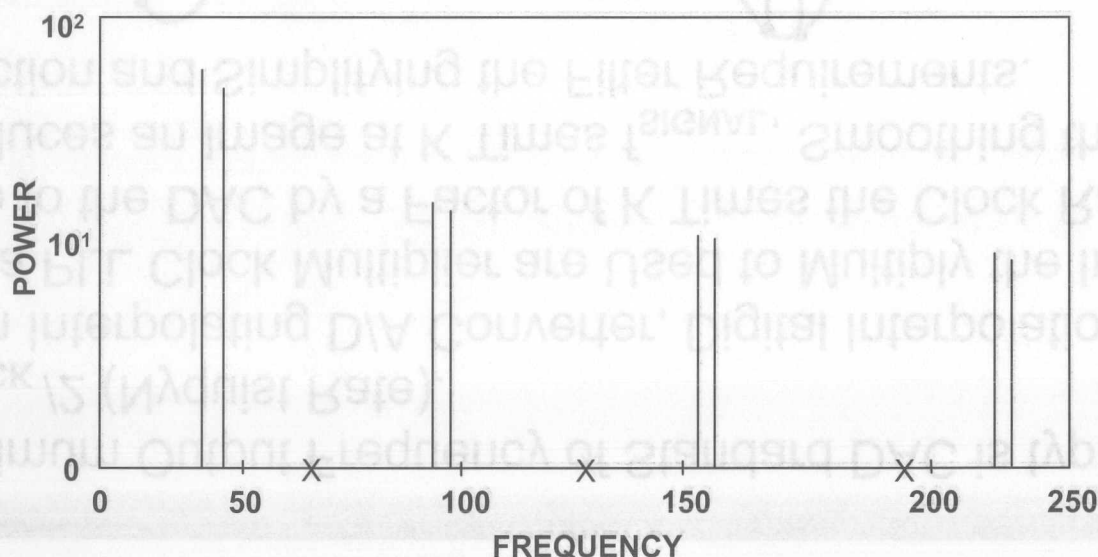
The output of a reconstruction DAC contains “images” (similar to “aliasing” in an ADC ... remember Nyquist Theory?) that are multiples of the clock or sampling frequency \pm the DAC output, F_{OUT} .



In the above example, $F_{OUT} = 0.293 F_S$

DAC Images (continued)

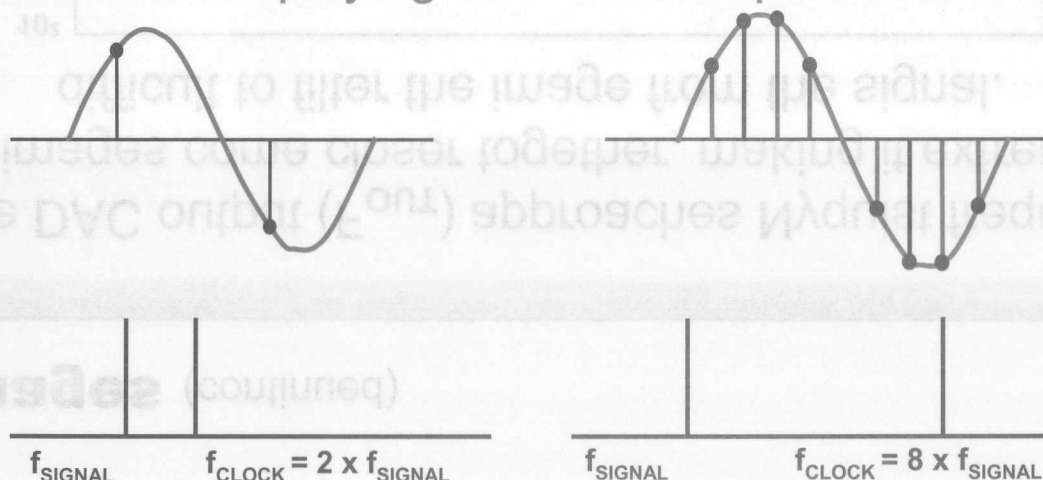
As the DAC output (F_{OUT}) approaches Nyquist frequency, the images come closer together, making it extremely difficult to filter the image from the signal.



In the above example, $F_{OUT} = 0.453 F_s$

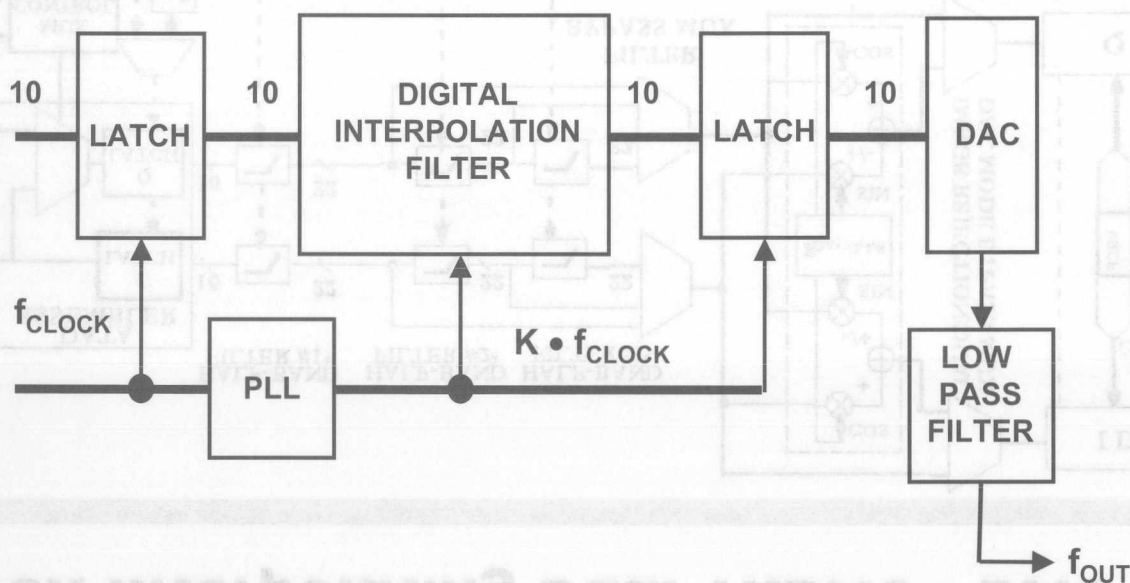
Interpolation

- Maximum Output Frequency of Standard DAC is typically $f_{\text{CLOCK}}/2$ (Nyquist Rate).
- In an Interpolating D/A Converter, Digital Interpolation Filters and a PLL Clock Multiplier are Used to Multiply the Input Data Rate to the DAC by a Factor of K Times the Clock Rate. This Produces an Image at K Times f_{SIGNAL} , Smoothing the Sine Function and Simplifying the Filter Requirements.

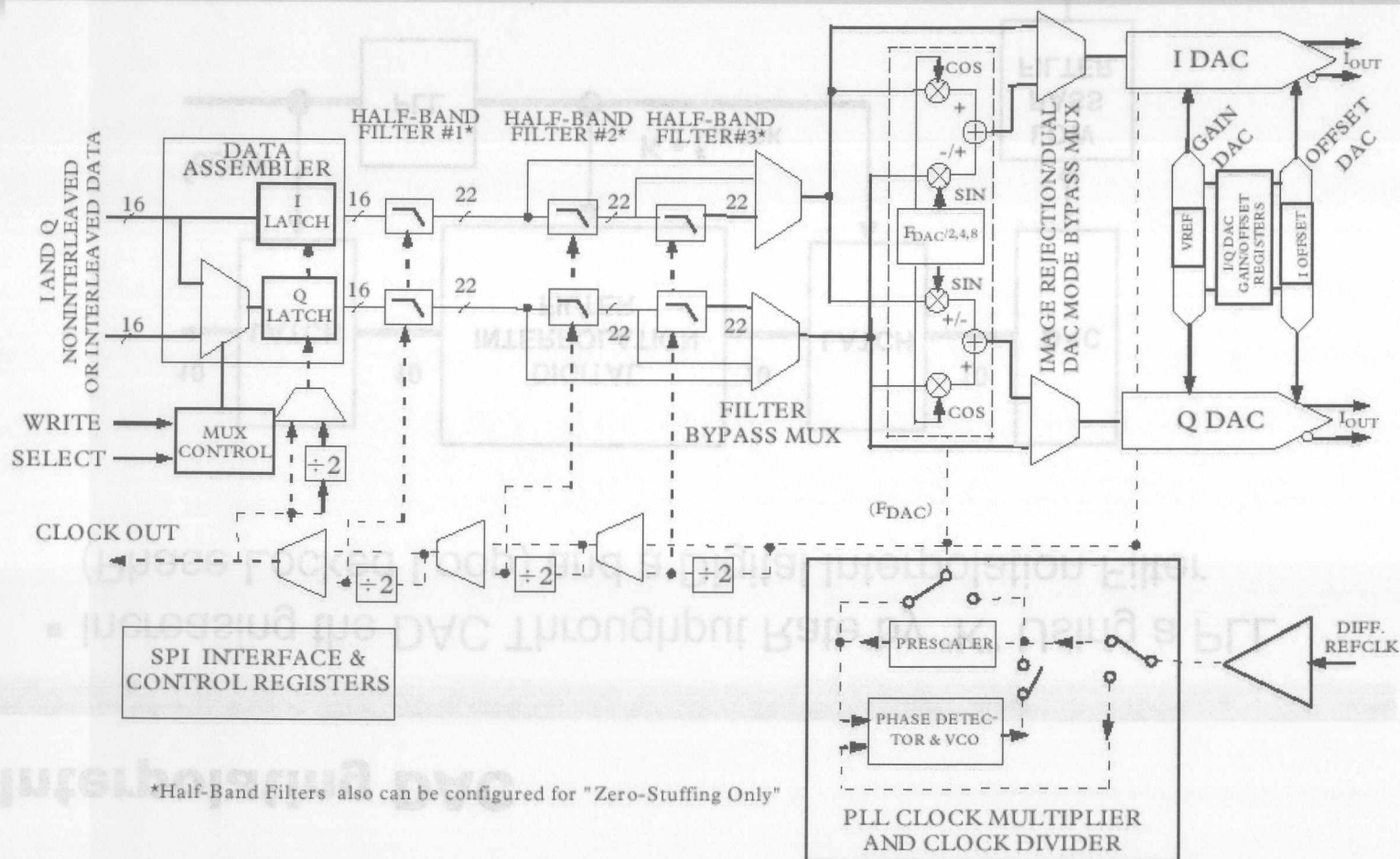


Interpolating DAC

- Increasing the DAC Throughput Rate by “K” Using a PLL (Phase Locked Loop) and a Digital Interpolation Filter



AD9773/75/77 12-/14-/16-Bit 160 MSPS 2x/4x/8x Interpolating Dual TxDAC+ DAC



AD9773/75/77 12-/14-/16-Bit 160 MSPS 2x/4x/8x Interpolating Dual TxDAC+ DAC

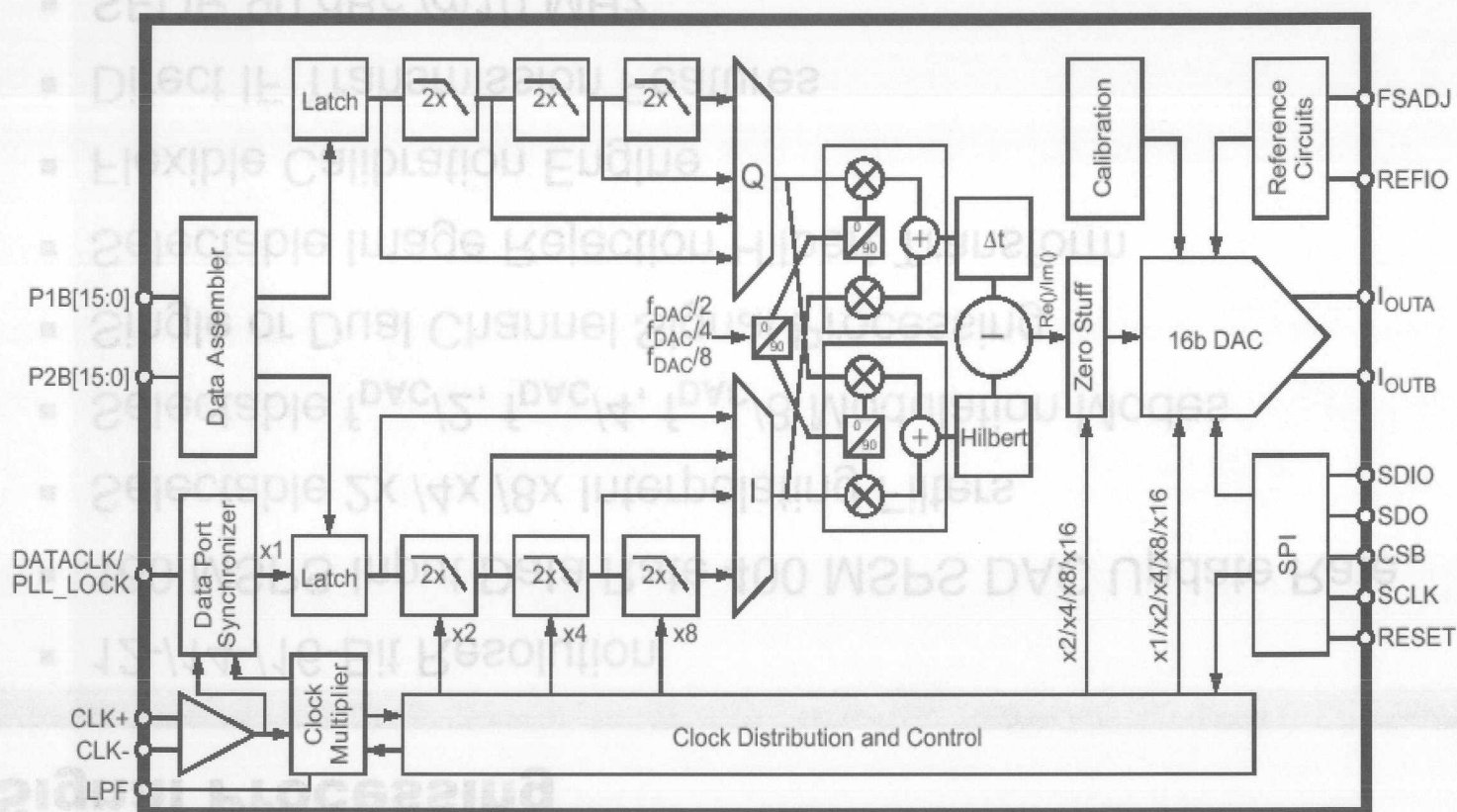
- Digital Complex Modulation Capability
 - $F_s/8$, $F_s/4$, $F_s/2$
 - Enables single sideband “Direct to RF” architectures
- 160 MSPS Input Data Rate, 400 MSPS DAC Update Rate
- Selectable Interpolation Rates (2X, 4X, 8X)
- Programmable Channel Gain and Offset Adjustment
- Direct IF Transmission Mode for 70 MHz + IFs
- Internal PLL Clock Multiplier
- Selectable Internal Clock Divider
- Versatile Clock Input
 - Differential/single-ended
 - Sine wave or CMOS/LVPECL-compatible

AD9773/75/77 12-/14-/16-Bit 165/400 MSPS 2x/4x/8x Interpolating Dual TxDAC+ DAC

- Excellent AC Performance
 - IMD: 80 dB @ 2 MHz–30 MHz
 - WCDMA ACPR: 71 dB @ IF = 71 MHz
- Fully Compatible SPI Port
- Versatile Data Interfaces
 - Two's complement/straight binary data coding
 - Dual-port or single-port interleaved data
- Single 3.3 V Supply
- 1.2 W Typical Power Dissipation
- 80-Lead TQFP Package

AD9782/84/86 12-/14-/16-Bit 160 MSPS TxDAC+® with 2x/4x/8x Interpolation and Signal Processing

3-18



AD9782/84/86 12-/14-/16-Bit 160 MSPS TxDAC+® with 2x/4x/8x Interpolation and Signal Processing

- 12-/14-/16-Bit Resolution
- 160 MSPS Input Data Rate 400 MSPS DAC Update Rate
- Selectable 2x /4x /8x Interpolating Filters
- Selectable $f_{\text{DAC}}/2$, $f_{\text{DAC}}/4$, $f_{\text{DAC}}/8$ Modulation Modes
- Single or Dual Channel Signal Processing
- Selectable Image Rejection Hilbert Transform
- Flexible Calibration Engine
- Direct IF Transmission Features
- SFDR 90 dBc @10 MHz
- W-CDMA ACLR = 75 dB
- DNL < ± 1 LSBs

AD9782/84/86 12-/14-/16-Bit 160 MSPS TxDAC+® with 2x/4x/8x Interpolation and Signal Processing

- Power Dissipation ~ 1 W
- 3.3 V Analog, 2.5 V Digital Supply
- 3.3 V Compatible Digital Interface
- On-Chip 1.2 V Reference
- Serial Control Interface
- Versatile Clock and Data Interface
- 80-Lead LQFP

General-Purpose DACs

AD53xx Family MicroPower DAC

Features of the AD53xx Family Include...

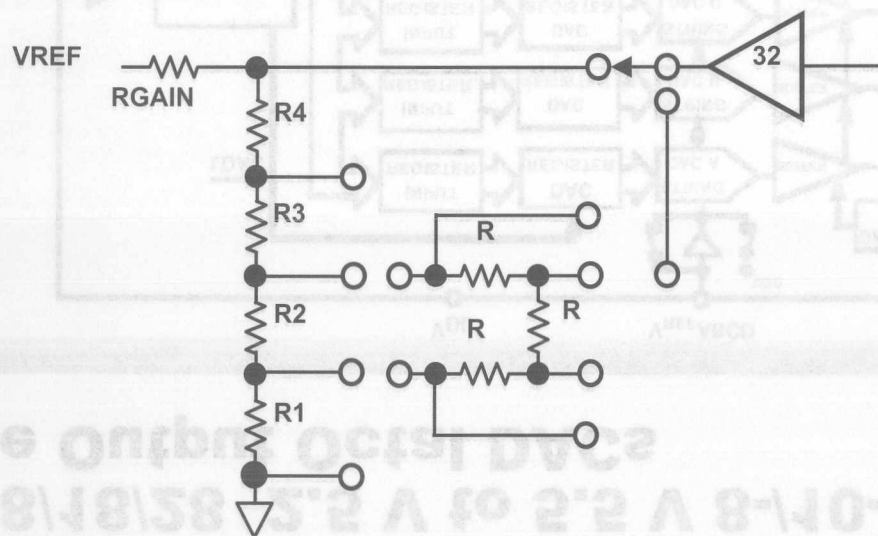
- Over 30 models from which to choose
- 8-, 10-, or 12-bit resolution
- Single, dual, and quad versions
- Versatile 3-wire, high-speed serial interface:
 - 30 MHz clock rates, Schmitt-Triggered
 - SPI, QSPI, and MICROWIRE-compatible
- 2-wire I²C interface: 400 kHz
- Parallel interface

AD53xx Family Features (continued)

- True Rail-to-Rail Output Performance:
 - 0 V to V_{REF} or 0 V to $2 \times V_{REF}$
- Low Power, Single 3 V/5 V Operation
- Power-On Reset to Zero
- Software-Selectable Output Loads During Power-Down
- -40°C to $+105^{\circ}\text{C}$ Temperature Range
- Pin-to-Pin Compatibility (Serial-Serial or Parallel-Parallel)

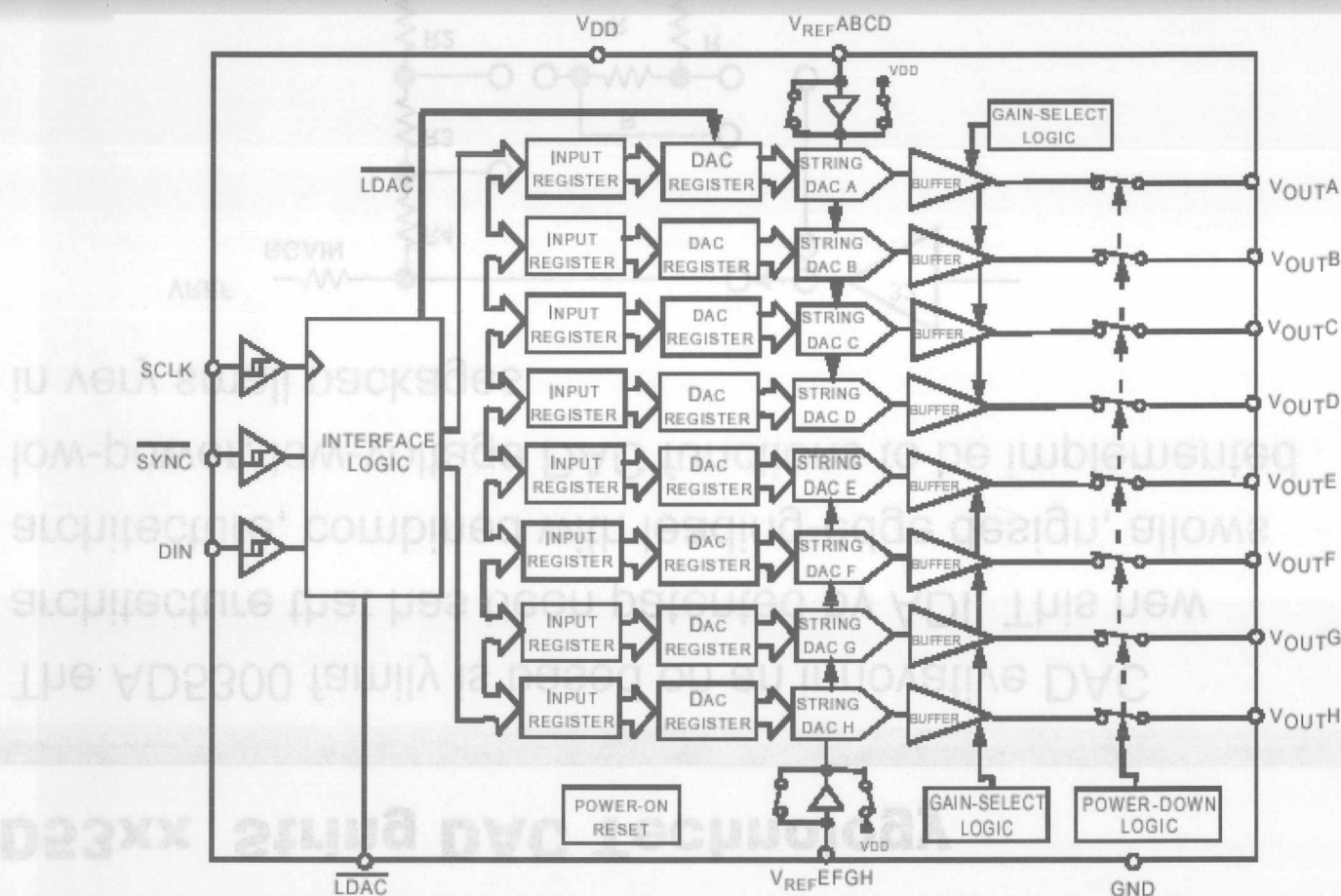
AD53xx String DAC Technology

The AD5300 family is based on an innovative DAC architecture that has been patented by ADI. This new architecture, combined with leading-edge design, allows low-power, low-voltage DAC functions to be implemented in very small packages.



U.S. Patent: 5,969,657

AD5308/18/28 2.5 V to 5.5 V 8-/10-/12-Bit Voltage Output Octal DACs



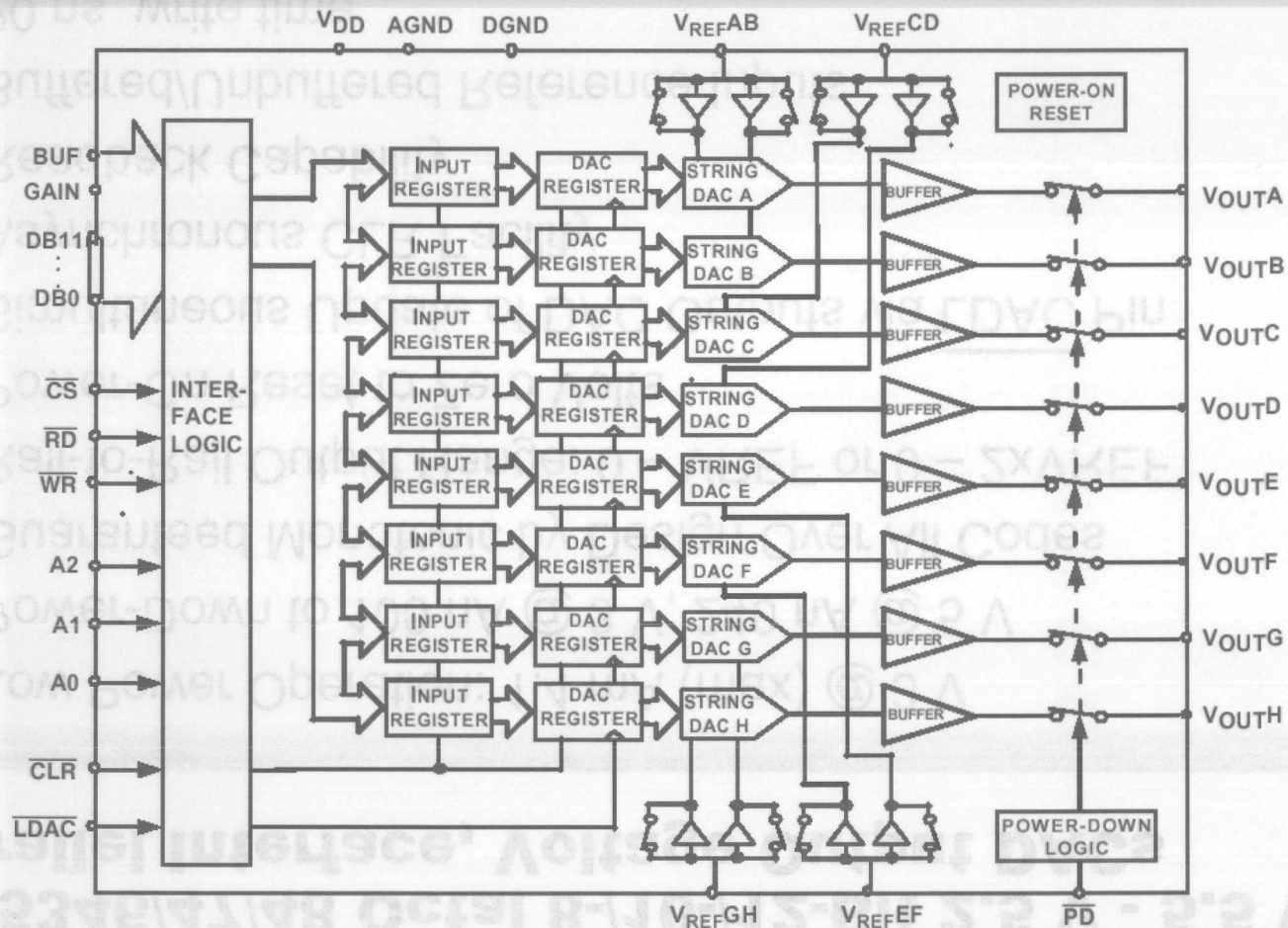
AD5308/18/28 2.5 V to 5.5 V 8-/10-/12-Bit Voltage Output Octal DACs

- AD5308: Eight Buffered 8-Bit DACs in 16-Lead TSSOP
- AD5318: Eight Buffered 10-Bit DACs in 16-Lead TSSOP
- AD5328: Eight Buffered 12-Bit DACs in 16-Lead TSSOP
- Guaranteed Monotonic By Design over All Codes
- Buffered/ Unbuffered/ V_{DD} Reference Input Options
- Output Range: $0 - V_{REF}$ or $0 - 2 V_{REF}$
- Power-On-Reset to Zero Volts
- On-Chip Rail-to-Rail Output Buffer Amplifiers
- Temperature Range -40°C to $+105^{\circ}\text{C}$

AD5308/18/28 2.5 V to 5.5 V 8-/10-/12-Bit Voltage Output Octal DACs

- Low Power Operation: 1.4 mA (Max) @ 3 V
- 2.5 V to 5.5 V Power Supply
- Power-Down to 120 nA @ 3 V, 400 nA @ 5 V
- Double-Buffered Input Logic
- Programmability
- Individual-Channel Powerdown
- Simultaneous Update of Outputs (LDAC Pin)
- Low Power, SPI™, QSPI™, MICROWIRE™, and DSP-Compatible 3-Wire Serial Interface

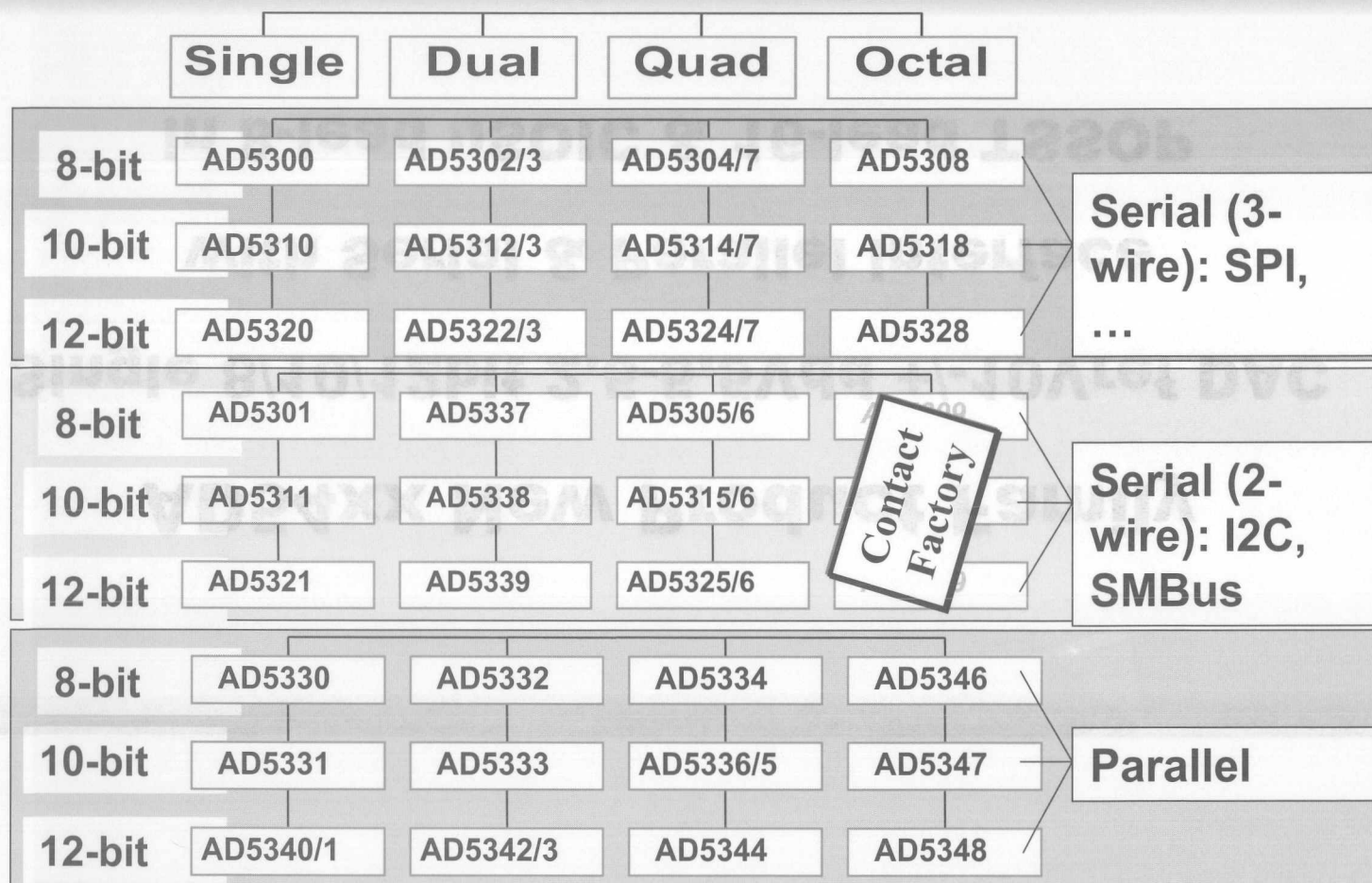
AD5346/47/48 Octal 8-/10-/12-Bit 2.5 V - 5.5 V Parallel Interface, Voltage Output DACs



AD5346/47/48 Octal 8-/10-/12-Bit 2.5 V - 5.5 V, Parallel Interface, Voltage Output DACs

- Low Power Operation: 1.4 mA (max) @ 3 V
- Power-Down to 100 nA @ 3 V, 240 nA @ 5 V
- Guaranteed Monotonic by Design Over All Codes
- Rail-to-Rail Output Range: 0 – VREF or 0 – 2xVREF
- Power-On Reset to Zero Volts
- Simultaneous Update of DAC Outputs via LDAC Pin
- Asynchronous CLR Facility
- Readback Capability
- Buffered/Unbuffered Reference Inputs
- 20 ns write time
- 38-lead TSSOP/6 mm x 6 mm 40-lead CSP Packaging
- Temperature Range: –40° C to +105° C

AD53xx Selector



AD54xx New Product Family
Single 8/10/12bit 2.5-5.5V_{dd} +/-10V_{ref} DAC
with Serial & Parallel interface
in 8-lead uSOIC & 16-lead TSSOP

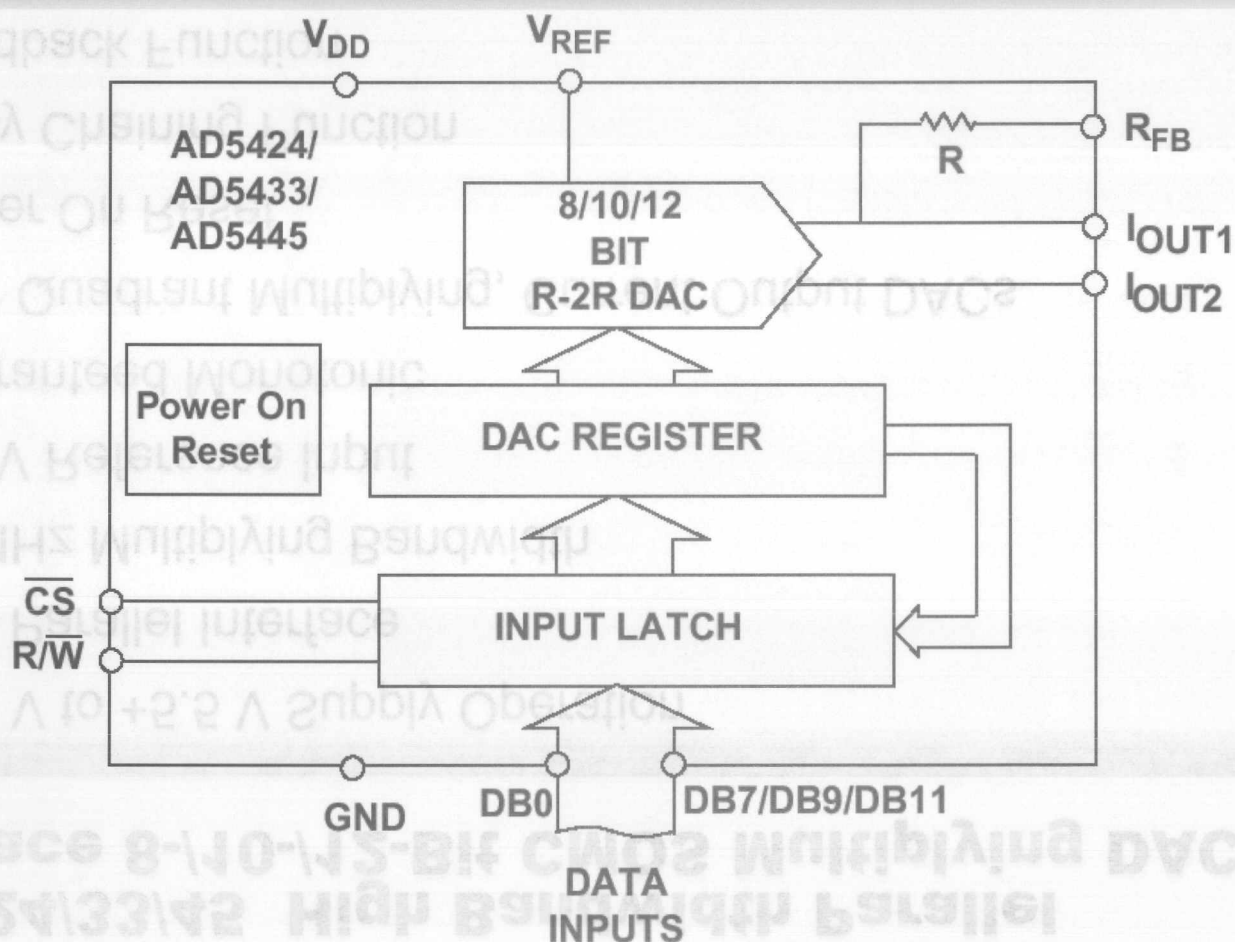
AD54xx Current Output DACs

- FAST 10MHz Multiplying Bandwidth
- 25MHz Update rate
- Pin & Software compatible 8-/10-/12-Bit
- SMALL 8-lead μ SOIC, 16-lead TSSOP
- SERIAL & PARALLEL
- PINNED-OUT Internal Nodes/ Resistors
- Low Voltage / Single Supply with ± 10 V Vref

AD54xx Current Output DAC Selector

Generic	# bits	Interface	package, leads	comment
AD5426	8	Serial	MSOP, 10	
AD5425	8	Serial	MSOP, 10	fast 8 bit load
AD5432	10	Serial	MSOP, 10	
AD5443	12	Serial	MSOP, 10	
AD5424	8	Parallel	TSSOP, 16	
AD5433	10	Parallel	TSSOP, 20	
AD5445	12	Parallel	TSSOP, 20	

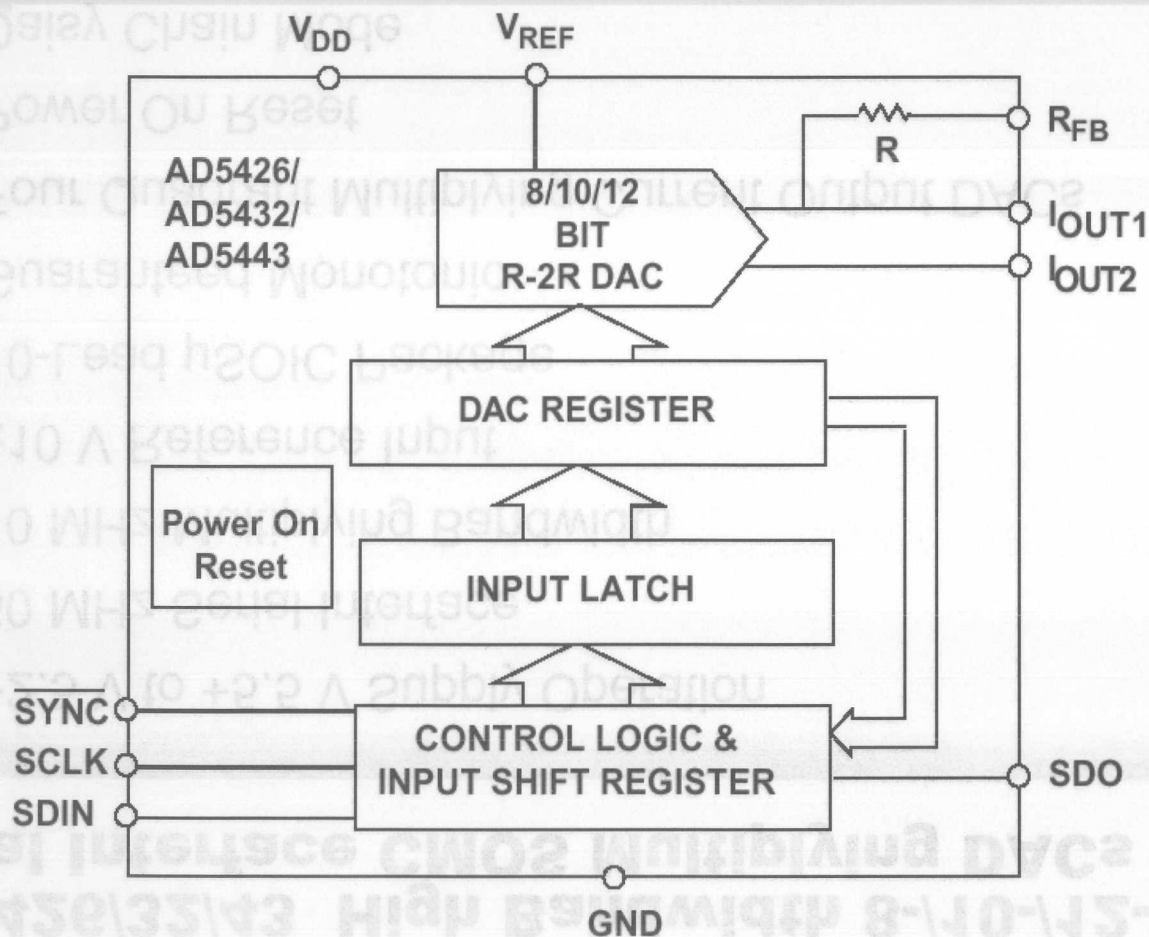
AD5424/33/45 High Bandwidth Parallel Interface 8-/10-/12-Bit CMOS Multiplying DACs



AD5424/33/45 High Bandwidth Parallel Interface 8-/10-/12-Bit CMOS Multiplying DACs

- +2.5 V to +5.5 V Supply Operation
- Fast Parallel Interface
- 10 MHz Multiplying Bandwidth
- ± 10 V Reference Input
- Guaranteed Monotonic
- Four Quadrant Multiplying, Current Output DACs
- Power On Reset
- Daisy Chaining Function
- Readback Function
- 5 μ A typical Supply Current
- 20-Lead TSSOP and Chip Scale (4 x 4 mm) Packages

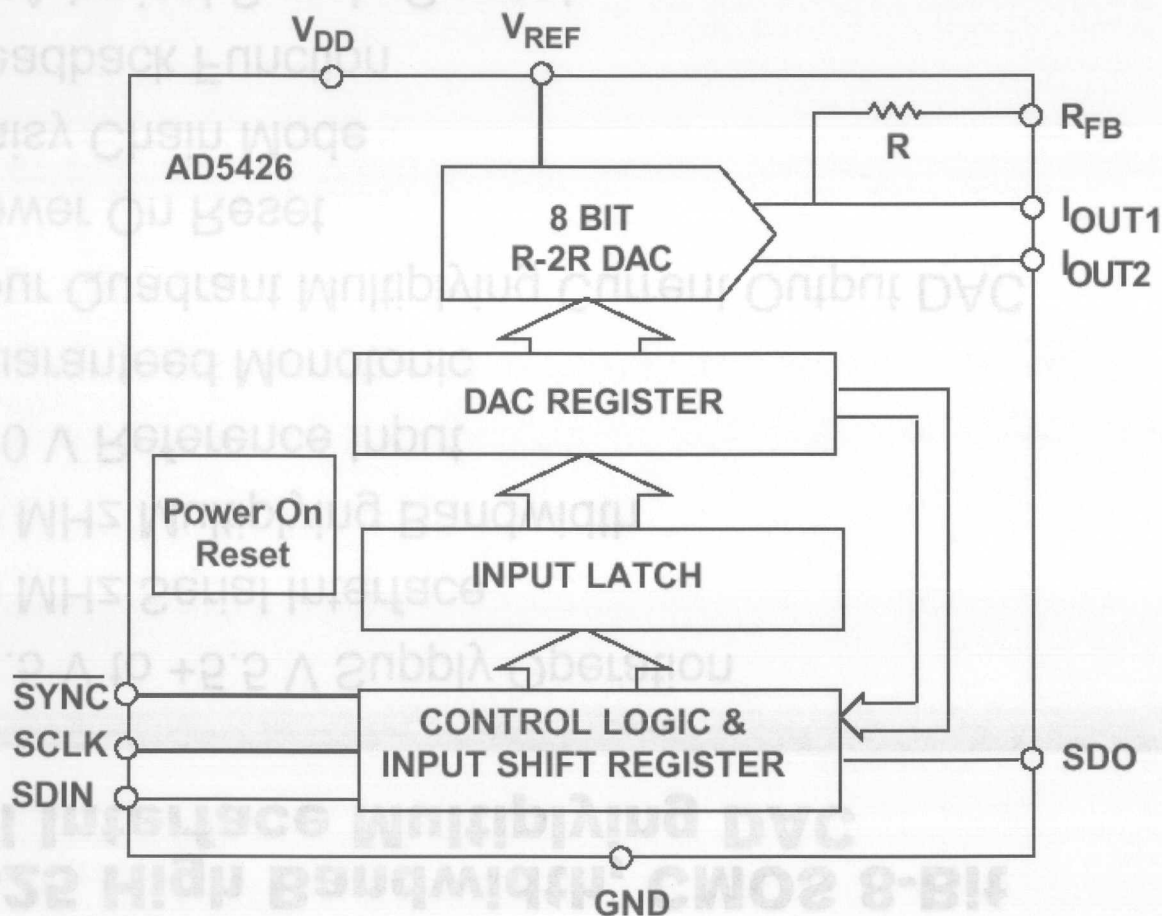
AD5426/32/43 High Bandwidth 8-/10-/12-Bit Serial Interface CMOS Multiplying DACs



AD5426/32/43 High Bandwidth 8-/10-/12-Bit Serial Interface CMOS Multiplying DACs

- +2.5 V to +5.5 V Supply Operation
- 50 MHz Serial Interface
- 10 MHz Multiplying Bandwidth
- ± 10 V Reference Input
- 10-Lead μ SOIC Package
- Guaranteed Monotonic
- Four Quadrant Multiplying Current Output DACs
- Power On Reset
- Daisy Chain Mode
- Readback Function
- 5 μ A typical Supply Current

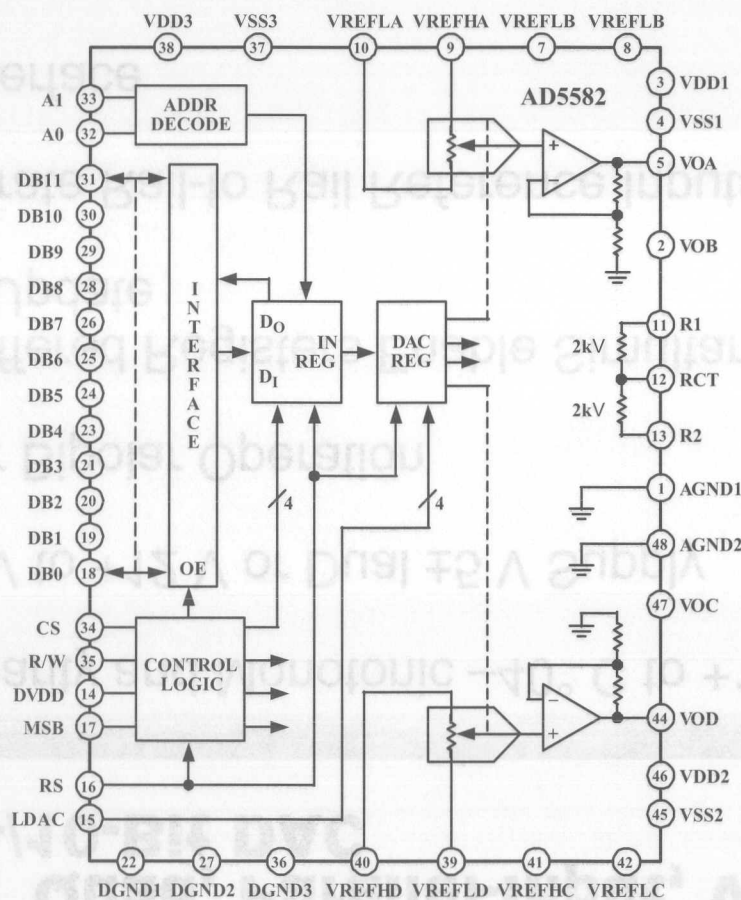
AD5425 High Bandwidth, CMOS 8-Bit Serial Interface Multiplying DAC



AD5425 High Bandwidth, CMOS 8-Bit Serial Interface Multiplying DAC

- +2.5 V to +5.5 V Supply Operation
- 50 MHz Serial Interface
- 10 MHz Multiplying Bandwidth
- ± 10 V Reference Input
- Guaranteed Monotonic
- Four Quadrant Multiplying Current Output DAC
- Power On Reset
- Daisy Chain Mode
- Readback Function
- 5 μ A typical Supply Current
- Automotive Temperature Range: -40° C to $+125^{\circ}$ C
- 10-Lead μ SOIC Package

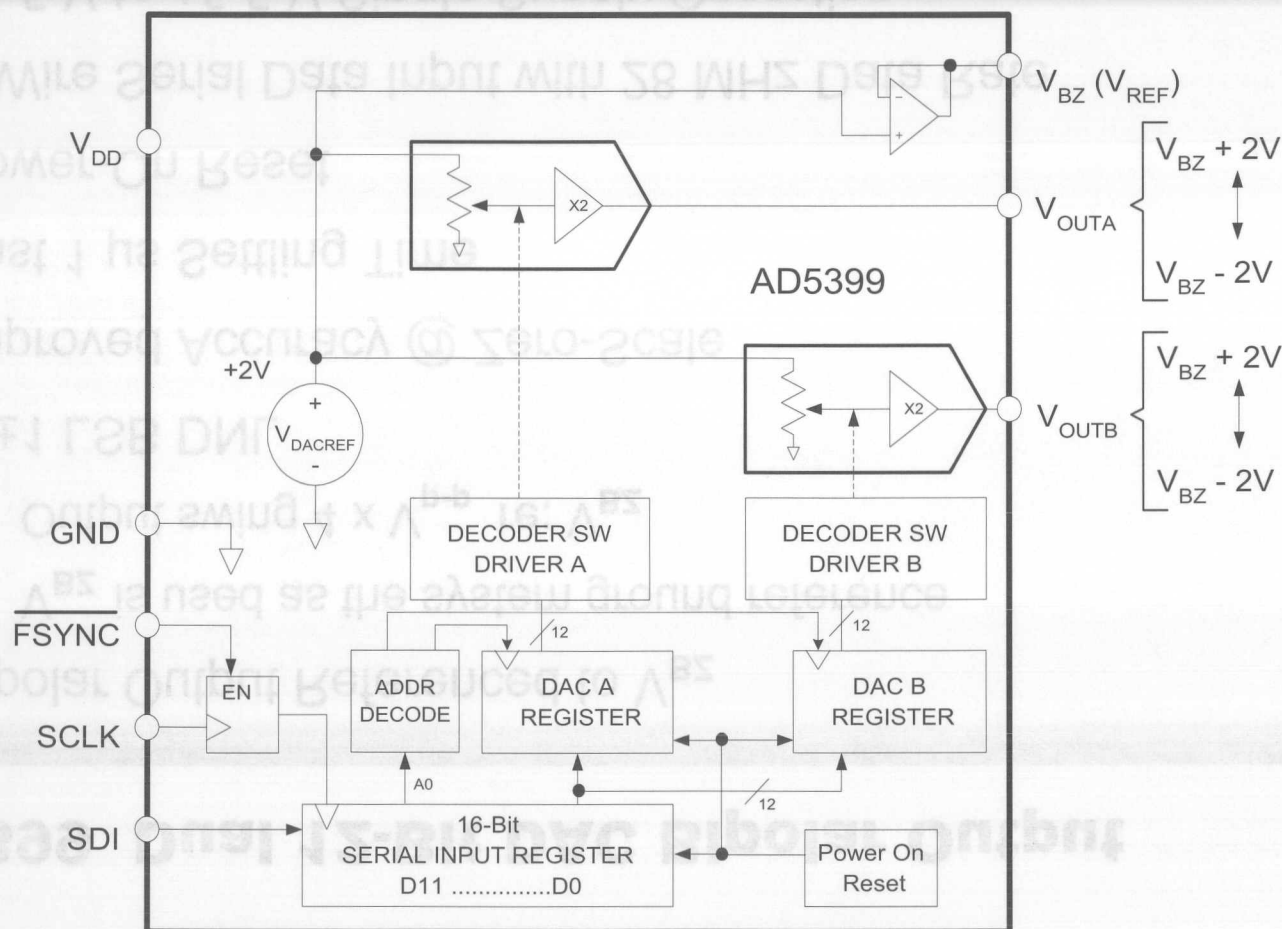
AD5582/83 Quad, Parallel-Input, Voltage Output, 12-/10-Bit DAC



AD5582/83 Quad, Parallel-Input, Voltage Output, 12-/10-Bit DAC

- 12-Bit Linearity and Monotonic -40°C to $+125^{\circ}\text{C}$
- Single $+5\text{ V}$ to $+12\text{ V}$ or Dual $\pm 5\text{ V}$ Supply
- Unipolar or Bipolar Operation
- Double Buffered Registers Enable Simultaneous Multi-Channels Update
- Four Separate Rail-to Rail Reference Inputs
- Parallel Interface
- Data Readback Capability
- $5\text{ }\mu\text{s}$ Settling Time

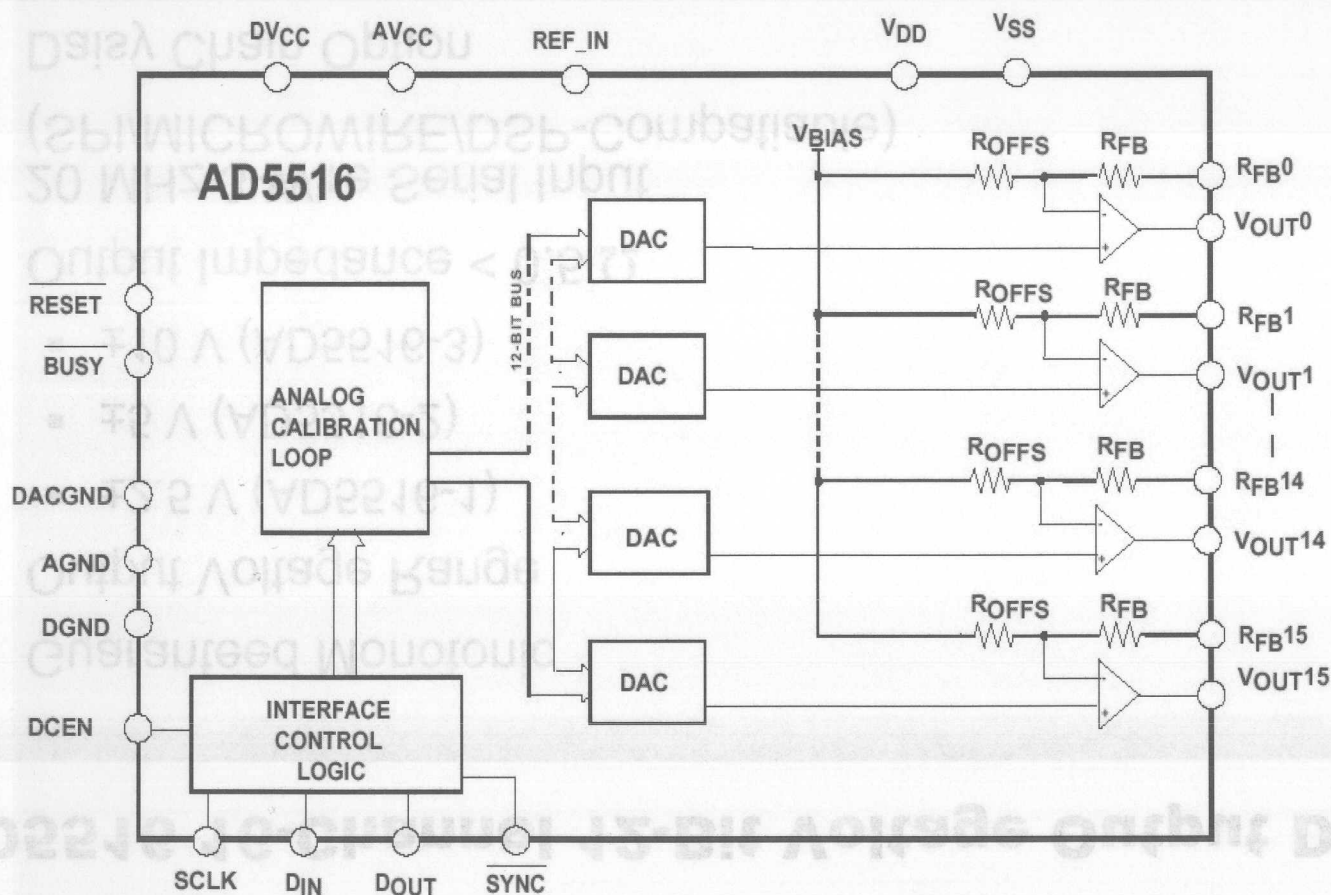
AD5399 Dual 12-Bit DAC Bipolar Output



AD5399 Dual 12-Bit DAC Bipolar Output

- Bipolar Output Referenced to V_{BZ}
 - V_{BZ} is used as the system ground reference
 - Output swing $4 \times V_{p-p}$ re: V_{BZ}
- $< \pm 1$ LSB DNL
- Improved Accuracy @ Zero-Scale
- Fast 1 μ s Settling Time
- Power-On Reset
- 3-Wire Serial Data Input with 28 MHz Data Rate
- +4.5 V to +5.5 V Single Supply Operation
- Internal REF

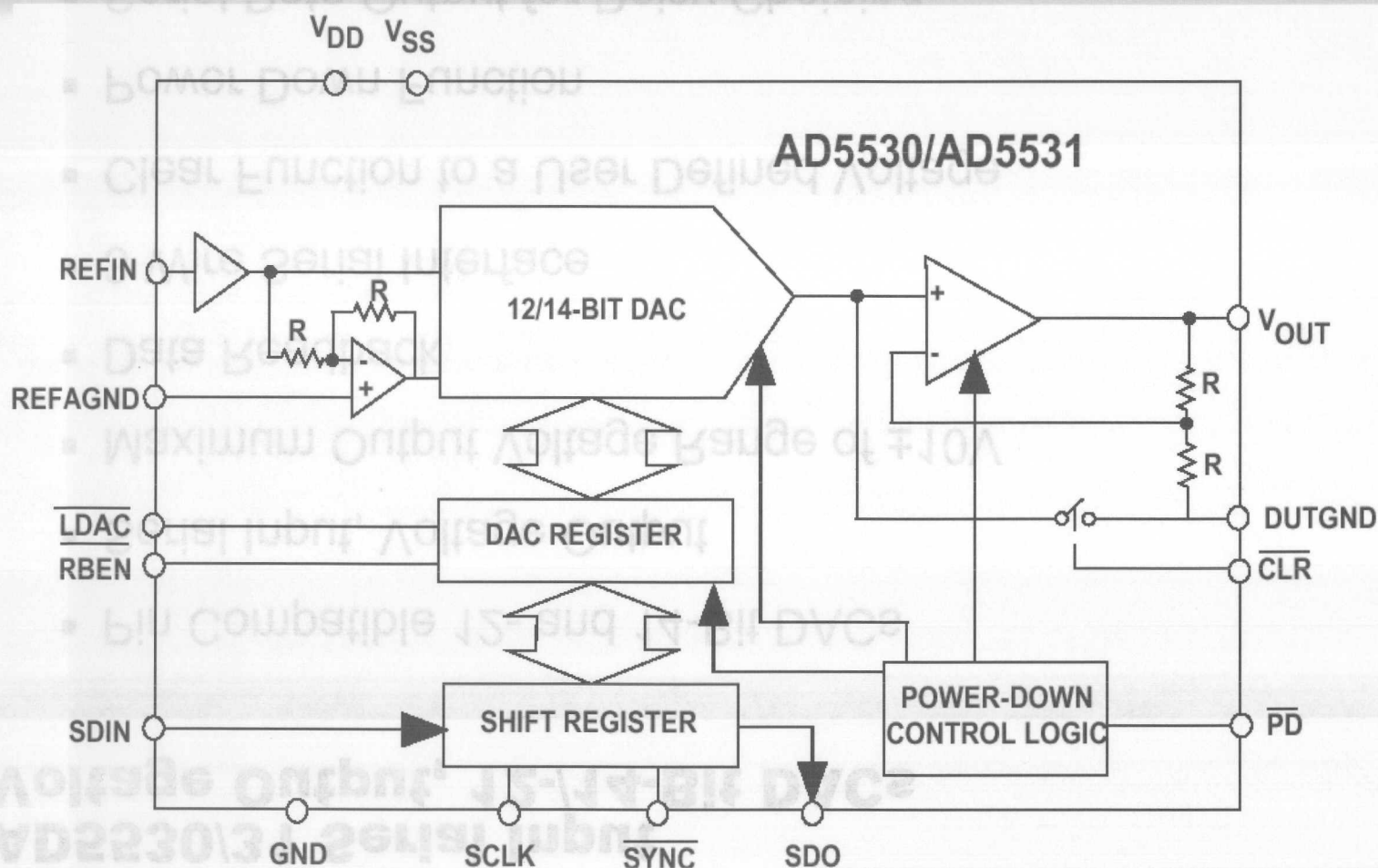
AD5516 16-Channel 12-Bit Voltage Output DAC



AD5516 16-Channel 12-Bit Voltage Output DAC

- Guaranteed Monotonic
- Output Voltage Range
 - ± 2.5 V (AD5516-1)
 - ± 5 V (AD5516-2)
 - ± 10 V (AD5516-3)
- Output Impedance $< 0.5 \Omega$
- 20 MHz 3-Wire Serial Input
(SPI/MICROWIRE/DSP-Compatible)
- Daisy Chain Option
- Asynchronous Reset
- Separate Analog and Digital Supplies

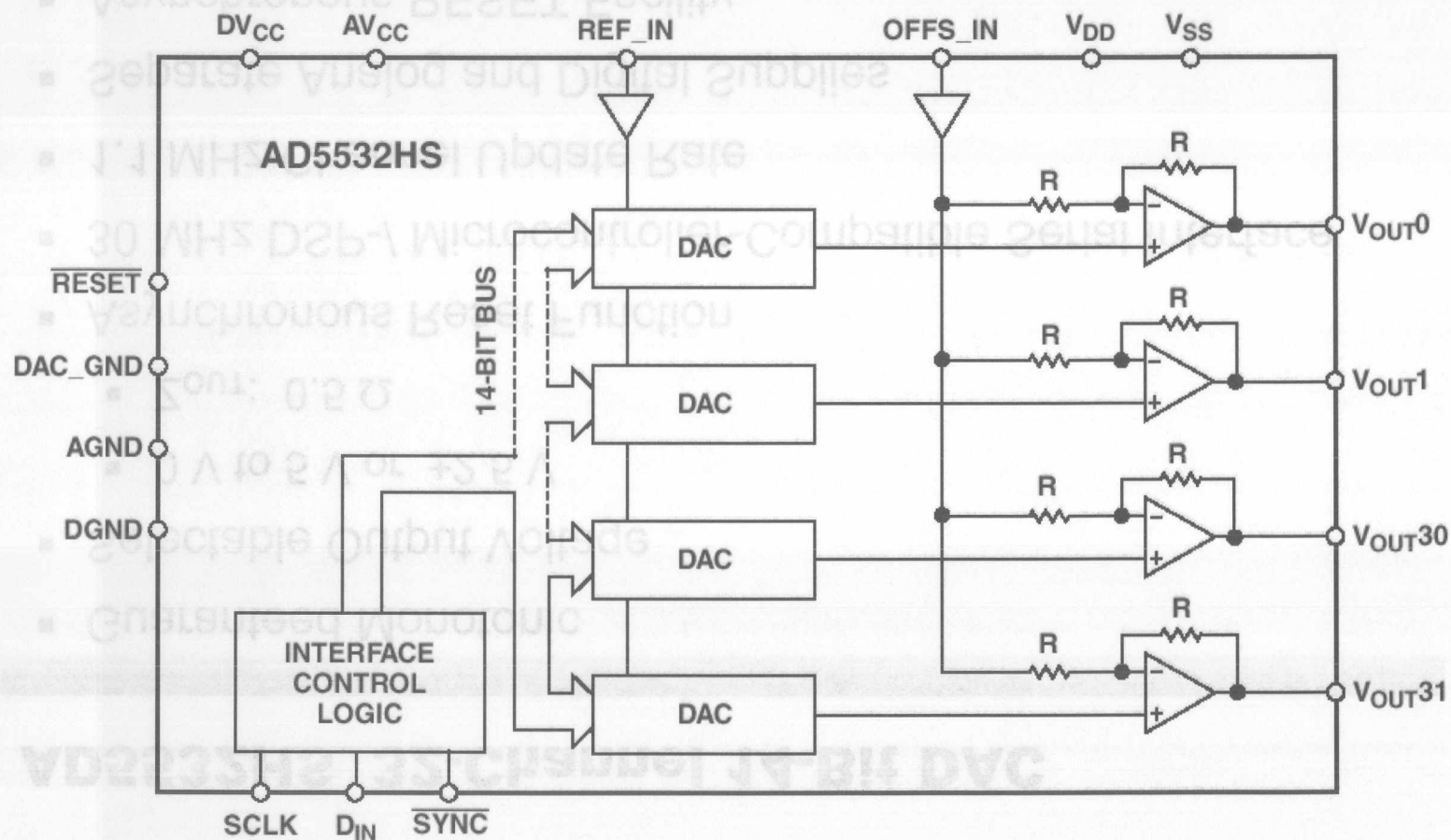
AD5530/31 Serial Input Voltage Output, 12-/14-Bit DACs



AD5530/31 Serial Input Voltage Output, 12-/14-Bit DACs

- Pin Compatible 12- and 14-Bit DACs
- Serial Input, Voltage Output
- Maximum Output Voltage Range of $\pm 10\text{V}$
- Data Readback
- 3 Wire Serial Interface
- Clear Function to a User Defined Voltage
- Power Down Function
- Serial Data Output for Daisy Chaining
- 16 Lead TSSOP Packages

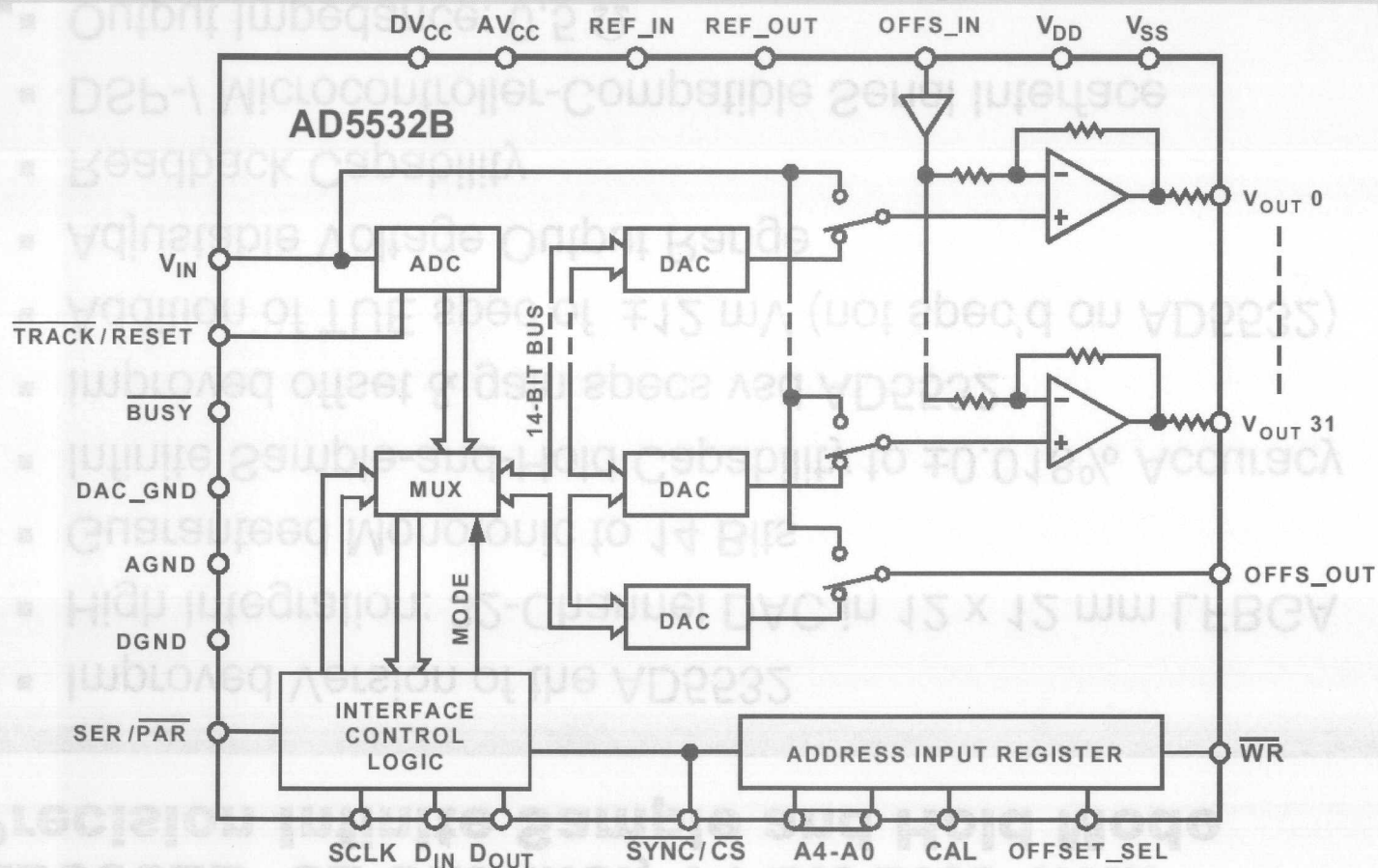
AD5532HS 32-Channel 14-Bit DAC



AD5532HS 32-Channel 14-Bit DAC

- Guaranteed Monotonic
- Selectable Output Voltage
 - 0 V to 5 V or ± 2.5 V
 - Z_{OUT} : $0.5\ \Omega$
- Asynchronous Reset Function
- 30 MHz DSP-/ Microcontroller-Compatible Serial Interface
- 1.1 MHz Channel Update Rate
- Separate Analog and Digital Supplies
- Asynchronous RESET Facility
- Temperature Range -40°C to $+85^{\circ}\text{C}$
- High Integration: 32-Channel DAC in 12 x 12 mm LFBGA

AD5532B 32-Channel, 14-Bit DAC with Precision Infinite Sample and Hold Mode



AD5532B 32-Channel, 14-Bit DAC with Precision Infinite Sample and Hold Mode

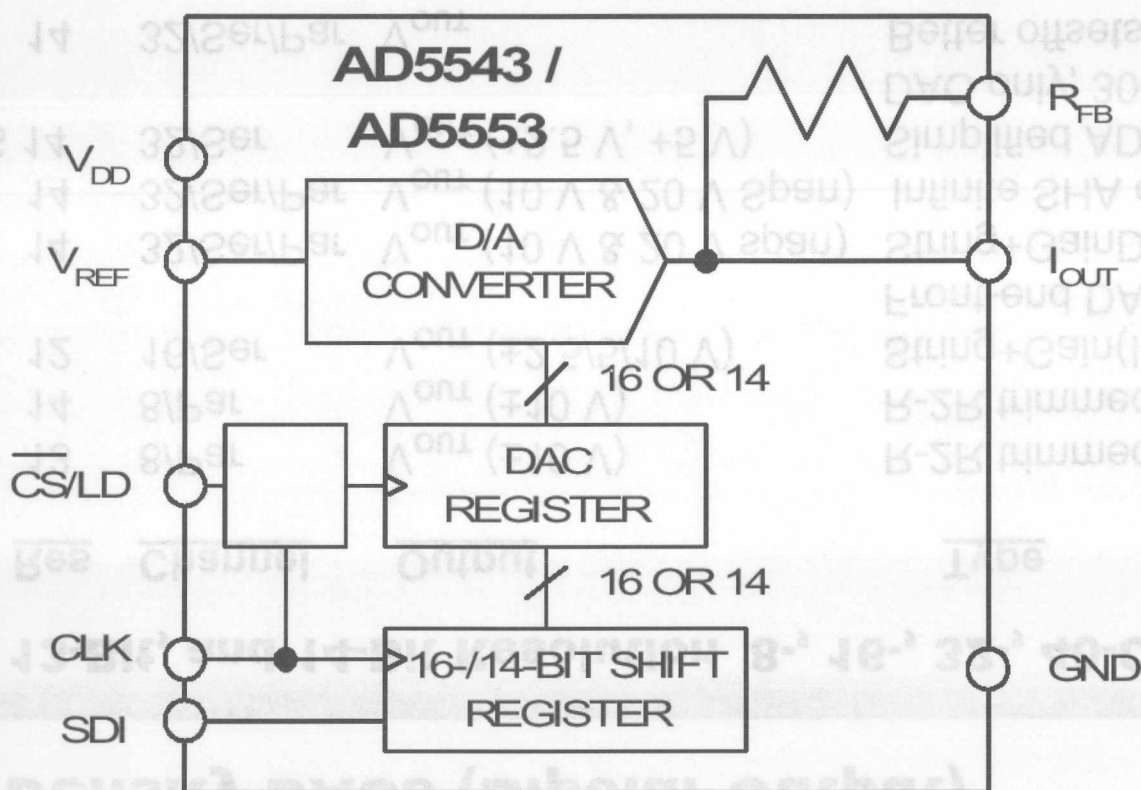
- Improved Version of the AD5532
- High Integration: 32-Channel DAC in 12 x 12 mm LFBGA
- Guaranteed Monotonic to 14 Bits
- Infinite Sample-and-Hold Capability to $\pm 0.018\%$ Accuracy
- Improved offset & gain specs vsd AD5532
- Addition of TUE spec of ± 12 mV (not spec'd on AD5532)
- Adjustable Voltage Output Range
- Readback Capability
- DSP-/ Microcontroller-Compatible Serial Interface
- Output Impedance: 0.5Ω
- Output Voltage Span 10 V
- Temperature Range -40°C to $+85^{\circ}\text{C}$

High Density DACs (Bipolar Output)

12-Bit, 13-Bit, and 14-Bit Resolution 8-, 16-, 32-, 40-Channel

<u>Part</u>	<u>Res</u>	<u>Channel</u>	<u>Output</u>	<u>Type</u>
AD7839	13	8/Par	V_{OUT} (± 10 V)	R-2R trimmed
AD7841	14	8/Par	V_{OUT} (± 10 V)	R-2R trimmed
AD5516	12	16/Ser	V_{OUT} ($\pm 2.5/5/10$ V)	String+Gain(I-SHA) Front-end DAC on-chip
AD5532	14	32/Ser/Par	V_{OUT} (10 V & 20 V span)	String+GainDAC or Inf-SHA
AD5533	14	32/Ser/Par	V_{OUT} (10 V & 20 V Span)	Infinite SHA only
AD5532HS	14	32/Ser	V_{OUT} (± 2.5 V, +5 V)	Simplified AD5532, DAC only, 30Hz t'put
AD5532B	14	32/Ser/Par	V_{OUT}	Better offsets, TUE,gain specs
AD5379	13	40/ Ser/Pa	V_{OUT} (± 10 V max)	Calibrated string DAC
AD5380	14	40/Ser/Pa	V_{OUT} (0–5 V)	Calibrated string DAC

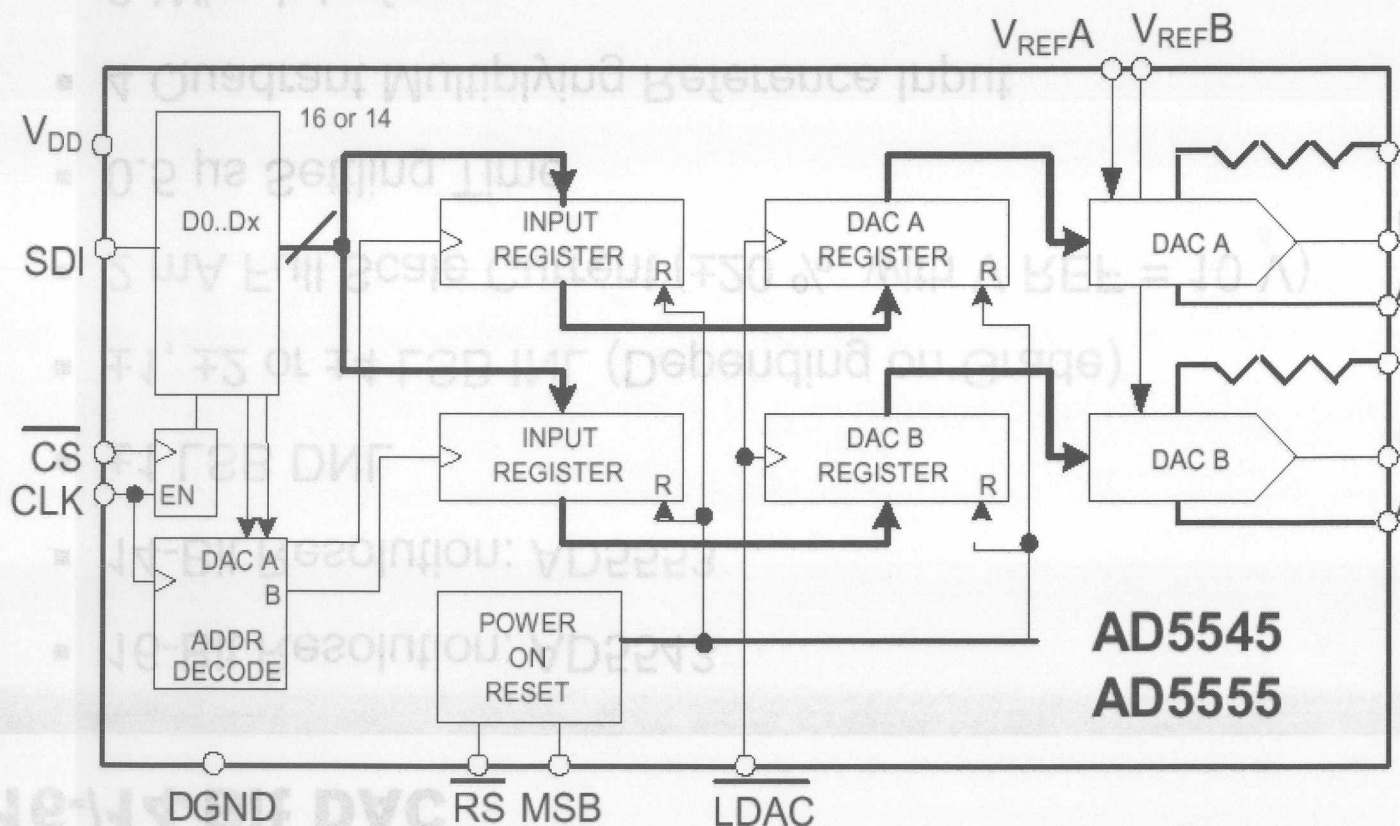
AD5543/53 Current-Output Serial-Input, 16-/14-Bit DAC



AD5543/53 Current-Output Serial-Input, 16-/14-Bit DAC

- 16-Bit Resolution: AD5543
- 14-Bit Resolution: AD5553
- ± 1 LSB DNL
- ± 1 , ± 2 or ± 4 LSB INL (Depending on Grade)
- 2 mA Full Scale Current ($\pm 20\%$, with $V_{REF} = 10\text{ V}$)
- $0.5\text{ }\mu\text{s}$ Settling Time
- 4 Quadrant Multiplying Reference Input
- 3-Wire Interface
- Ultra Compact $\mu\text{SOIC-8}$ Package

AD5545/55 Dual, Current-Output Serial-Input 16-/14-Bit DAC



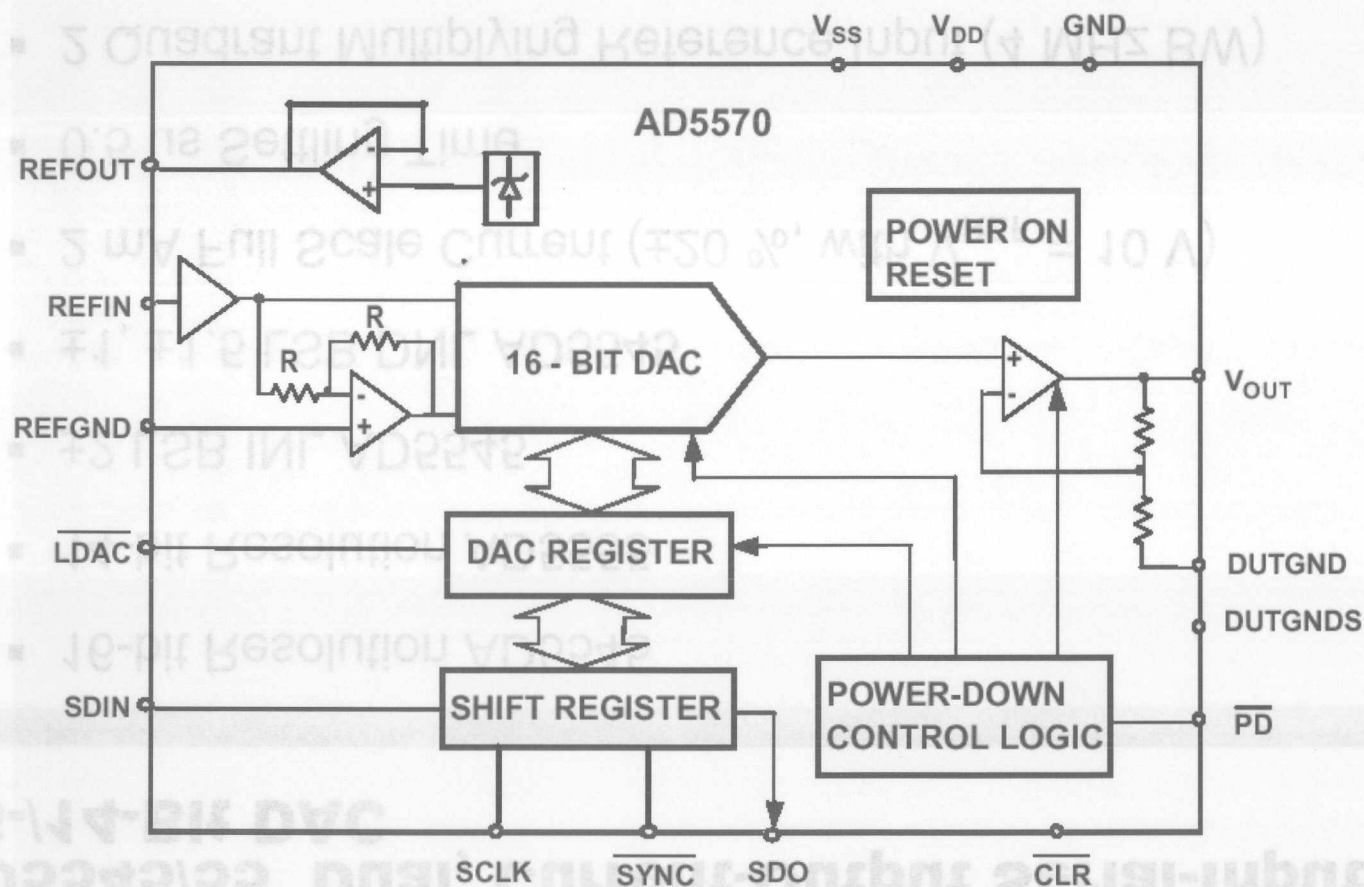
AD5545
AD5555

AD5545/55 Dual, Current-Output Serial-Input, 16-/14-Bit DAC

- 16-bit Resolution AD5545
- 14-bit Resolution AD5555
- ± 2 LSB INL AD5545
- $\pm 1, \pm 1.5$ LSB DNL AD5545
- 2 mA Full Scale Current ($\pm 20\%$, with $V_{REF} = 10$ V)
- 0.5 μ s Settling Time
- 2 Quadrant Multiplying Reference Input (4 MHz BW)
- 3-Wire Interface
- Compact TSSOP-16 Package

AD5570 12 V/ 15 V, 16-Bit DAC

Serial Input, Voltage Output,



AD5570 12 V/ 15 V, 16-Bit DAC

Serial Input, Voltage Output,

- Full 16-Bit Performance
- 1 LSB Max INL and DNL
- Maximum Output Voltage Range of ± 10 V
- Settling Time of 10 μ s max at 16 bits
- Clear Function to a User Defined Voltage
- Asynchronous Update of Outputs (LDAC pin)
- Power On Reset to 0 Volts
- Serial Data Output for Daisy Chaining
- Data Readback Facility
- Temperature Range: -40° C to $+125^{\circ}$ C



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PRECISIONARY DATA

- Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Data Feedback Facility
- Serial Data Output for Daisy Chaining
- Power On Reset to 0 Volts
- Asynchronous Update of Outputs (LDAC pin)
- Clear Function to a User Defined Voltage
- Self-Test
- Maximum Output Voltage Range of $\pm 10\text{ V}$
- ± 128 Max Int and DNL
- Full 16-Bit Performance

Digital Potentiometers

Serial Input, Voltage Output,
AD2210 $\pm 5\text{ V}$ $\pm 12\text{ V}$, 16-Bit DAC



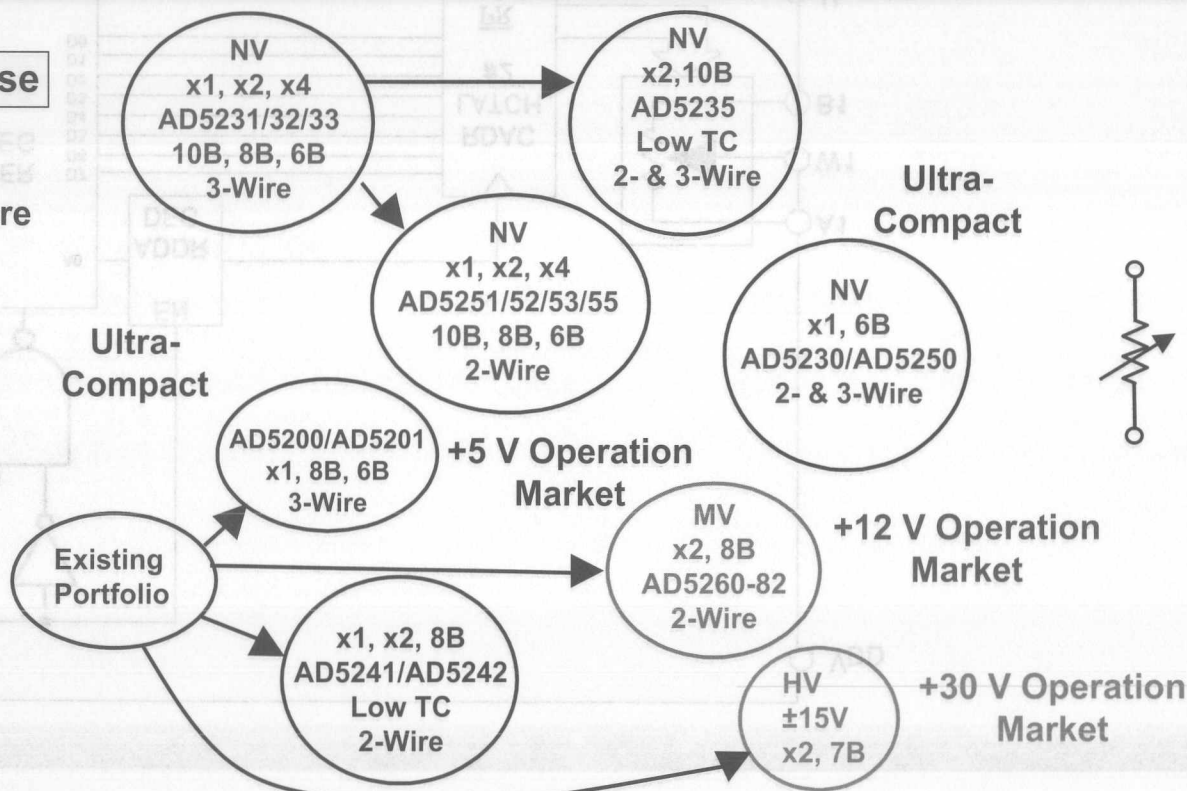
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Digital Potentiometer Roadmap

General-Purpose

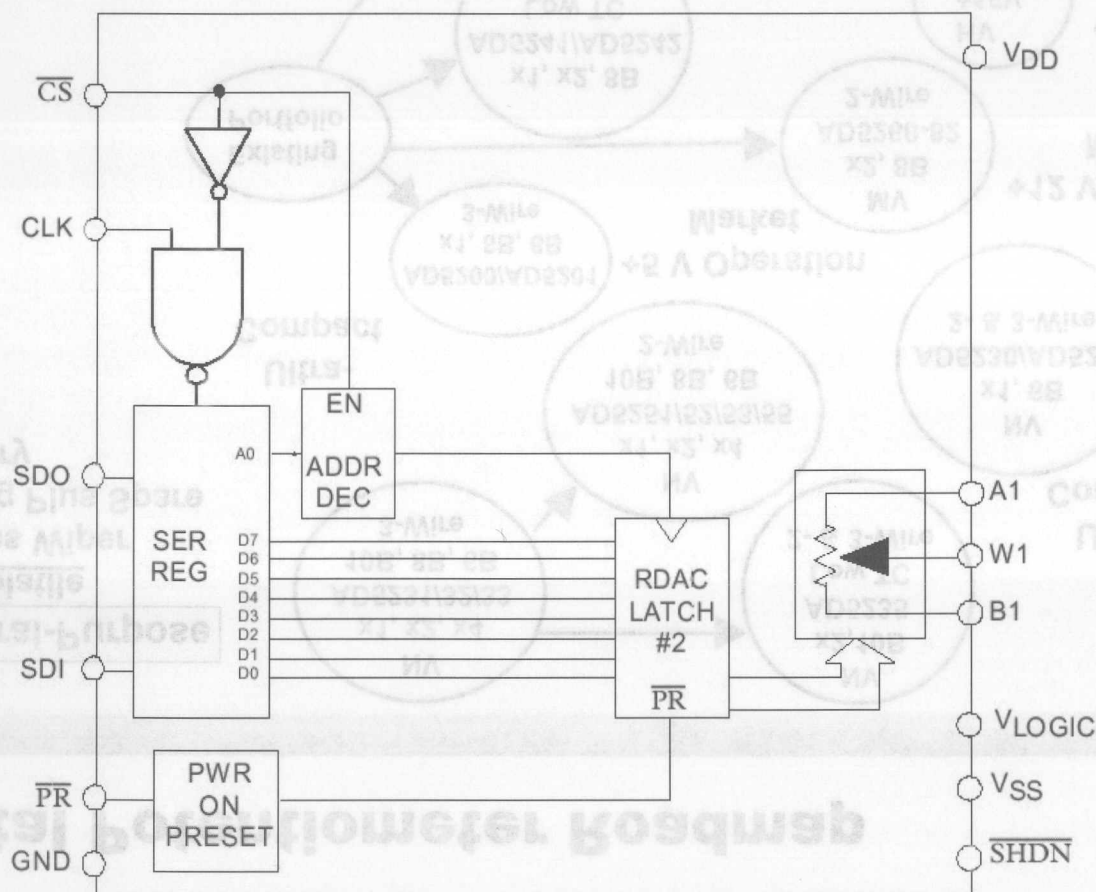
Nonvolatile

Retains Wiper
Setting Plus Spare
Memory

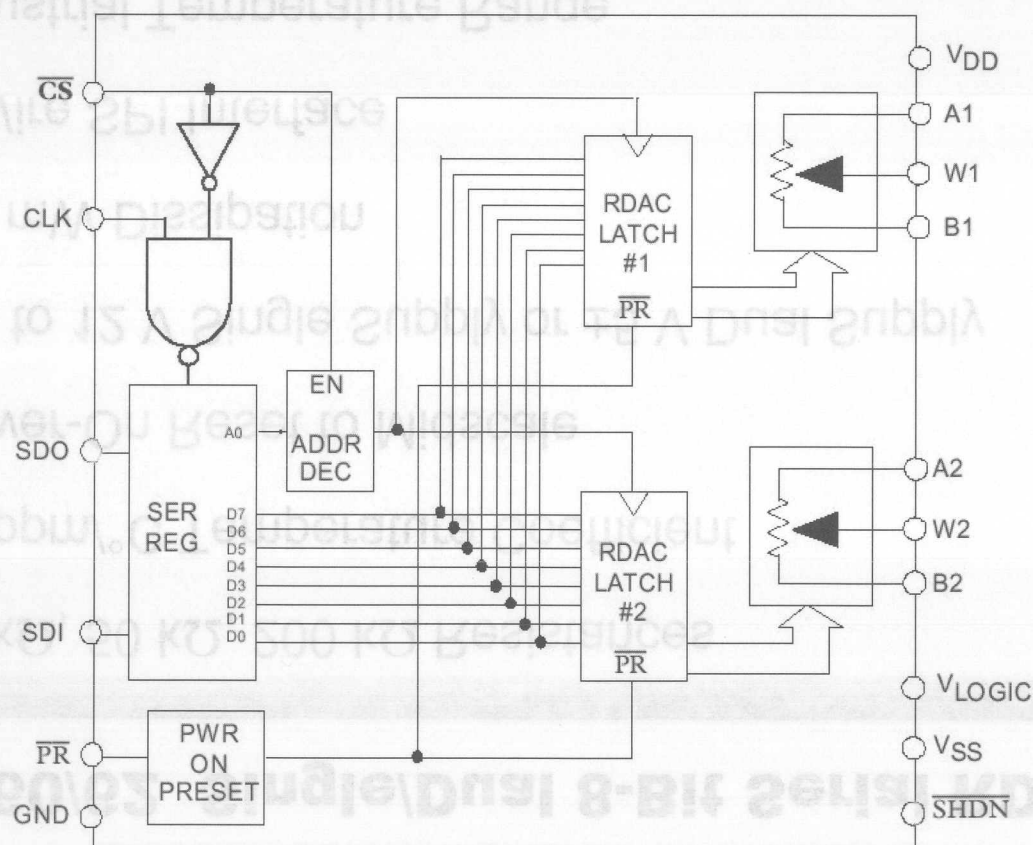


INSTRUMENTATION

AD5260 8-Bit Serial RDAC



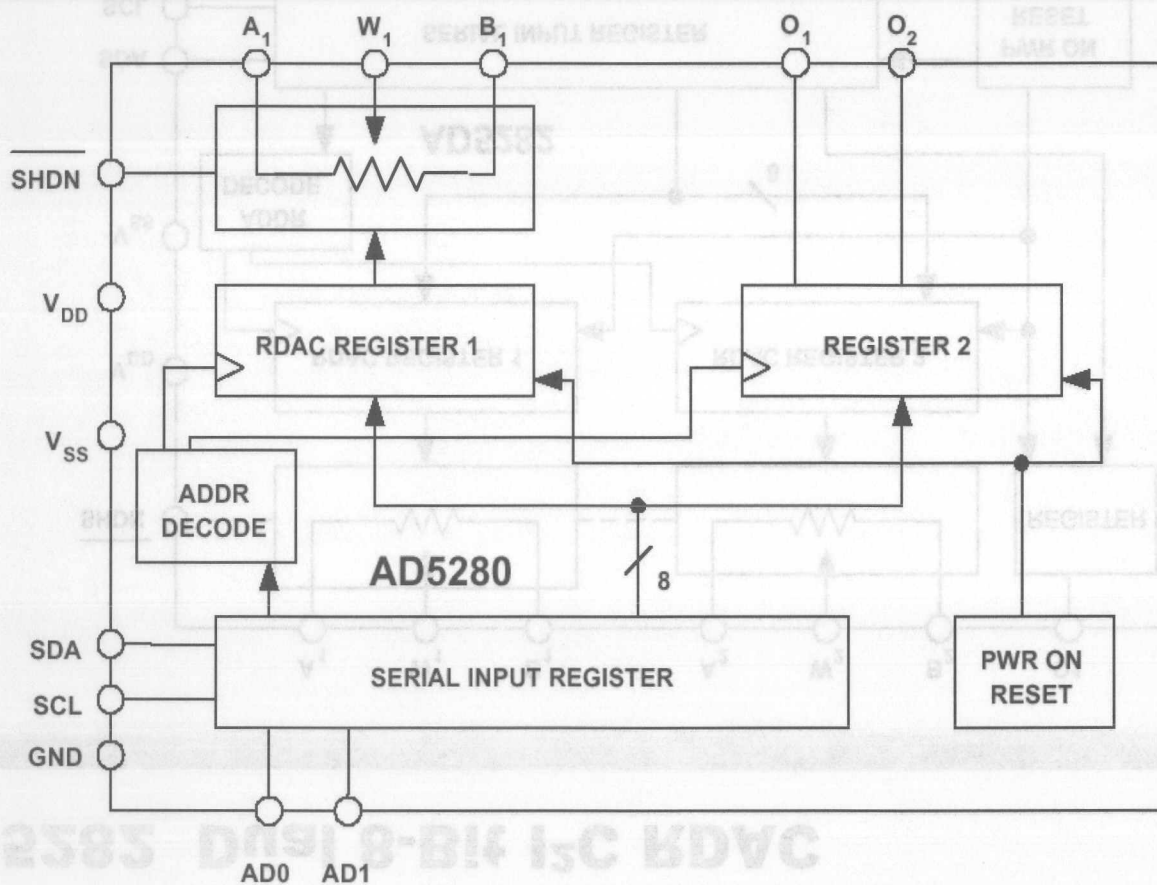
AD5262 Dual 8-Bit Serial RDAC



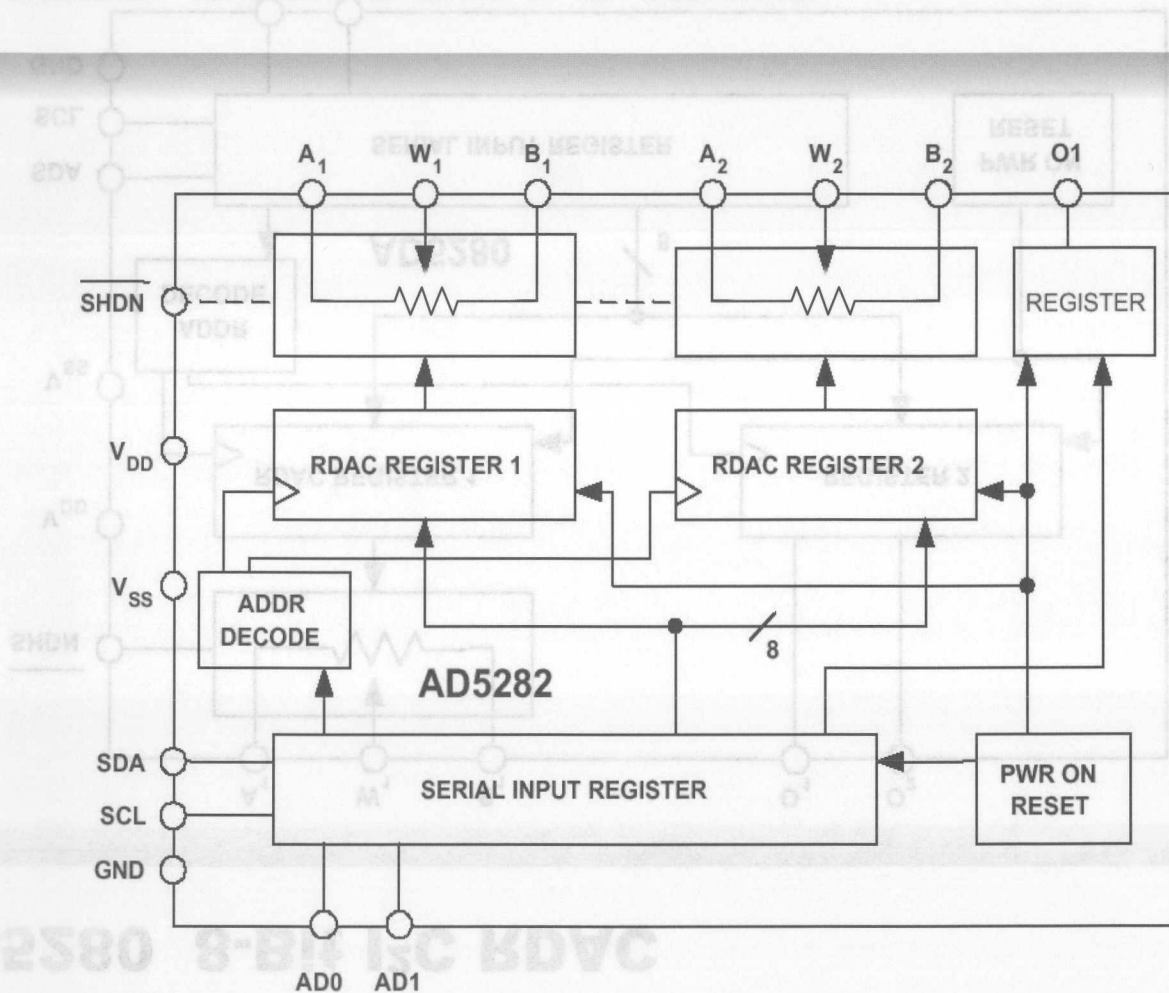
AD5260/62 Single/Dual 8-Bit Serial RDAC

- 20 k Ω , 50 k Ω , 200 k Ω Resistances
- 50 ppm/ $^{\circ}$ C Temperature Coefficient
- Power-On Reset to Midscale
- 5 V to 12 V Single Supply or ± 5 V Dual Supply
- 0.6 mW Dissipation
- 3-Wire SPI Interface
- Industrial Temperature Range
 - -40 $^{\circ}$ C to +125 $^{\circ}$ C

AD5280 8-Bit I²C RDAC



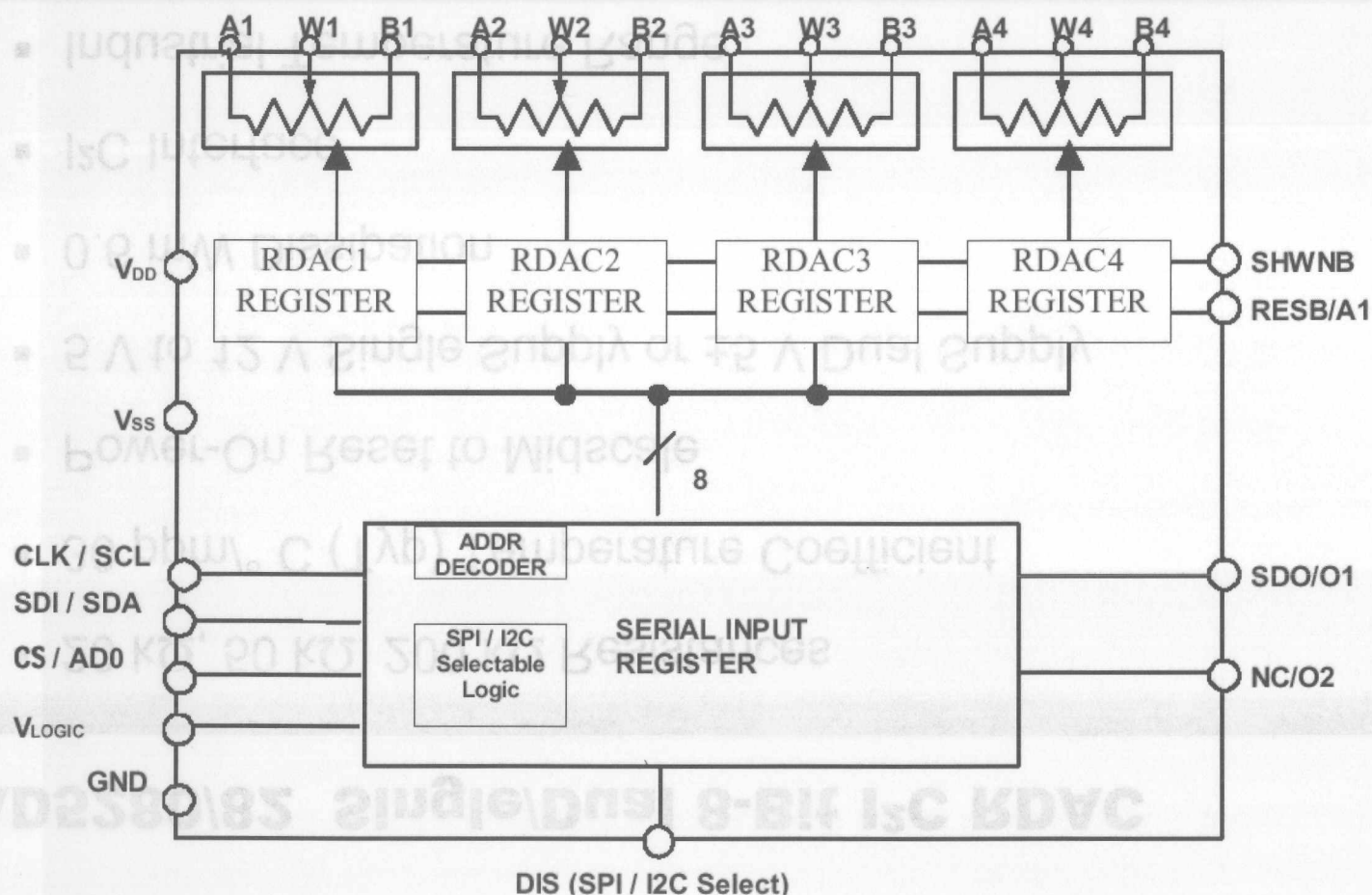
AD5282 Dual 8-Bit I²C RDAC



AD5280/82 Single/Dual 8-Bit I²C RDAC

- 20 k Ω , 50 k Ω , 200 k Ω Resistances
- 30 ppm/ $^{\circ}$ C (Typ) Temperature Coefficient
- Power-On Reset to Midscale
- 5 V to 12 V Single Supply or ± 5 V Dual Supply
- 0.6 mW Dissipation
- I²C Interface
- Industrial Temperature Range
 - -40 $^{\circ}$ C to +125 $^{\circ}$ C

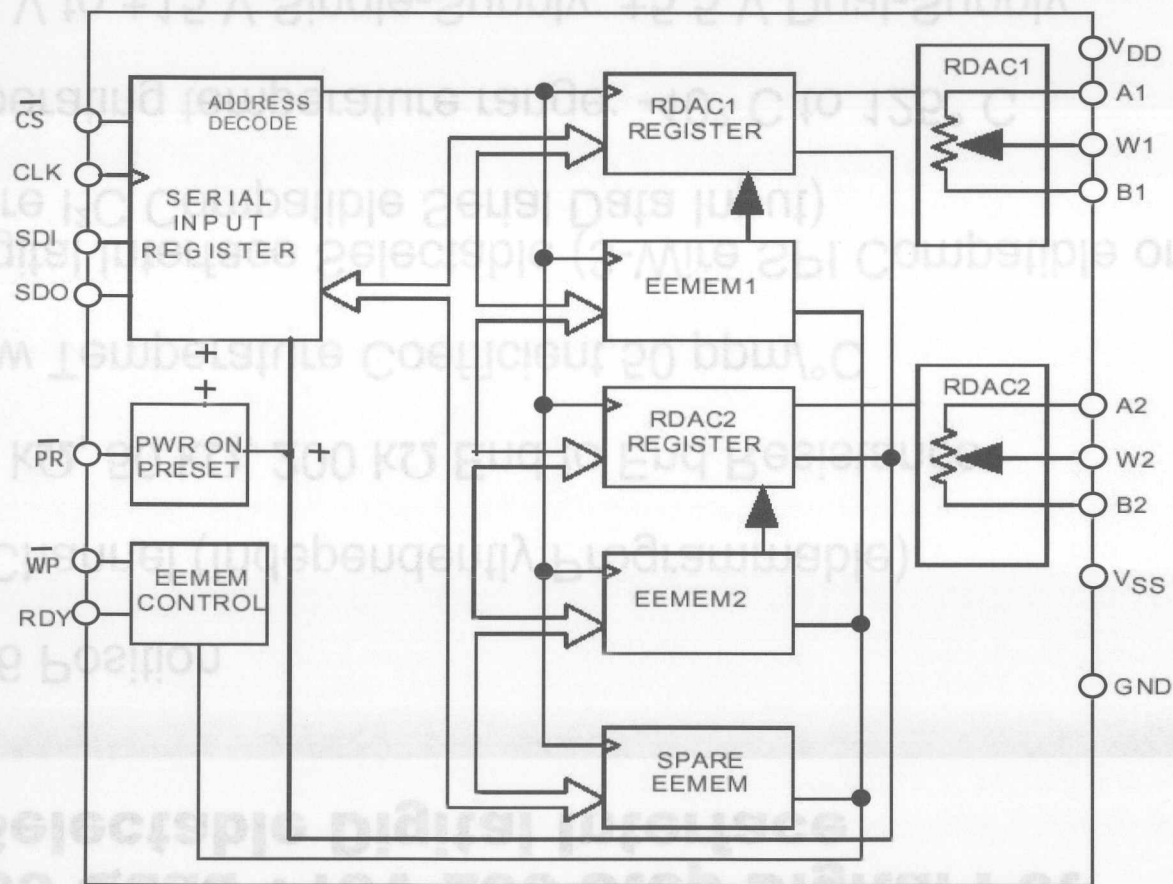
AD5263 Quad +15V 256-Step Digital Pot with Selectable Digital Interface



AD5263 Quad +15V 256-Step Digital Pot with Selectable Digital Interface

- 256 Position
- 4-Channel (Independently Programmable)
- 20 k Ω , 50 k Ω , 200 k Ω End to End Resistance
- Low Temperature Coefficient 50 ppm/ $^{\circ}$ C
- Digital Interface Selectable (3-Wire SPI Compatible or 2-Wire I²C Compatible Serial Data Input)
- Operating temperature range: -40 $^{\circ}$ C to 125 $^{\circ}$ C
- +5 V to +15 V Single-Supply; \pm 5.5 V Dual-Supply Operation

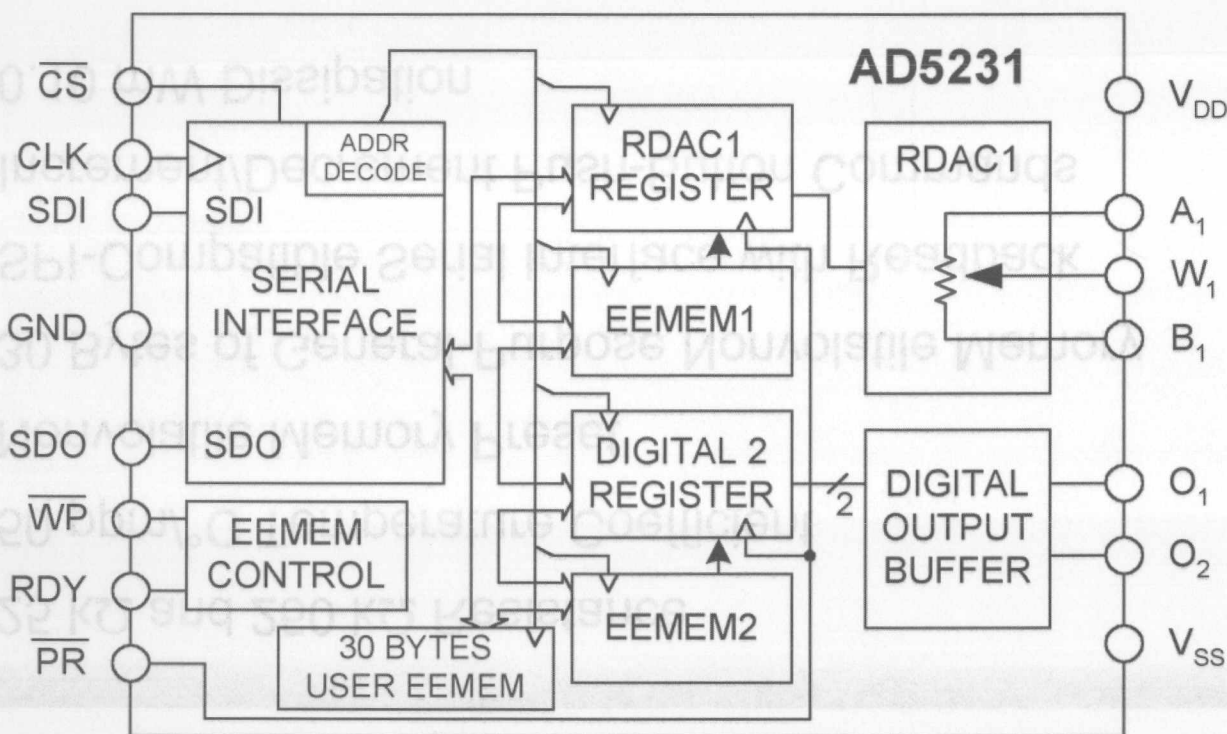
AD5235 Dual 10-Bit SPI Digital Potentiometer



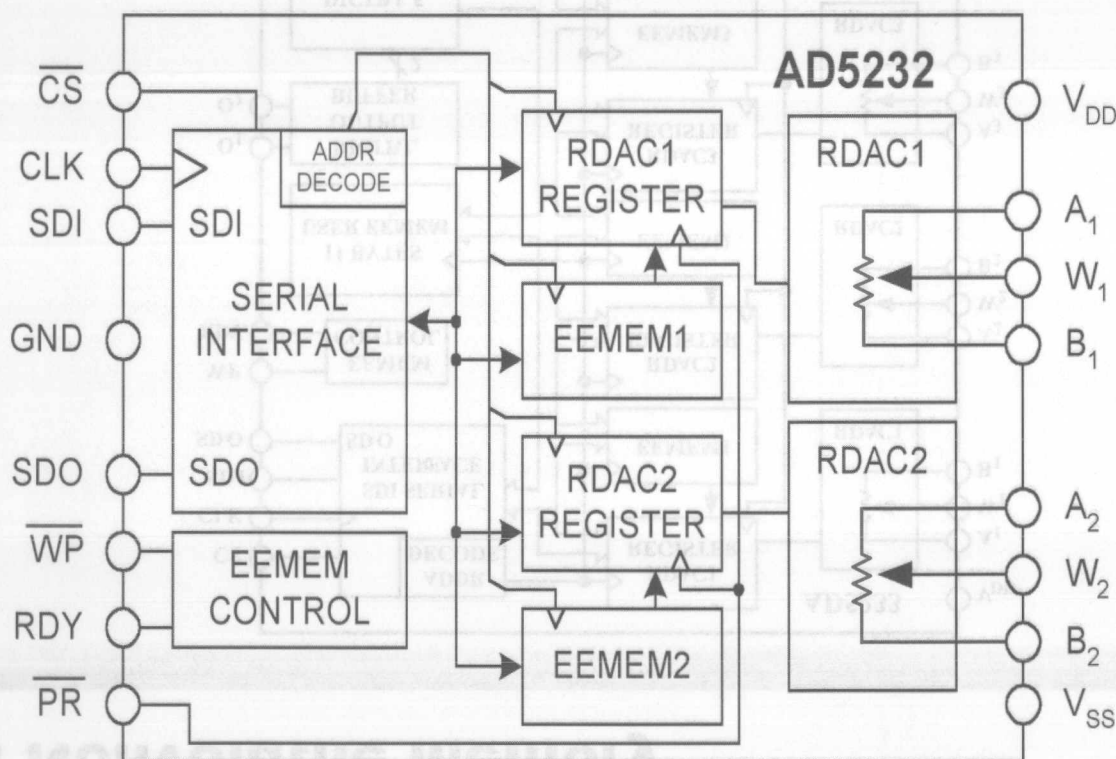
AD5235 Dual 10-Bit SPI Digital Potentiometer

- 25 k Ω and 250 k Ω Resistance
- 50 ppm/ $^{\circ}$ C Temperature Coefficient
- Nonvolatile Memory Preset
- 30 Bytes of General-Purpose Nonvolatile Memory
- SPI-Compatible Serial Interface with Readback
- Increment/Decrement Push-Button Commands
- 0.10 mW Dissipation

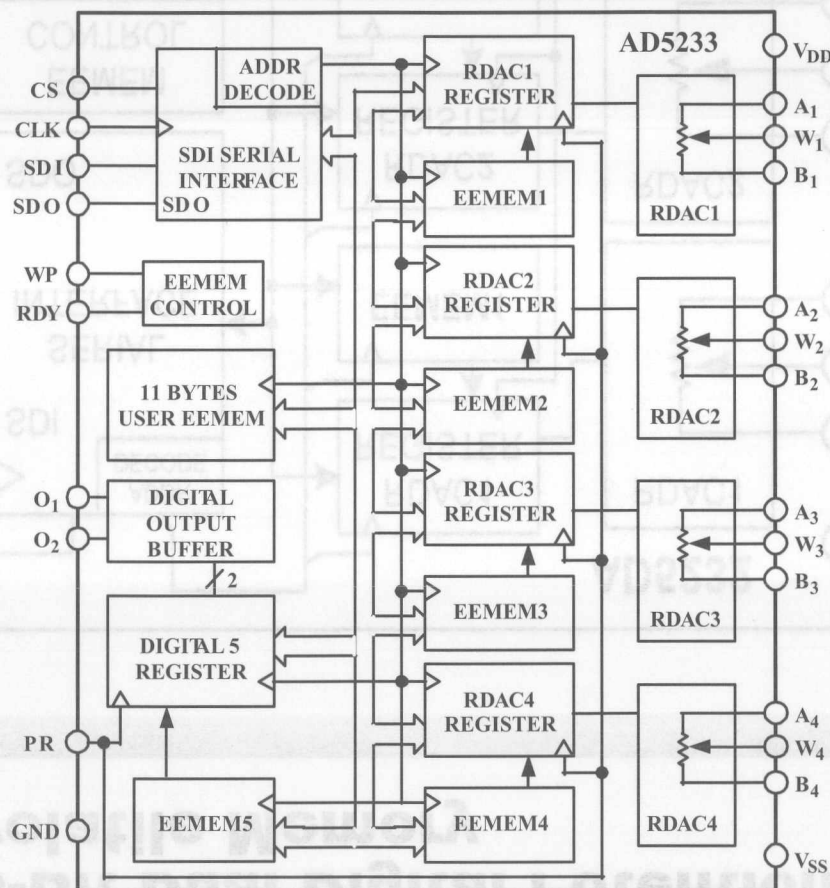
AD5231 10-Bit Digital Potentiometer with Nonvolatile Memory



AD5232 8-Bit Dual Digital Potentiometer with Nonvolatile Memory



AD5233 Quad 6-Bit Digital Potentiometer with Nonvolatile Memory



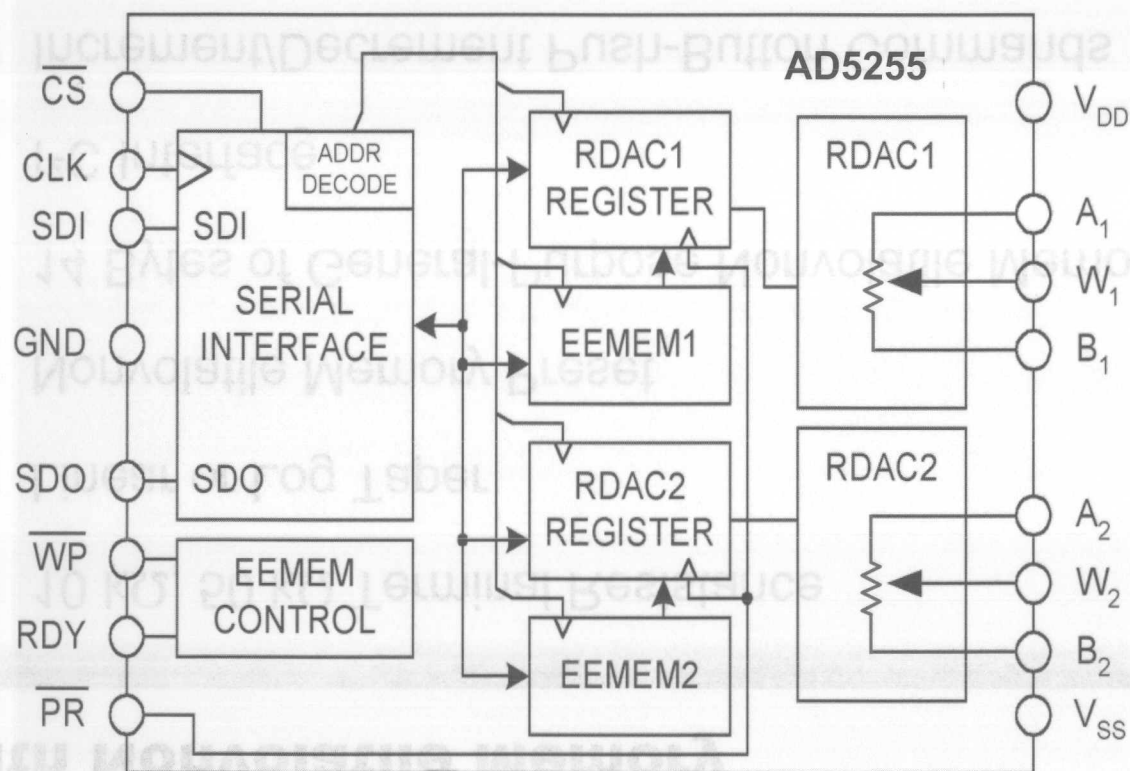
AD5231/32/33 Single/Dual/Quad Digital Pot with Nonvolatile Memory

- 0.10 mW Dissipation
- AD5231 Single 1024-Position Resolution
- AD5232 Dual 256-Position Resolution
- Increment/Decrement Commands
- AD5233 Quad 64-Position Resolution
- SPI-Compatible Serial Interface with Backup
- 10 k Ω , 50 k Ω , and 100 k Ω Terminal Resistance
- 58 Bytes of General-Purpose Nonvolatile Memory
- Nonvolatile Memory Preset
- Linear or Log Taper

AD5231/32/33 Single/Dual/Quad Digital Pot with Nonvolatile Memory

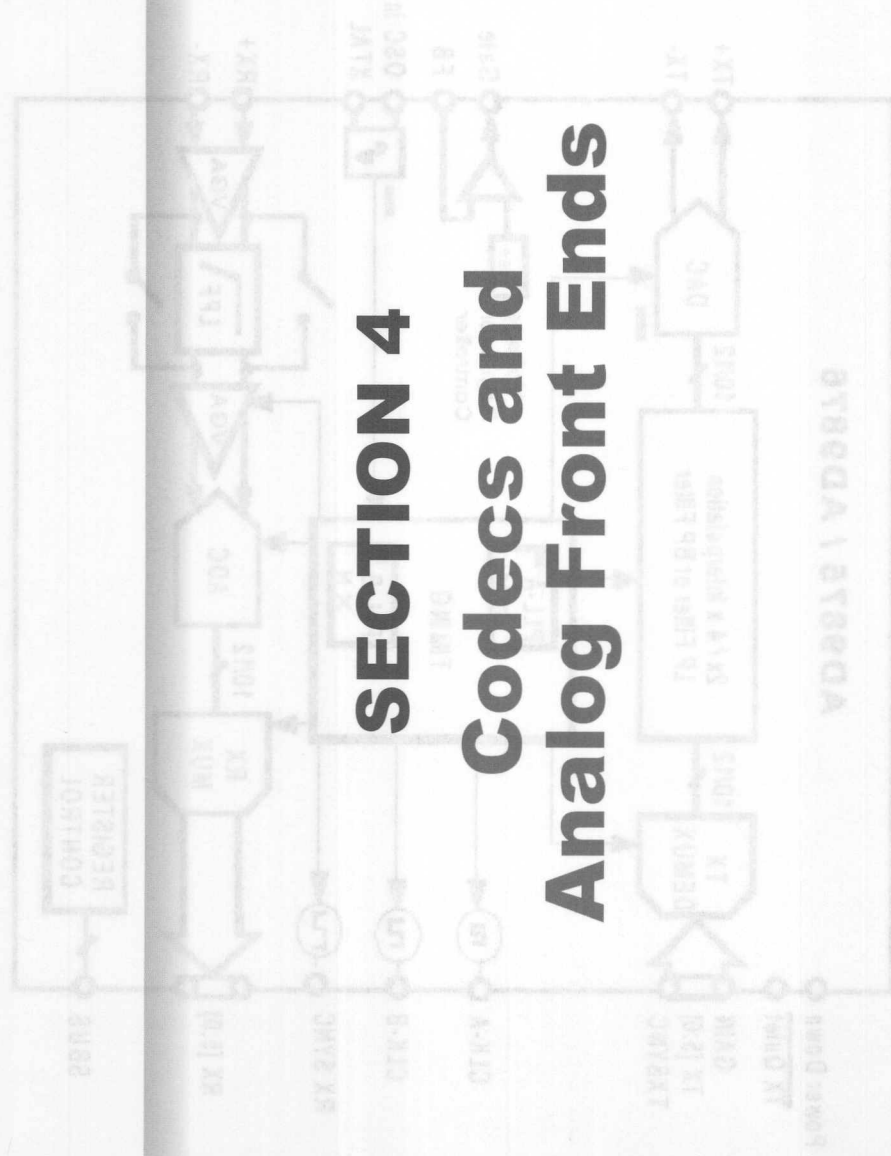
- Nonvolatile Memory Preset
- 200 ppm/°C Temperature Coefficient
- 28 Bytes of General-Purpose Nonvolatile Memory
- 10 kΩ, 20 kΩ, 50 kΩ, 100 kΩ Terminal Resistance
- SPI-Compatible Serial Interface with Readback
- AD5233 Quad 84-Position Resolution
- Increment/Decrement Commands
- AD5232 Dual 528-Position Resolution
- 3 V to 5 V Single Supply or ± 2.5 V Dual Supply
- AD5231 Single 1024-Position Resolution
- 0.10 mW Dissipation

AD5255 Dual 10-Bit I²C RDAC with Nonvolatile Memory



AD5255 Dual 10-Bit I²C RDAC with Nonvolatile Memory

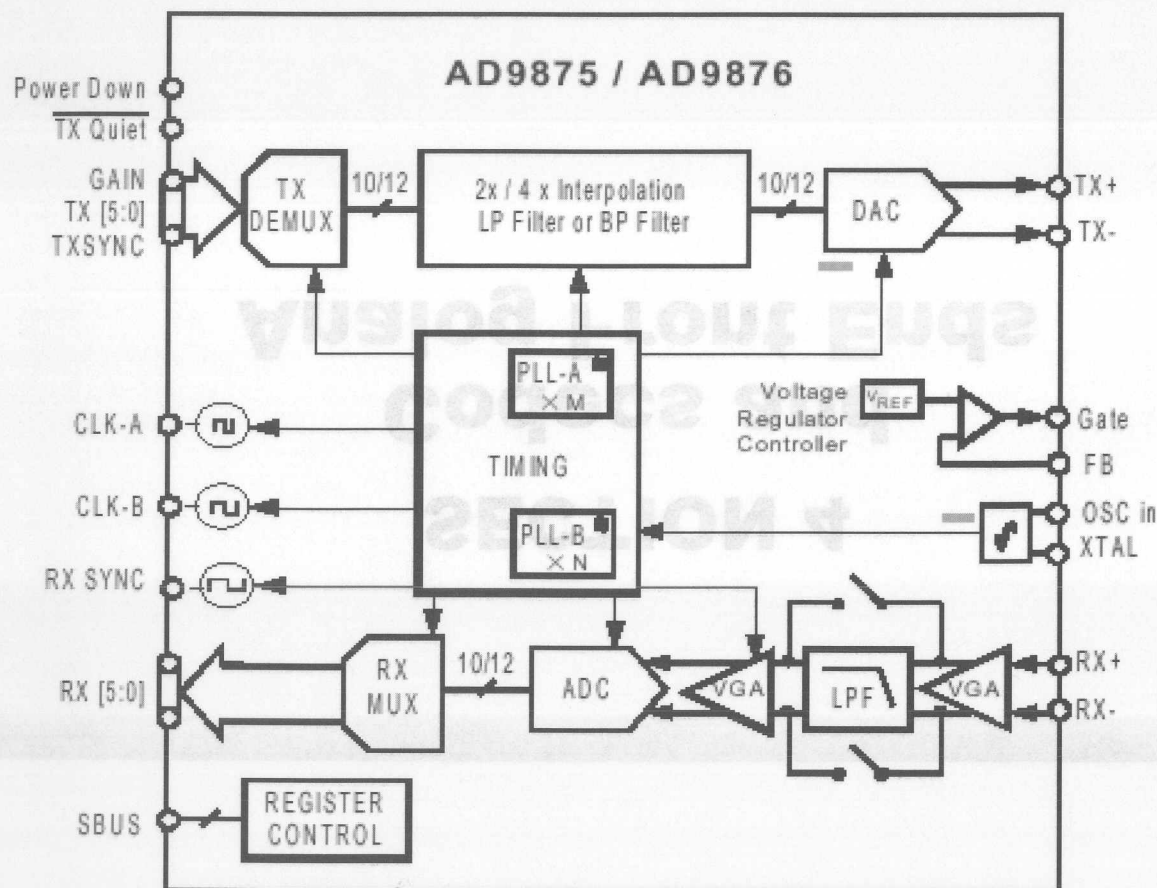
- 10 k Ω , 50 k Ω Terminal Resistance
- Linear or Log Taper
- Nonvolatile Memory Preset
- 14 Bytes of General-Purpose Nonvolatile Memory
- I²C Interface
- Increment/Decrement Push-Button Commands
- 3 V to 5 V Single Supply or ± 2.5 V Dual Supply
- 0.05 mW Dissipation



SECTION 4

Codecs and Analog Front Ends

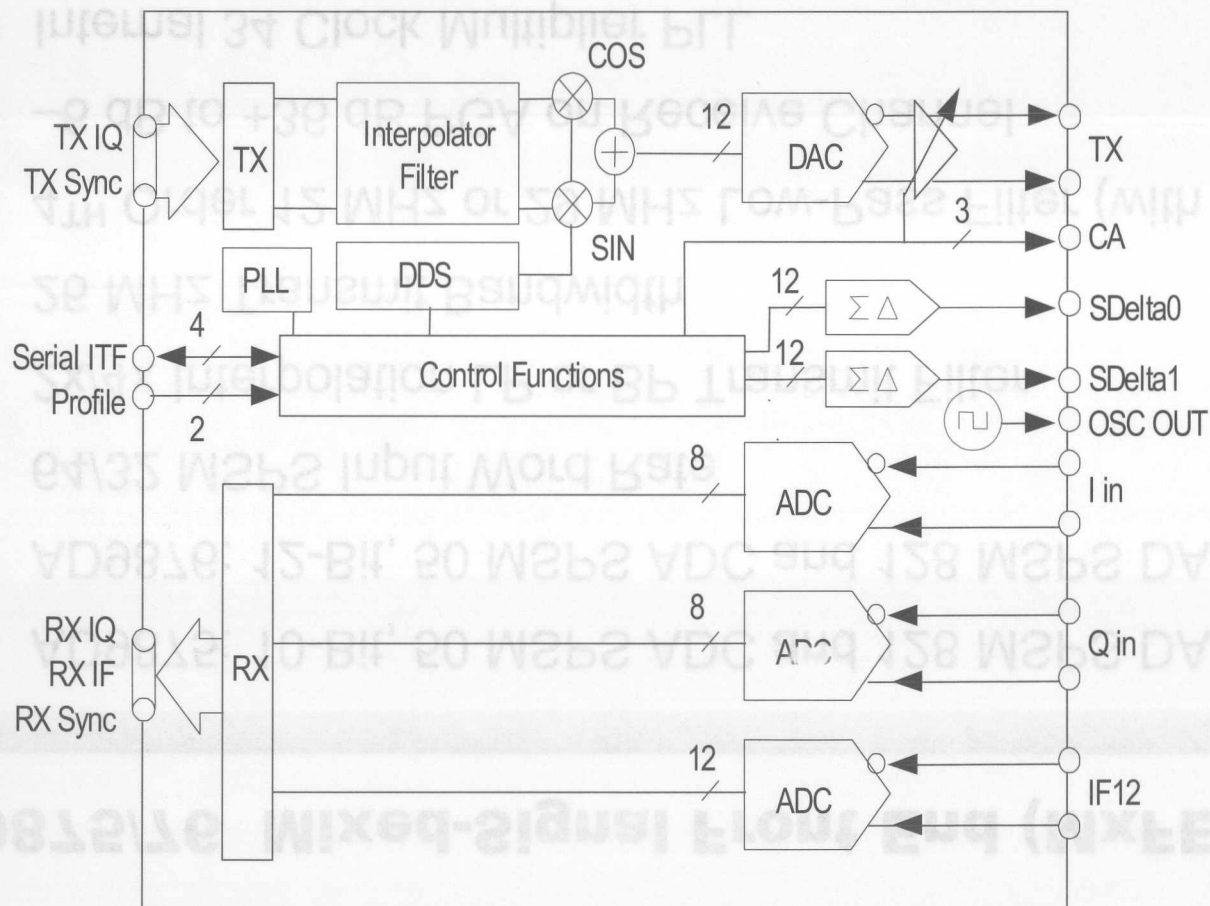
AD9875/76 Mixed-Signal Front End (MxFE™)



AD9875/76 Mixed-Signal Front End (MxFE™)

- AD9875: 10-Bit, 50 MSPS ADC and 128 MSPS DAC
- AD9876: 12-Bit, 50 MSPS ADC and 128 MSPS DAC
- 64/32 MSPS Input Word Rate
- 2x/4x Interpolation LP or BP Transmit Filter
- 26 MHz Transmit Bandwidth
- 4TH Order 12 MHz or 29 MHz Low-Pass Filter (with Bypass)
- -6 dB to +36 dB PGA on Receive Channel
- Internal 34 Clock Multiplier PLL
- Power-Down Mode

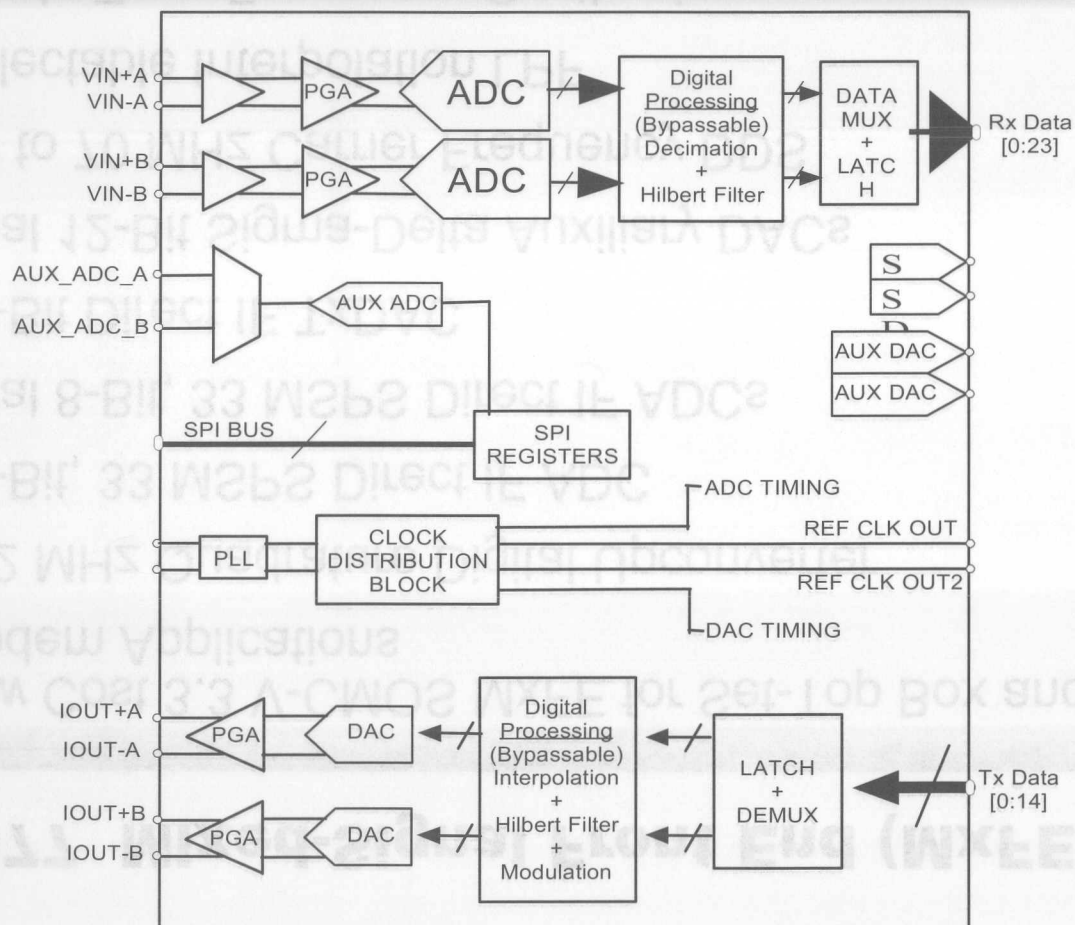
AD9877 Mixed-Signal Front End (MxFE™)



AD9877 Mixed-Signal Front End (MxFE™)

- Low Cost 3.3 V-CMOS MxFE for Set-Top Box and Cable Modem Applications
- 232 MHz Quadrature Digital Upconverter
- 12-Bit, 33 MSPS Direct IF ADC
- Dual 8-Bit, 33 MSPS Direct IF ADCs
- 12-Bit Direct IF TxDAC
- Dual 12-Bit Sigma-Delta Auxiliary DACs
- Up to 70 MHz Carrier Frequency DDS
- Selectable Interpolation LPF
- Single Tone Frequency Synthesis
- Analog Tx Output Level Adjust

AD9860/62 MxFE™ for Broadband Communications



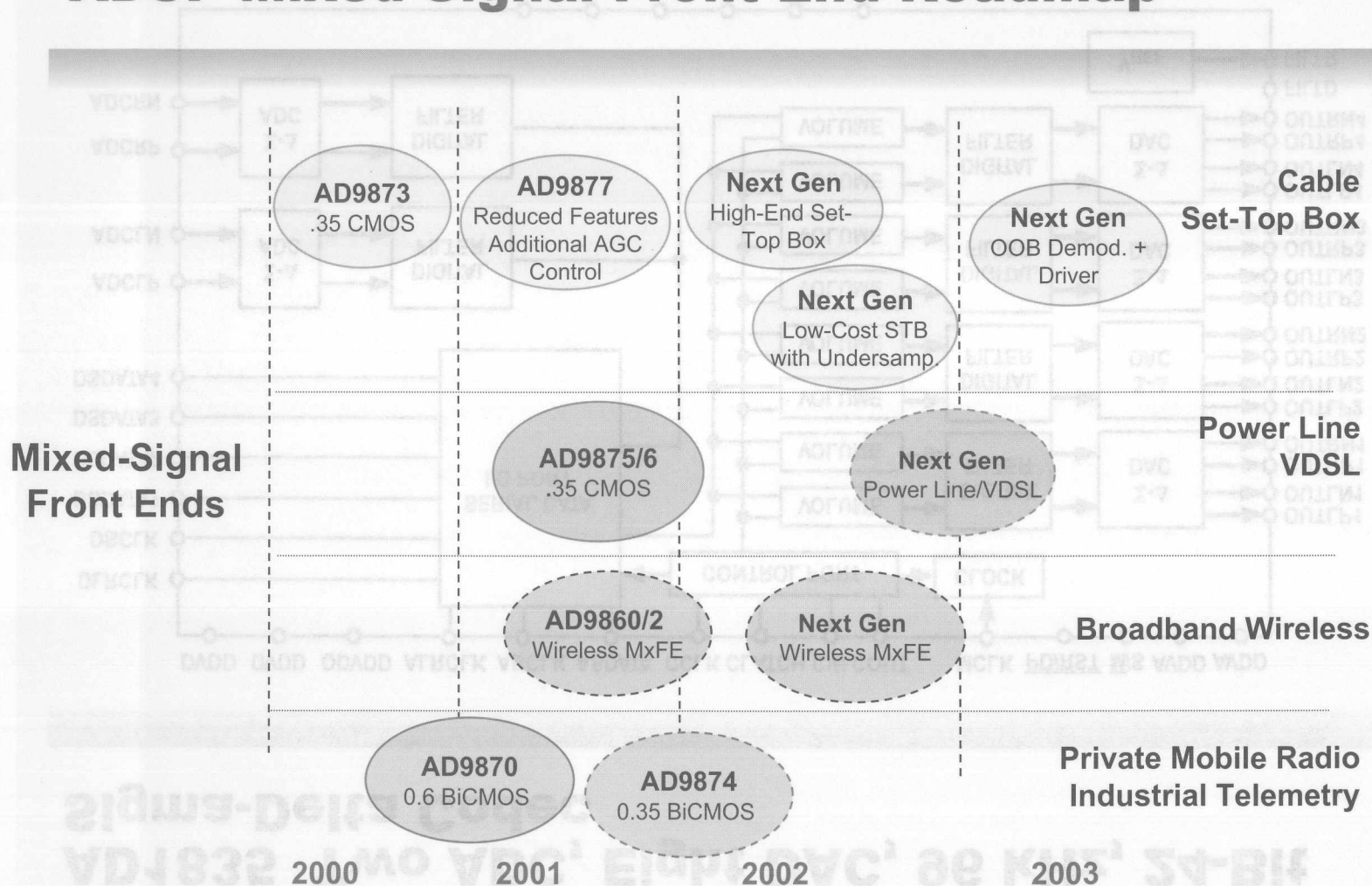
AD9860/62 MxFE™ for Broadband Communications

- A Versatile Mixed-Signal Front End Processor with Dual Receive and Dual Transmit Channels
- Dual 10-/12-Bit, 64 MSPS Sampling A/D Converters
- PGAs, Low-Pass Decimation Filters, and Digital Hilbert Block
- Dual 12-/14-Bit, 128 MSPS D/A Converters
- Programmable Full-Scale Output Current, Interpolation Filters, and Digital Hilbert Block
- Bypassable Digital Upconverters, Digital I/Q or Real Signal
- Internal Clock Distribution Block Including a Phase-locked Loop and Timing Generation Circuitry
- Programmable Output Clocks
- SPI Compliant Port, Two Programmable Sigma-Delta Outputs, Two Auxiliary DAC Outputs, Two Auxiliary ADC Inputs

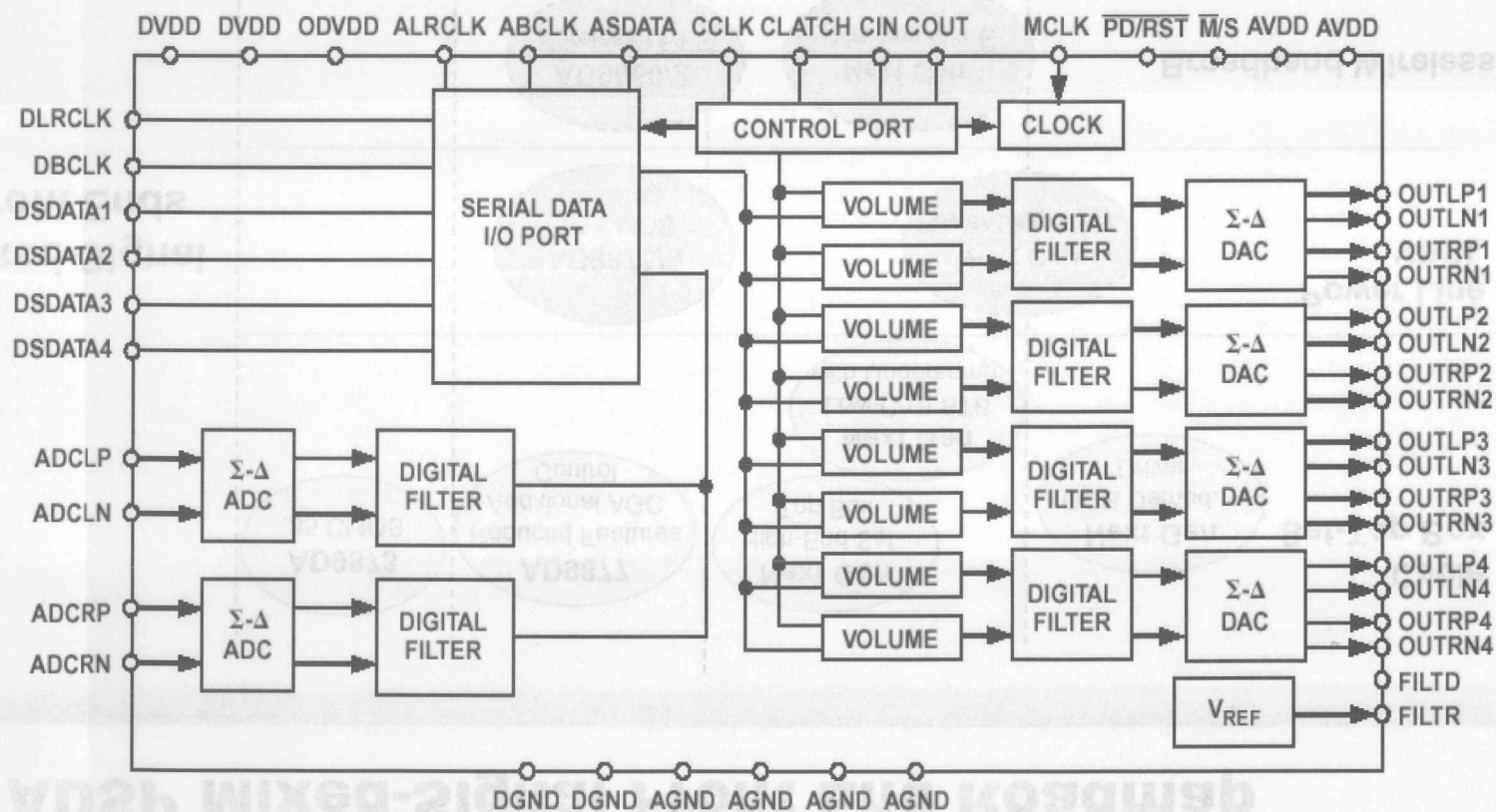
Cable Modem MxFE™ Matrix

Function	AD9873	AD9877	Next Gen	Next Gen
DDS (Bits)	26	28	28	26
Interpolation LPF	x12/x16	x12/x16	x12/x16	x16
Tx Sinc Function	Y	N	Y	Y
Tx Gain Adjustment	N	Y	Y	Y
IF ADC 1	12b	12b/US	12b/US	12b/US
IF ADC 2	10b	None	Dual 10b	10b
IF ADC 3	8b	8b	None	6b
Video Clamp	Y	N	Y	Y
Profiles	4	4	4	2
Auxiliary DACs	2	2	2	2
Cable Driver Interface	8321/3	8321/2/3/7	8321/2/3/7	8321/2/3/7

ADSP Mixed-Signal Front End Roadmap



AD1835 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec



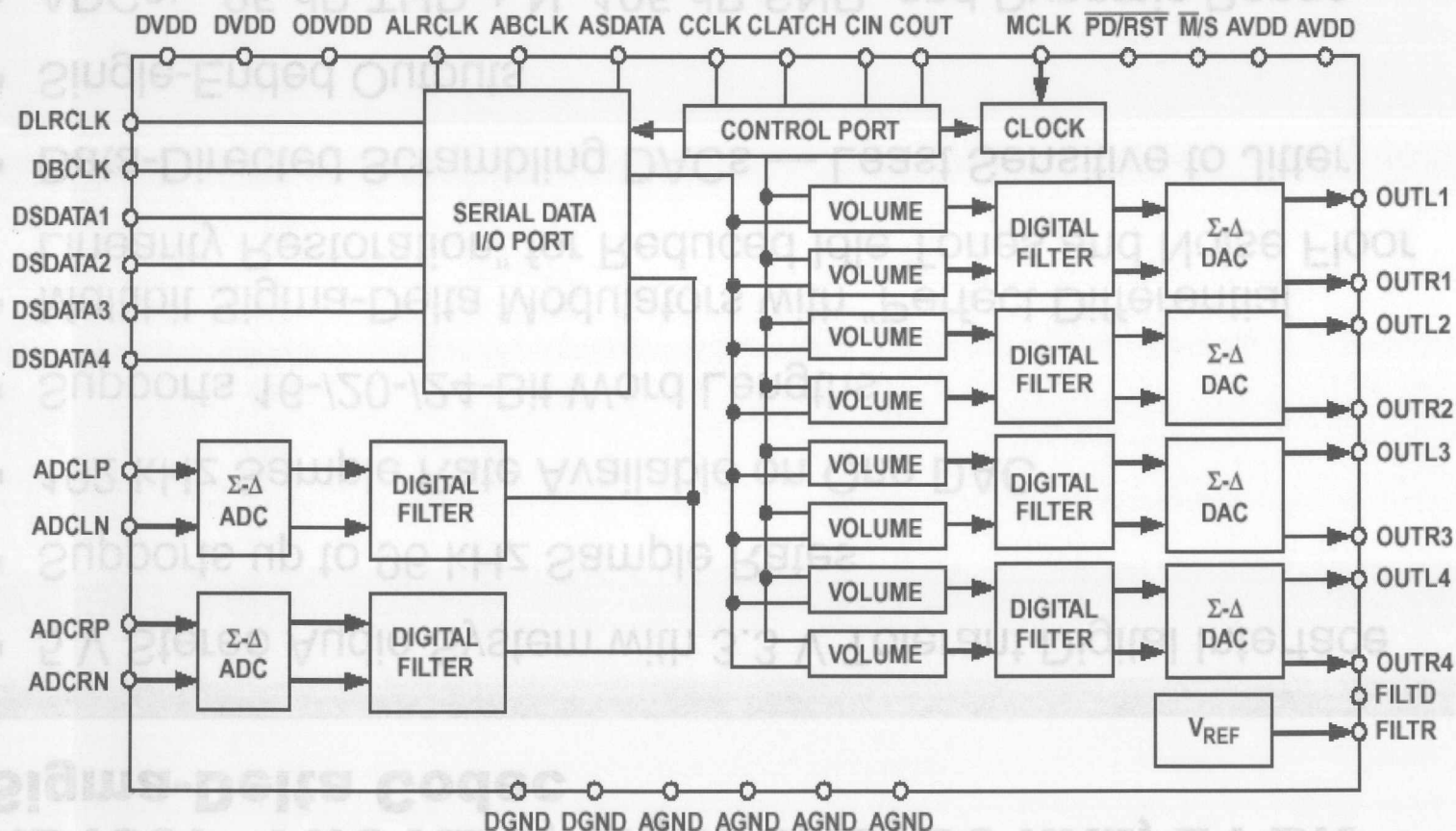
AD1835 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports up to 96 kHz Sample Rates
- 192 kHz Sample Rate Available on One DAC
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data-Directed Scrambling DACs — Least Sensitive to Jitter
- Differential Output for Optimum Performance
- ADCs: –95 dB THD + N, 105 dB SNR, and Dynamic Range
- DACs: –95 dB THD + N, 108 dB SNR, and Dynamic Range

AD1835 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024-Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing Supports $256 \times F_s$, $512 \times F_s$, and $768 \times F_s$ Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using Single SHARC SPORT
- 52-Lead MQFP Plastic Package

AD1837 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec



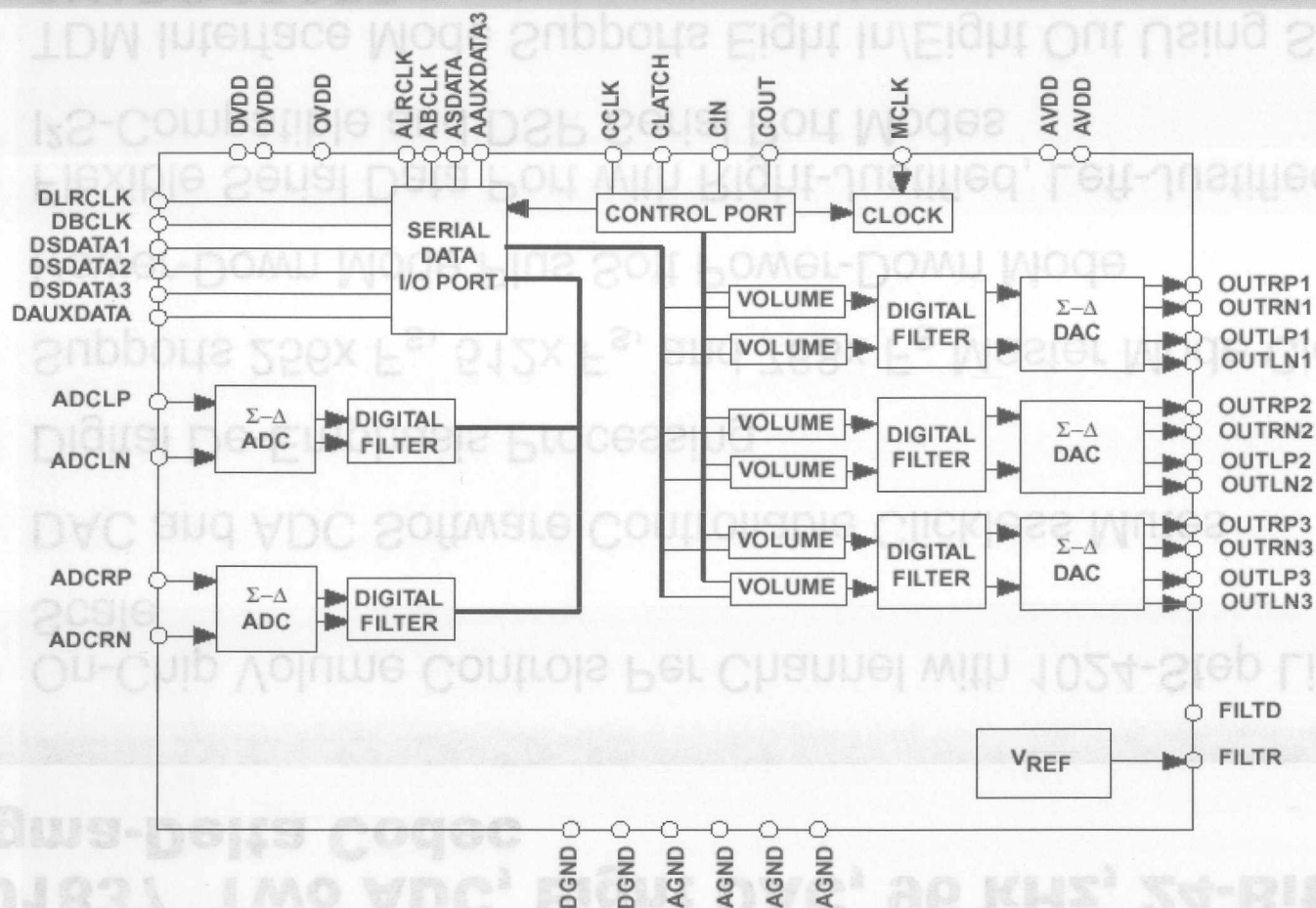
AD1837 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports up to 96 kHz Sample Rates
- 192 kHz Sample Rate Available on One DAC
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data-Directed Scrambling DACs — Least Sensitive to Jitter
- Single-Ended Outputs
- ADCs: -95 dB THD + N, 105 dB SNR, and Dynamic Range
- DACs: -92 dB THD + N, 108 dB SNR, and Dynamic Range

AD1837 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024-Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports $256 \times F_s$, $512 \times F_s$, and $768 \times F_s$ Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using Single SHARC SPORT
- 52-Lead MQFP Plastic Package

2144031



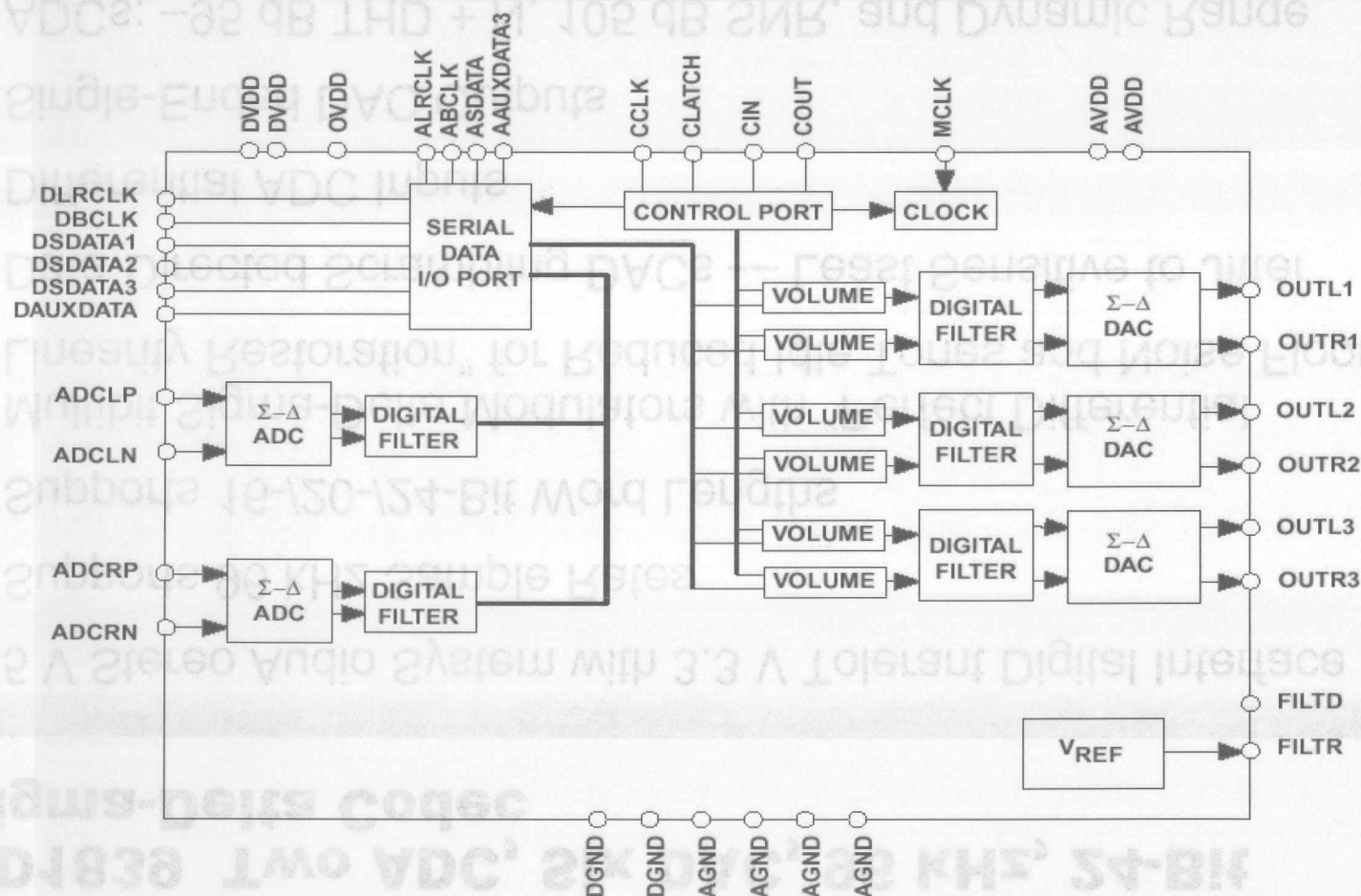
AD1838 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data-Directed Scrambling DACs — Least Sensitive to Jitter
- Differential Output for Optimum Performance
- ADCs: -95 dB THD + N, 105 dB SNR, and Dynamic Range
- DACs: -95 dB THD + N, 108 dB SNR, and Dynamic Range

AD1838 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024-Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports $256 \times F_s$, $512 \times F_s$ and $768 \times F_s$, Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using a Single SHARC SPORT
- 52-Lead MQFP Plastic Package

AD1839 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec



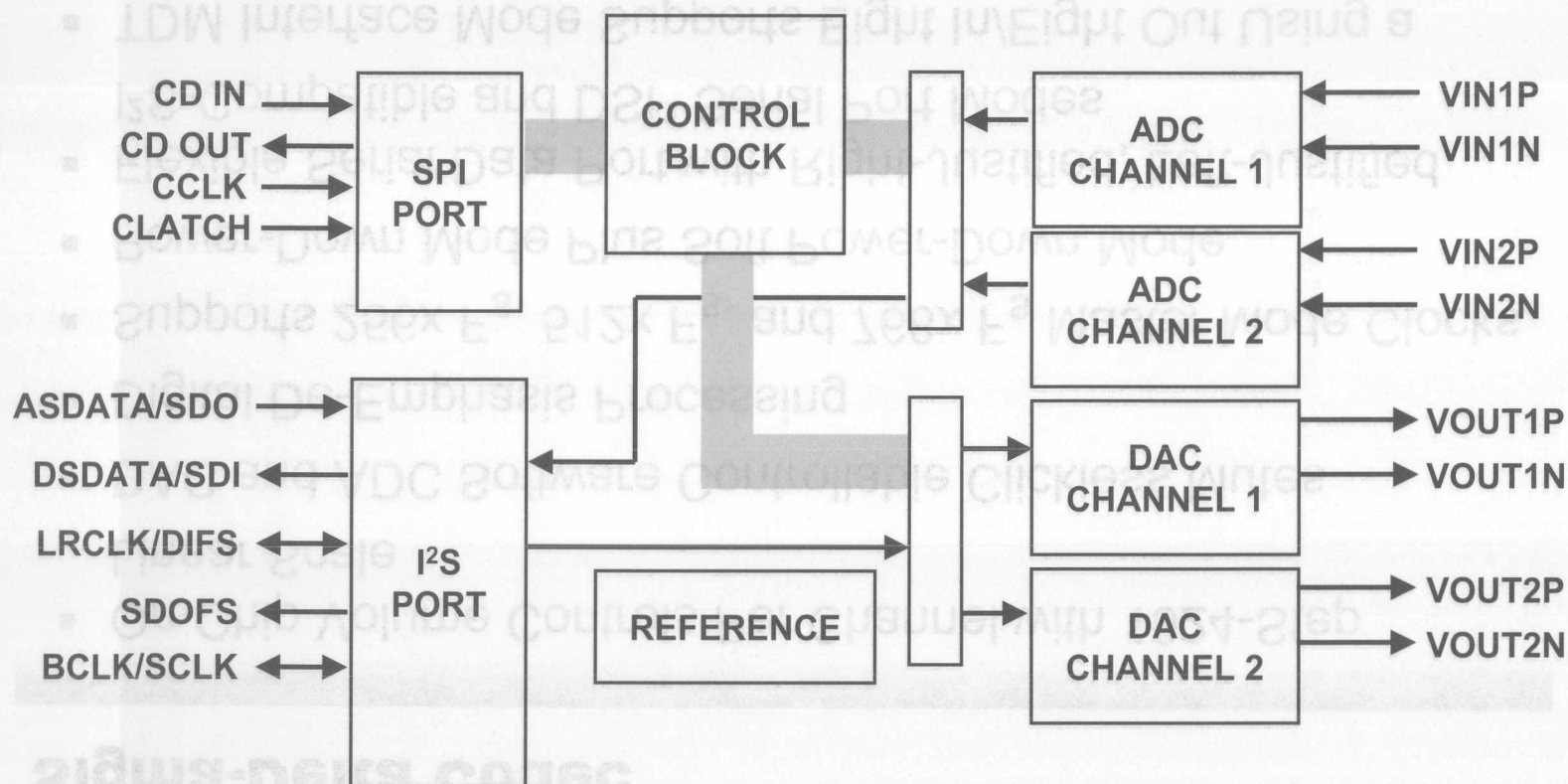
AD1839 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data-Directed Scrambling DACs — Least Sensitive to Jitter
- Differential ADC Inputs
- Single-Ended DAC Outputs
- ADCs: -95 dB THD + N, 105 dB SNR, and Dynamic Range
- DACs: -92 dB THD + N, 105 dB SNR, and Dynamic Range

AD1839 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024-Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports $256 \times F_s$, $512 \times F_s$, and $768 \times F_s$ Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using a Single SHARC SPORT
- 52-Lead MQFP Plastic Package

AD74322 Low-Cost Audio Analog Front End



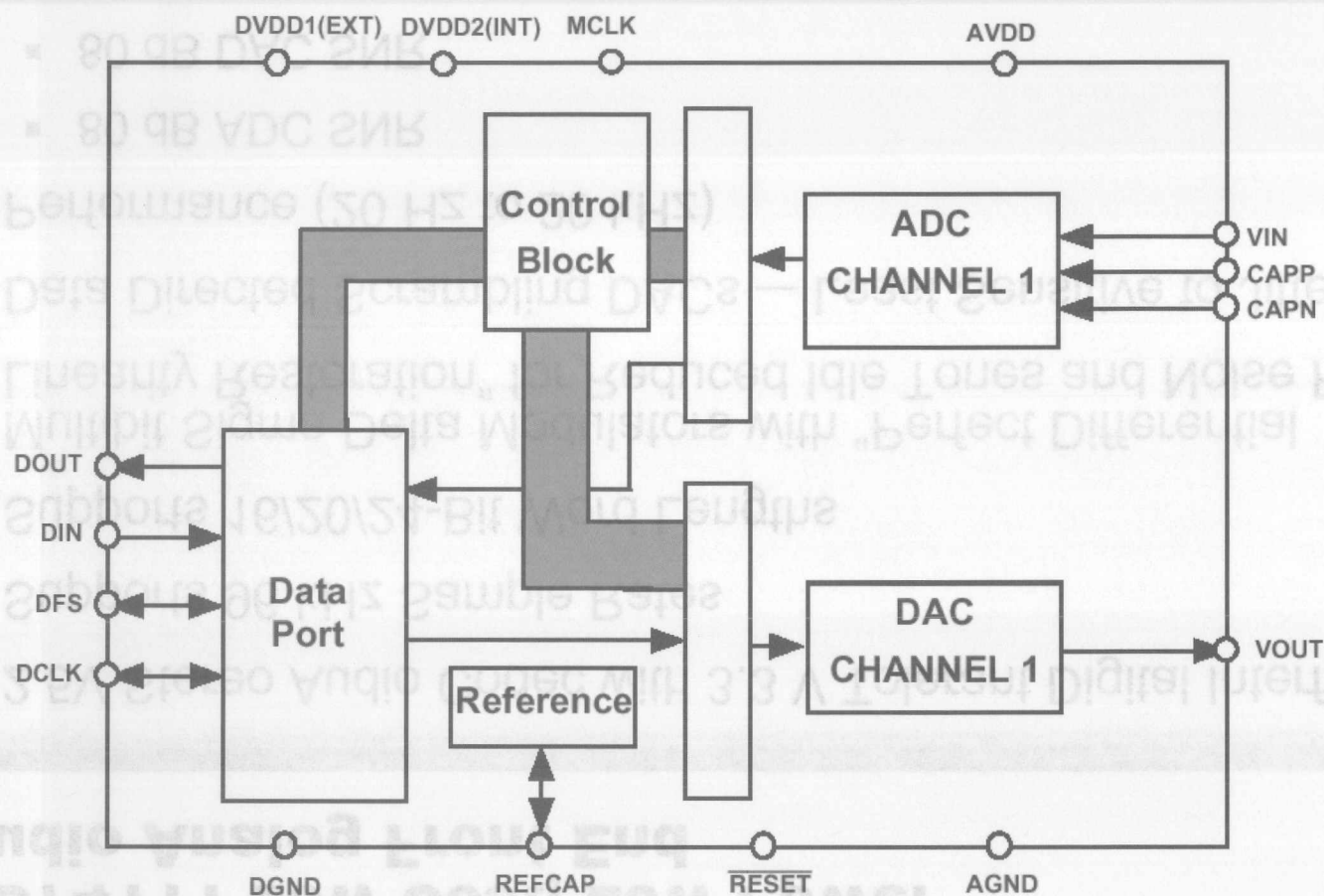
AD74322 Low-Cost Audio Analog Front End

- 2.5 V Stereo Audio Codec with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/18-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data-Directed Scrambling DAC — Least Sensitive to Jitter
- Differential Output for Optimum Performance
- Programmable Automatic Level Control on Input Channel
- Performance (20 Hz to 20 kHz): 90 dB ADC and DAC SNR
- Digitally Programmable Input/Output Gain On-Chip Volume Control

AD74322 Low-Cost Audio Analog Front End

- Digitally Programmable Input/Output Gain On-Chip
- Software Controllable Clickless Mute
- Digital De-Emphasis Processing
- Supports $256 \times F_s$, $512 \times F_s$, and $768 \times F_s$ Master Mode Clocks
- Master Clock Prescaler for Use with DSP Master Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- Supports Packed Data Mode (“TDM”) for Cascading Devices
- On-Chip Reference
- 20-Lead SOIC and TSSOP Packages

AD74111 Low Cost, Low Power Audio Analog Front End



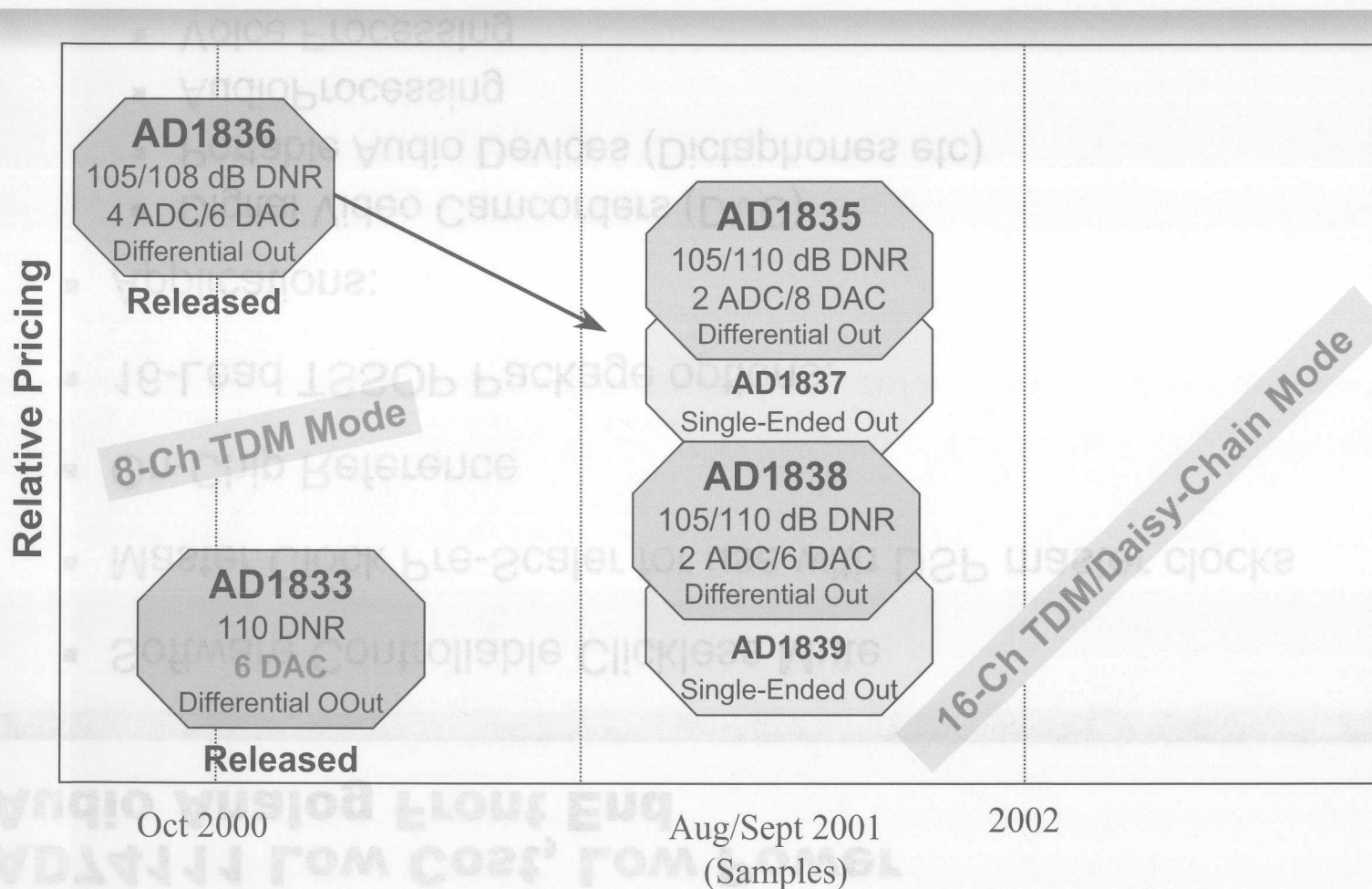
AD74111 Low Cost, Low Power Audio Analog Front End

- 2.5V Stereo Audio Codec with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16/20/24-Bit Word Lengths
- Multibit Sigma Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs — Least Sensitive to Jitter
- Performance (20 Hz to 20 kHz)
 - 80 dB ADC SNR
 - 80 dB DAC SNR
- Digitally Programmable Input/Output Gain
- On-chip Volume Control for Output Channel

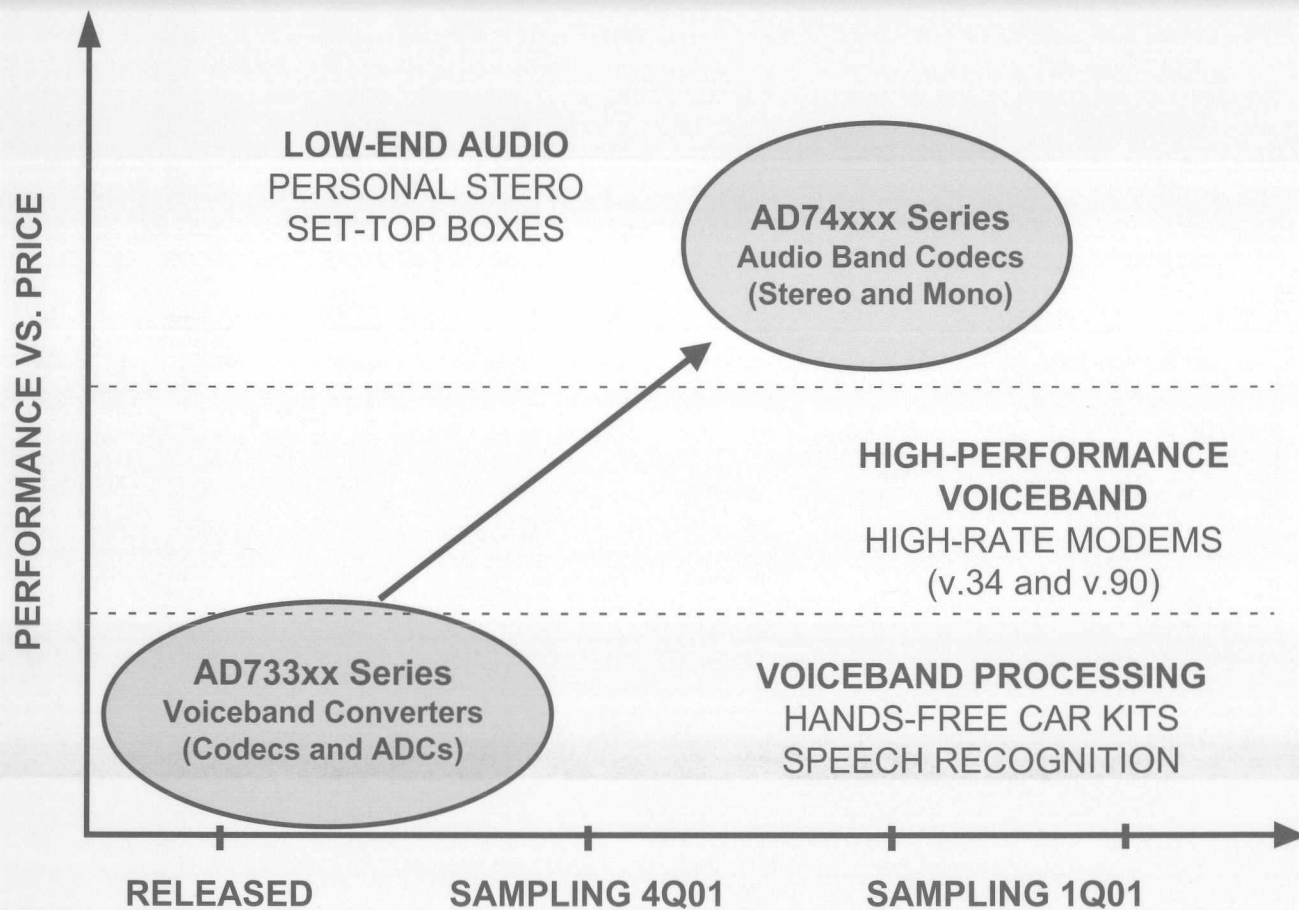
AD74111 Low Cost, Low Power Audio Analog Front End

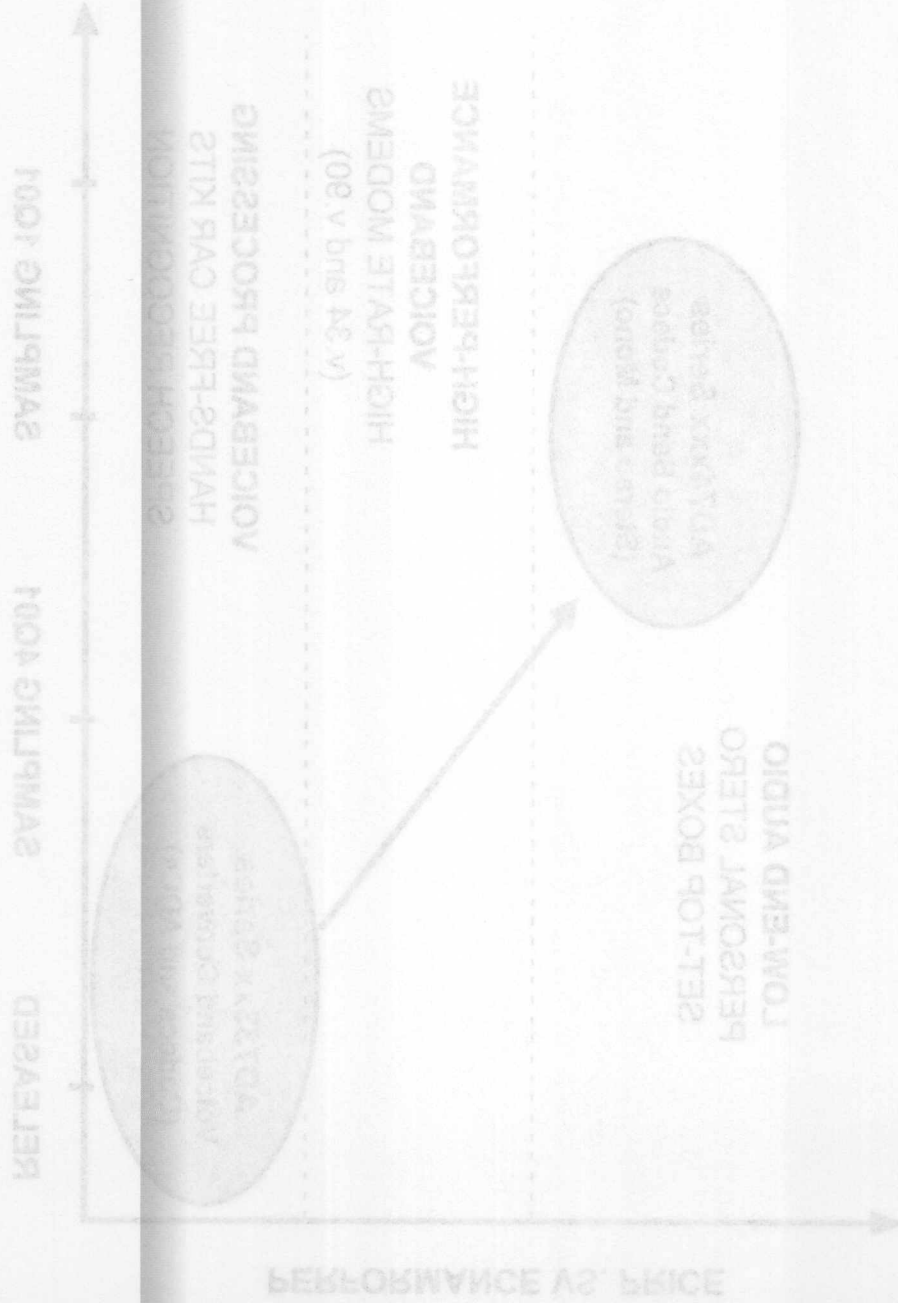
- Software Controllable Clickless Mute
- Master Clock Pre-Scaler for use with DSP master clocks
- On-Chip Reference
- 16-Lead TSSOP Package options.
- Applications:
 - Digital Video Camcorders (DVC)
 - Portable Audio Devices (Dictaphones etc)
 - AudioProcessing
 - Voice Processing
 - Conference Phones
 - General Purpose Analog I/O

Multichannel Codec Roadmap



Next Generation Codec Family





Next Generation Codec Family

SECTION 5

CONVERTER SUPPORT

MULTIPLEXERS

SWITCHES

MULTIPLEXERS

REFERENCES

REFERENCES

MULTIPLEXERS

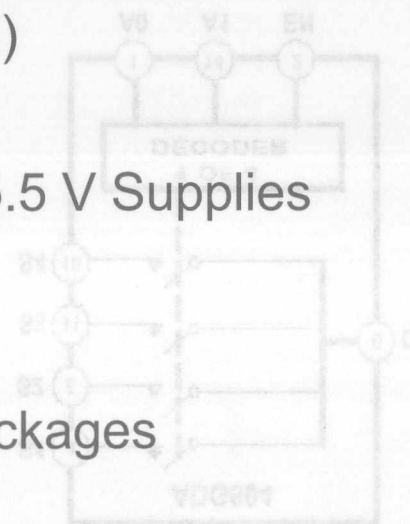
SWITCHES MULTIPLEXERS

CONVERTER SUPPORT

SECTION 2

ADG601/02 2.2 Ω CMOS ± 5 V/+5 V SPST Switches

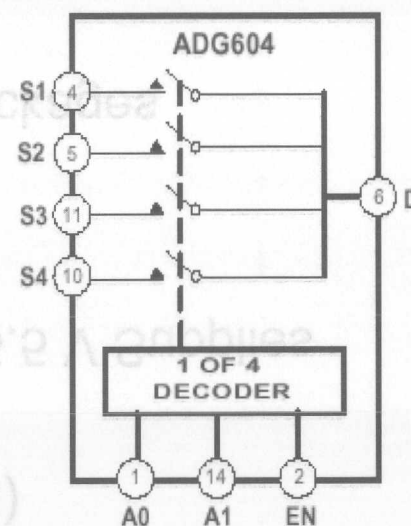
- Lowest Resistance ± 5 V Switches (3 Ω Max)
- <0.6 Ω ON-Resistance Flatness
- Dual ± 2.7 V to ± 5.5 V or Single +2.7 V to +5.5 V Supplies
- Rail-to-Rail Input Signal Range
- 40 ns Switching Times
- Tiny 6-Lead SOT-23 and 8-Lead μ SOIC Packages
- Low Power Consumption
- Ideal Instrumentation, Medical, and Communication Applications



ADG601 In	ADG602 In	Switch Condition
0	1	OFF
1	0	ON

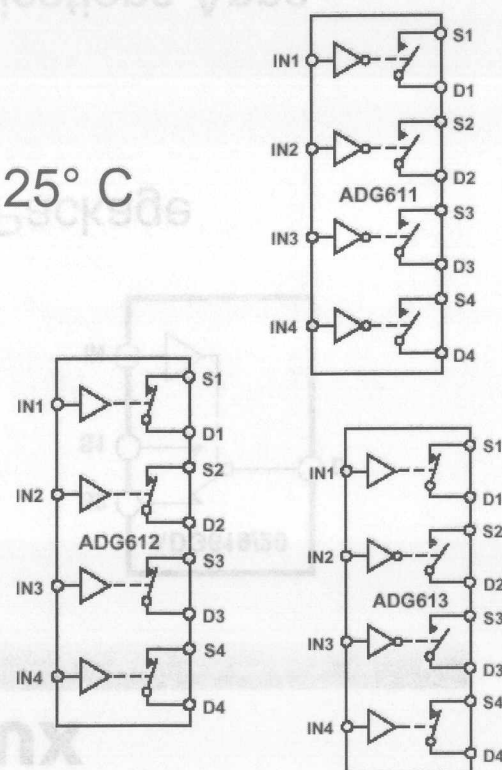
ADG604 1.5 pC Charge Injection, Low Leakage CMOS 4-Channel Multiplexer

- ± 1.5 pC Charge Injection Across Voltage Range
- ± 2.7 V to ± 5.5 V Dual Supply
- +2.7 V to +5.5 V Single Supply
- 100 pA max Leakage Current @ 25° C
- 85 Ω Typ ON Resistance
- Fully Specified at 125° C
- Rail-to-Rail Operation
- Fast Switching Times
- Typical Power Consumption (< 0.1 μ W)
- Ideal for Automotive and Industrial Applications
- 14-Lead TSSOP Package



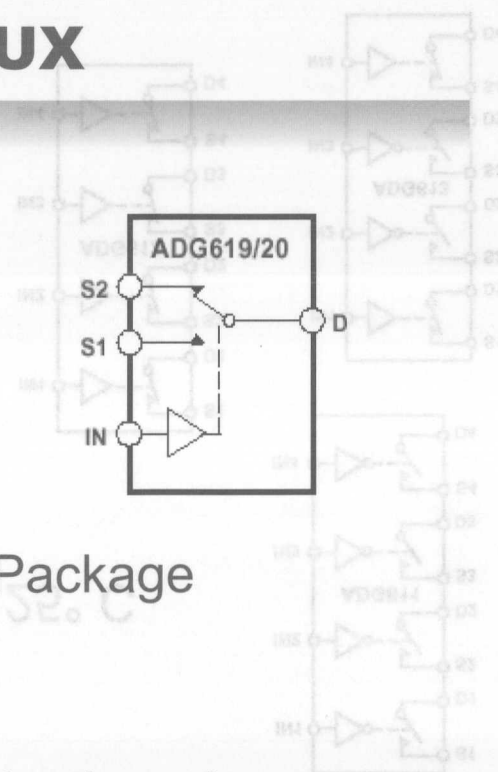
ADG611/12/13 1 pC Charge Injection, 100 pA Leakage, Quad SPST Switches

- ± 1.5 pC Charge Injection Across the Entire Voltage Range
- ± 2.7 V to ± 5.5 V Dual Supply
- +2.7 V to +5.5 V Single Supply
- Extended Temperature Range -40°C to $+125^{\circ}\text{C}$
- 100 pA max. Leakage Current @ 25°C
- $85\ \Omega$ ON Resistance
- Rail-to-Rail Switching Operation
- Fast Switching Times
- 16-Lead TSSOP Packages
- Typical Power Consumption ($<0.1\ \mu\text{W}$)
- Ideal for Automotive and Instrumentation



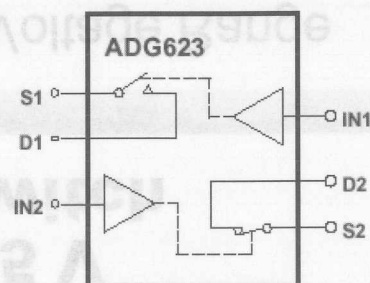
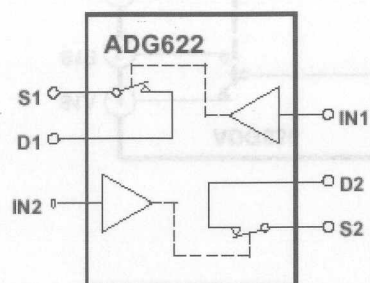
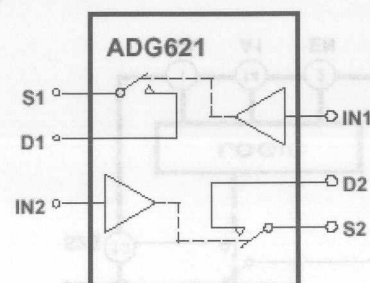
ADG619/20 CMOS ± 5 V/ +5 V 4 Ω Single SPDT Switches/ 2:1 MUX

- +2.7 V to +5.5 V Single Supply
- ± 2.7 V to ± 5.5 V Dual Supply
- 6 Ω (Max) ON Resistance
- 0.8 Ω (Max) ON-Resistance Flatness
- Rail-to-Rail Operation
- 8-Lead SOT-23 Package, 8-Lead μ SOIC Package
- Fast Switching Times
- Typical Power Consumption (<0.1 μ W)
- Ideal for Industrial, Medical, and Communications Apps
- ADG619 Break before Make
- ADG620 Make before Break



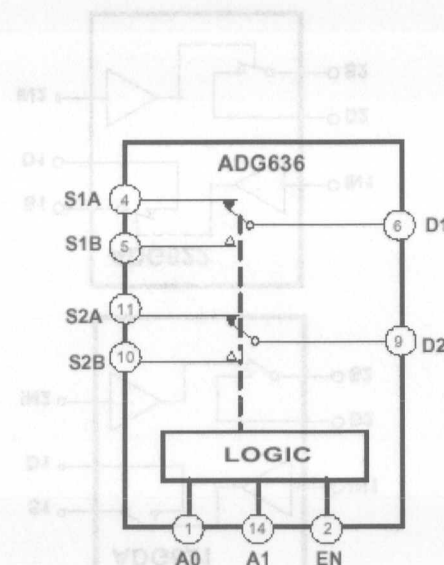
ADG621/22/23 CMOS ± 5 V/ 5 V 4 Ω Dual SPST Switches

- +2.7 V to +5.5 V Single Supply
- ± 2.7 V to ± 5.5 V Dual Supply
- 5.5 Ω (Max) ON Resistance
- 0.9 Ω (Max) ON-Resistance Flatness
- Rail-to-Rail Operation
- 10-Lead μ SOIC Package
- Fast Switching Times
- Typical Power Consumption (<0.01 μ W)
- ADG621 NO, ADG622 NC
- ADG623 NO/NC Configuration



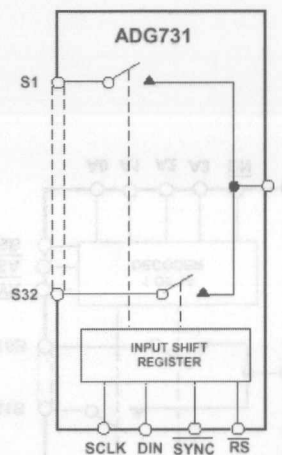
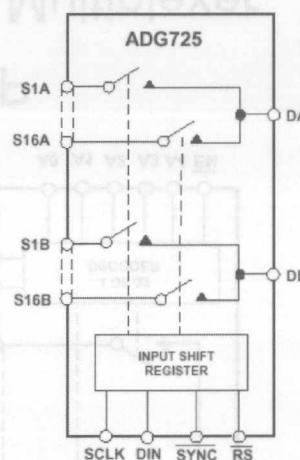
ADG636 1 pC Charge Injection, ± 5 V Low Leakage CMOS Dual SPDT Switch

- ± 1 pC Charge Injection Across the Entire Voltage Range
- ± 2.7 V to ± 5.5 V Dual Supply
- +2.7 V to +5.5 V Single Supply
- 100 pA max Leakage Current @ 25° C
- 85 Ω Typ ON Resistance
- Fully Specified at 125° C
- Rail-to-Rail Operation
- Fast Switching Times
- Typical Power Consumption (<0.1 μ W)
- Ideal for Automotive and Instrumentation Apps
- 14-Lead TSSOP Package



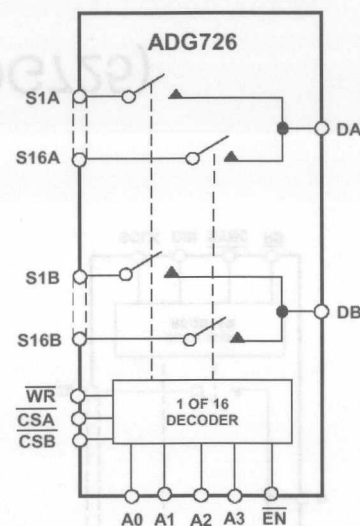
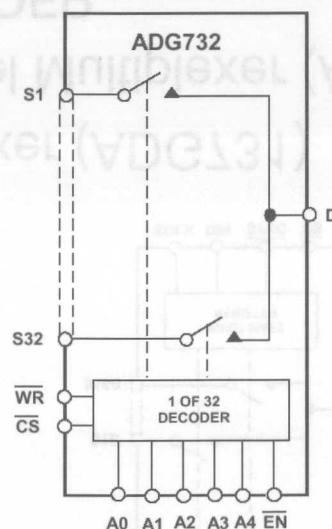
ADG731/25 16-/32-Channel, Serially Controlled 2.5 Ω Analog Mux

- 3-Wire SPI Serial Interface
- 1.8 V to 5.5 V Single Supply
- ± 2.5 V Dual Supply Operation
- 2.5 Ω ON Resistance
- 0.5 Ω ON-Resistance Flatness
- Rail-to-Rail Operation
- Power-On Reset
- Single 32- to 1-Channel Multiplexer (ADG731)
- Dual/Differential 16- to 1-Channel Multiplexer (ADG725)
- Available in 48-Lead CSP and TQFP
- Ideal for Optical Networking



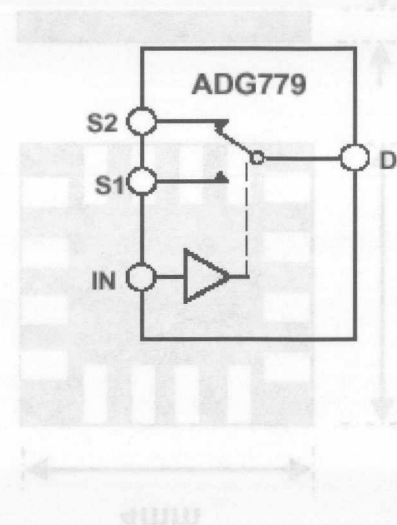
ADG732/26 32-Channel Low Voltage Analog Multiplexer

- +3 V, +5 V Supplies
- 2.5 Ω ON Resistance
- Low Ron Flatness
- Rail-to-Rail Operation
- Fast Switching Times
- Enable Input
- Low Power Consumption
- Available in 48-Lead CSP and TQFP
- Dual (Differential) 16- to 1-Channel Multiplexer (ADG726)
- Single 32- to 1-Channel Multiplexer (ADG732)
- Ideal for Optical Networking



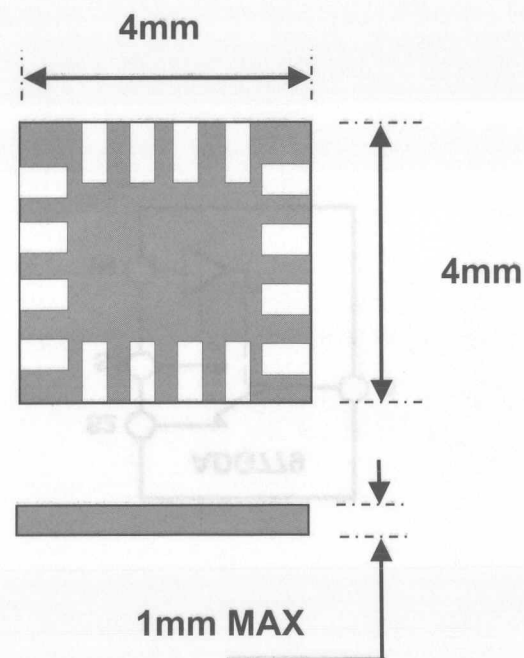
ADG779 CMOS Low Voltage 2.5 Ω SPDT Switch/ 2:1 Mux

- +1.8 V to +5.5 V Single Supply
- 5 Ω (Max) ON Resistance
- 0.75 Ω (Typ) ON-Resistance Flatness
- -3 dB Bandwidth > 200 MHz
- Rail-to-Rail Operation
- Tiny 6-Lead SC-70 Package
- Fast Switching Times
- $t_{ON} = 20$ ns, $t_{OFF} = 6$ ns
- Typical Power Consumption (<0.01 μ W)
- Low Cost Switch for Communications Applications



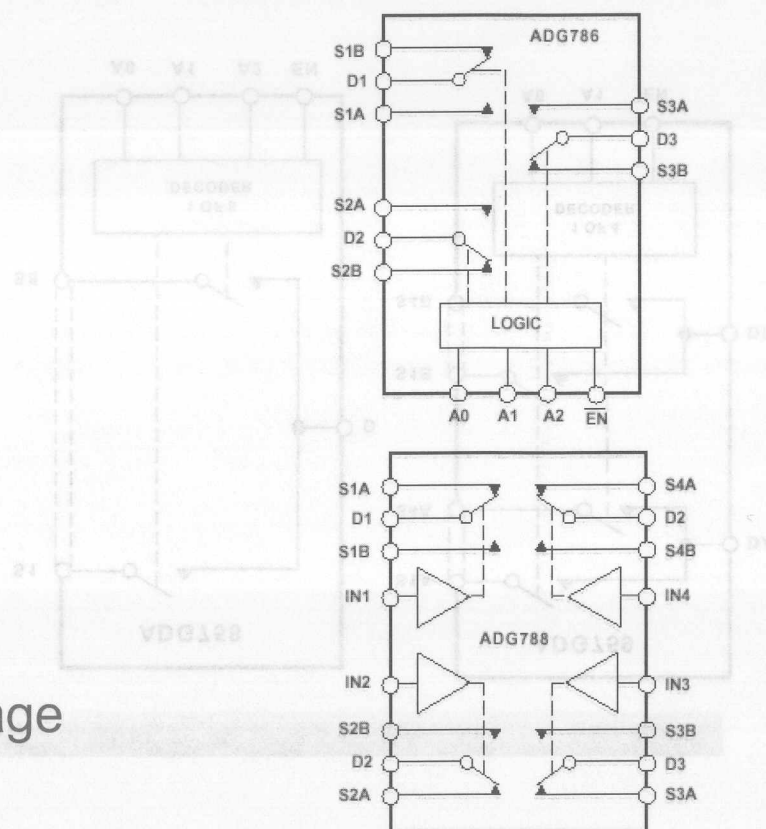
ADG78x Tiny CSP Switch/MUX Family

- R_{ON} 2.5 Ω (typ)
- +2.7 V to +5.5 V Operation
(Some Dual ± 2.5 V Operation)
- Quad SPST: ADG781/ADG782/ADG783
- Triple SPDT: ADG786
- Quad SPDT: ADG788
 - Independent control
- Quad SPDT: ADG784
 - Common control
- 50% Smaller than Equivalent Traditional Package



ADG786/88 CMOS, 2.5 Ω Low Voltage, Triple/Quad SPDT Switches in Chip Scale

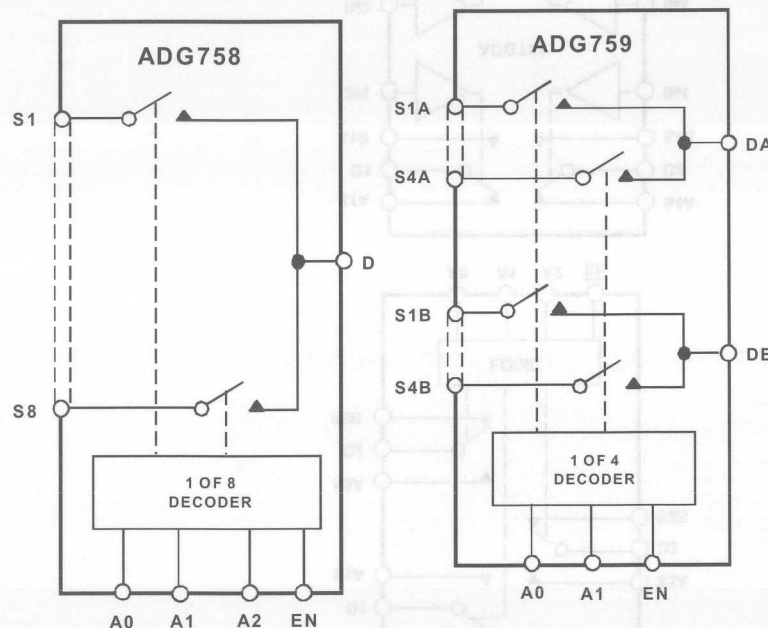
- +1.8 V to +5.5 V Single Supply
- ± 2.5 V Dual Supply
- 2.5 Ω ON Resistance
- 0.5 Ω ON-Resistance Flatness
- 100 pA Leakage Currents
- 19 ns Switching Times
- Triple SPDT: ADG786
- Quad SPDT: ADG788
- 4 mm x 4 mm Chip Scale Package
- Low Power Consumption
- ADG733/34 Equivalent in Traditional Package



ADG785/59 8-Ch/ Diff 4-Ch Multiplexers in Chip Scale Package

8-Ch/Diff 4-Channel MUX

- 1.8 V to 5.5 V single supply
- $\pm 3\text{V}$ dual supply
- 3Ω on resistance
- 0.75Ω on-resistance flatness
- 100 pA leakage typical
- 14 ns switching time
- $<0.01\text{ mW}$ power consumption
- ADG758 – 8:1 MUX
- ADG759 – Diff 4:1 MUX



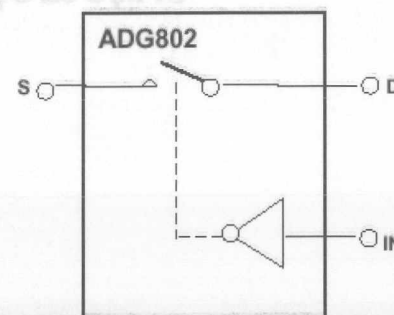
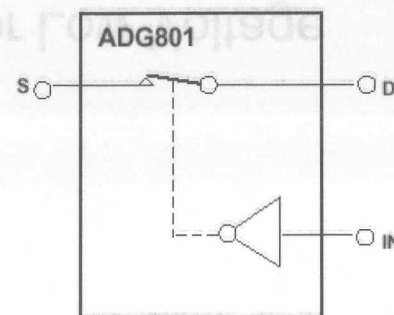
ADG8xx Family — Ultralow Resistance

- Lowest ON-Resistance Switches
 - (SPST <0.5 Ω , SPDT <1.0 Ω)
- Low Voltage Single and Dual Supply
- Operating Temperature to 125° C Ideal for Automotive Applications
- Small μ SOIC and SOT-23 Packages
- Entire Family Specified to 125° C
- Ultra-Low Resistance Makes ADG8xx Ideal for Low Voltage Handheld Battery-Powered Applications such as PDA etc.



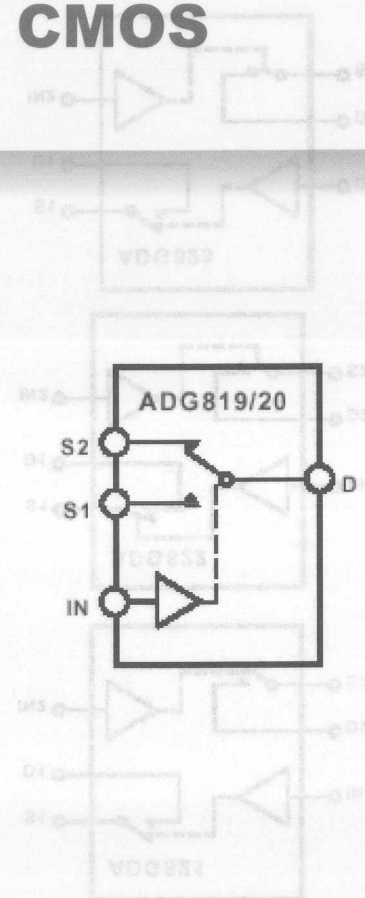
ADG801/02 <0.25 Ω Low Voltage CMOS SPST Switches

- 0.4 Ω Max Ron @ 5 V Supply & 125° C
- 0.08 Ω ON-Resistance Flatness
- +1.8 V to +5.5 V Single Supply
- 35 ns Switching Times
- Operates to 125° C
- 400 mA Current Carrying Capability
- Low Power Consumption
- TTL/CMOS Compatible Inputs
- Tiny 6-Lead SOT-23 and 8-Lead μ SOIC Packages



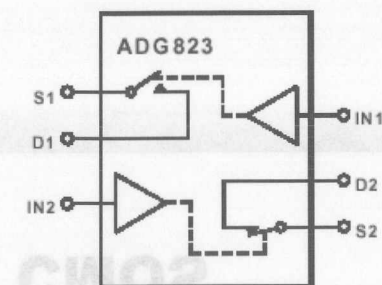
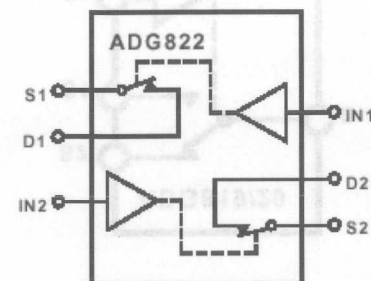
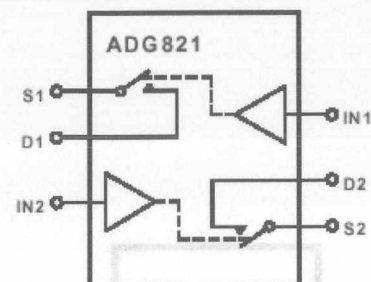
ADG819/20 1 Ω SPDT Low Voltage CMOS Switch

- +1.8 V to +5.5 V Single Supply
- 0.8 Ω (Max) ON Resistance
- 0.2 Ω (Max) ON-Resistance Flatness
- Rail-to-Rail Operation
- Operates to 125° C
- Fast Switching Times
- Typical Power Consumption (<0.01 μ W)
- TTL/CMOS Compatible Inputs
- ADG819 Break before Make
- ADG820 Make before Break
- Ideal for Handsets and PDAs
- 6-Lead SOT-23 Package, 8-Lead μ SOIC Package



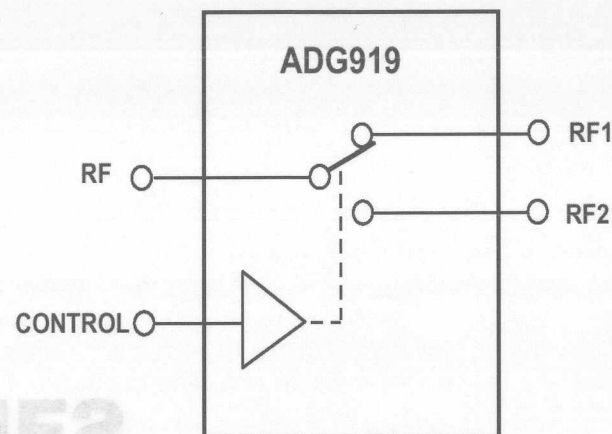
ADG821/22/23 1 Ω Dual SPST Low Voltage CMOS Switches

- +1.8 V to +5.5 V Single Supply
- 0.8 Ω (Max) ON Resistance
- 0.2 Ω (Max) ON-Resistance Flatness
- Rail-to-Rail Operation
- 8-Lead and 10-Lead μ SOIC Package
- Fast Switching Times
- Operates to 125° C
- Typical Power Consumption (<0.01 μ W)
- TTL/CMOS Compatible Inputs



ADG919 Wideband, 30 dB Isolation @ 1GHz, 1.65 V to 2.7 V, 2:1 Mux/SPDT CMOS Switch

- Wideband DC to 2 GHz
- High Off Isolation (30 dB @ 1 GHz)
- Low Insertion Loss:
(0.65 dB DC to 500 MHz)
- Single 1.65 V to 2.7 V power supply
- CMOS/LVTTL Control Logic
- Tiny 6 lead SC70 Package
- Low Power Consumption (5 μ A)



IN	ON SWITCH
0	RF1
1	RF2

• Low Power Consumption (2 nW)

• Tiny 8 Lead SO10 Package

BUS SWITCHES

• Single 1.8V to 5V Power Supply

• Low Insertion Loss:

(0.22 dB DC to 200 MHz)

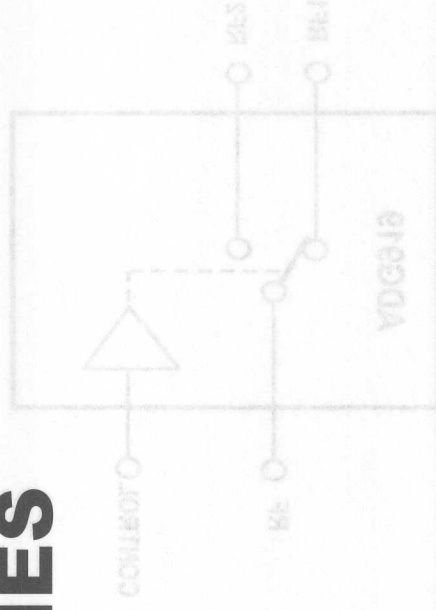
• High Off Isolation (30 dB @ 1 GHz)

• Wideband DC to 5 GHz

IN ON SWITCH

0 KE1

0 KE1



1.8V to 5V Single Supply CMOS Switch
ADG304 0.22 dB DC to 200 MHz, 30 dB Isolation @ 1GHz

ADG3245 2.5 V/ 3.3 V, 8 Bit, 2 Port Level Translator, Bus Switch

- 50 Tera 1280b/s CSB Packages

- 5.2 V to 1.8 V
- 3.3 V to 1.8 V
- 3.3 V to 5.2 V

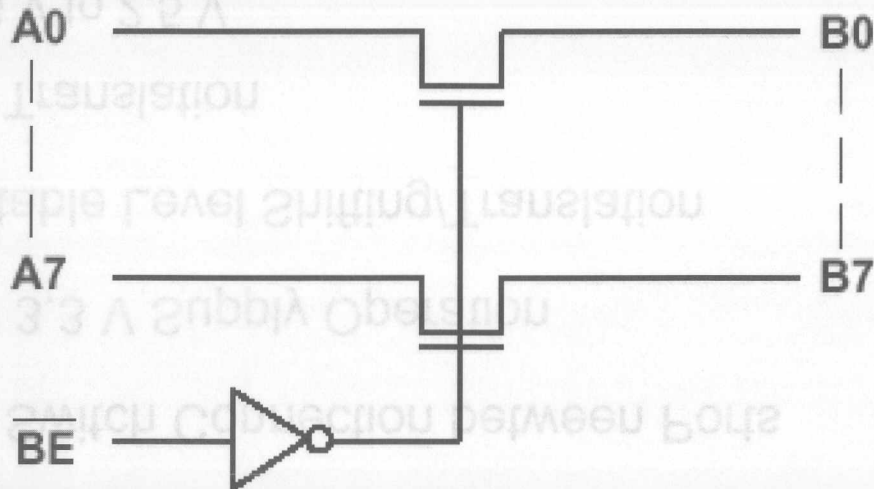
- Level Translation

- Selectable Level Shifting/Translation

- 5.2 V/ 3.3 V Supply Operation

- 3.2 V Switch Connection between Ports

- 175 ps Propagation Delay through the switch



Level Translator, Bus Switch

ADG3245 5.2 V/ 3.3 V, 8 Bit, 2 Port

ADG3245 2.5 V/ 3.3 V, 8 Bit, 2 Port Level Translator, Bus Switch

- 175 ps Propagation Delay through the switch
- 3.5 Ω Switch Connection between Ports
- 2.5 V/ 3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Level Translation
 - 3.3 V to 2.5 V
 - 3.3 V to 1.8 V
 - 2.5 V to 1.8 V
- 20 Lead TSSOP & CSP Packages

ADG3246 2.5 V/ 3.3 V, 10 Bit, 2 Port Level Translator, Bus Switch

- 54 Lead TSSOP and CSP Packages

• 5.2 V to 1.8 V

• 3.3 V to 1.8 V

• 3.3 V to 2.5 V

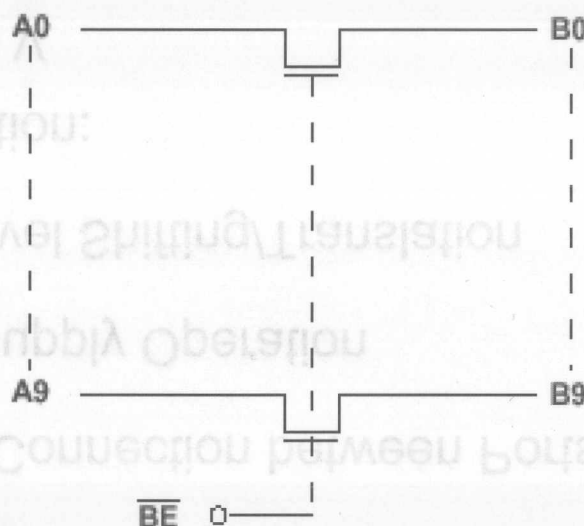
- Level Translation:

- Selectable Level Shifting/Translation

- 2.5 V/ 3.3 V Supply Operation

- 3.2 Ω Switch Connection between Ports

- 175 ns Propagation Delay through the switch



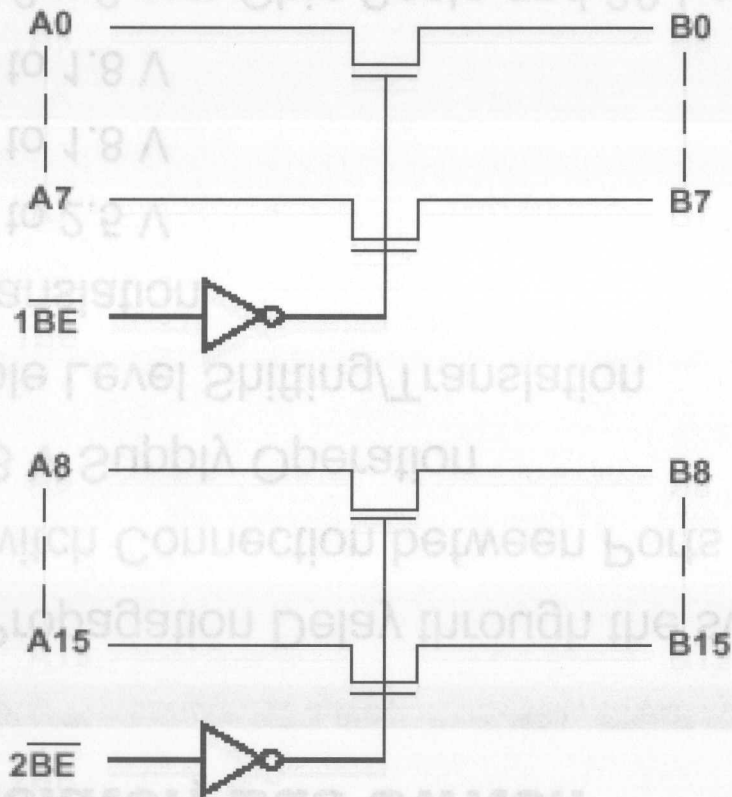
Level Translator, Bus Switch

ADG3246 2.5 V/ 3.3 V, 10 Bit, 2 Port

ADG3246 2.5 V/ 3.3 V, 10 Bit, 2 Port Level Translator, Bus Switch

- 175 ps Propagation Delay through the switch
- 3.5 Ω Switch Connection between Ports
- 2.5 V/ 3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Level Translation:
 - 3.3 V to 2.5 V
 - 3.3 V to 1.8 V
 - 2.5 V to 1.8 V
- 24 Lead TSSOP and CSP Packages

ADG3247 2.5 V/ 3.3 V, 16 Bit, 2 Port Level Translator, Bus Switch

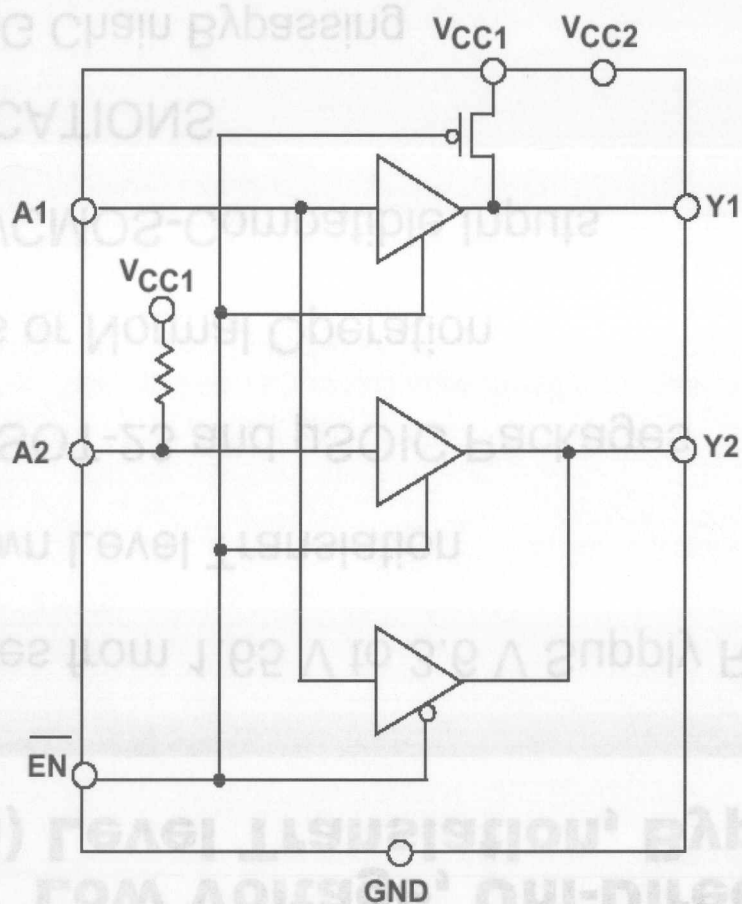


ADG3247 2.5 V/ 3.3 V, 16 Bit, 2 Port Level Translator, Bus Switch

- 175 ps Propagation Delay through the switch
- 3.5 Ω Switch Connection between Ports
- 2.5 V/3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Level Translation
 - 3.3 V to 2.5 V
 - 3.3 V to 1.8 V
 - 2.5 V to 1.8 V
- 40 Lead 6 x 6 mm Chip Scale and 38 Lead TSSOP Packages

Level Translator, Bus Switch
ADG3247 2.5 V/ 3.3 V, 16 Bit, 2 Port

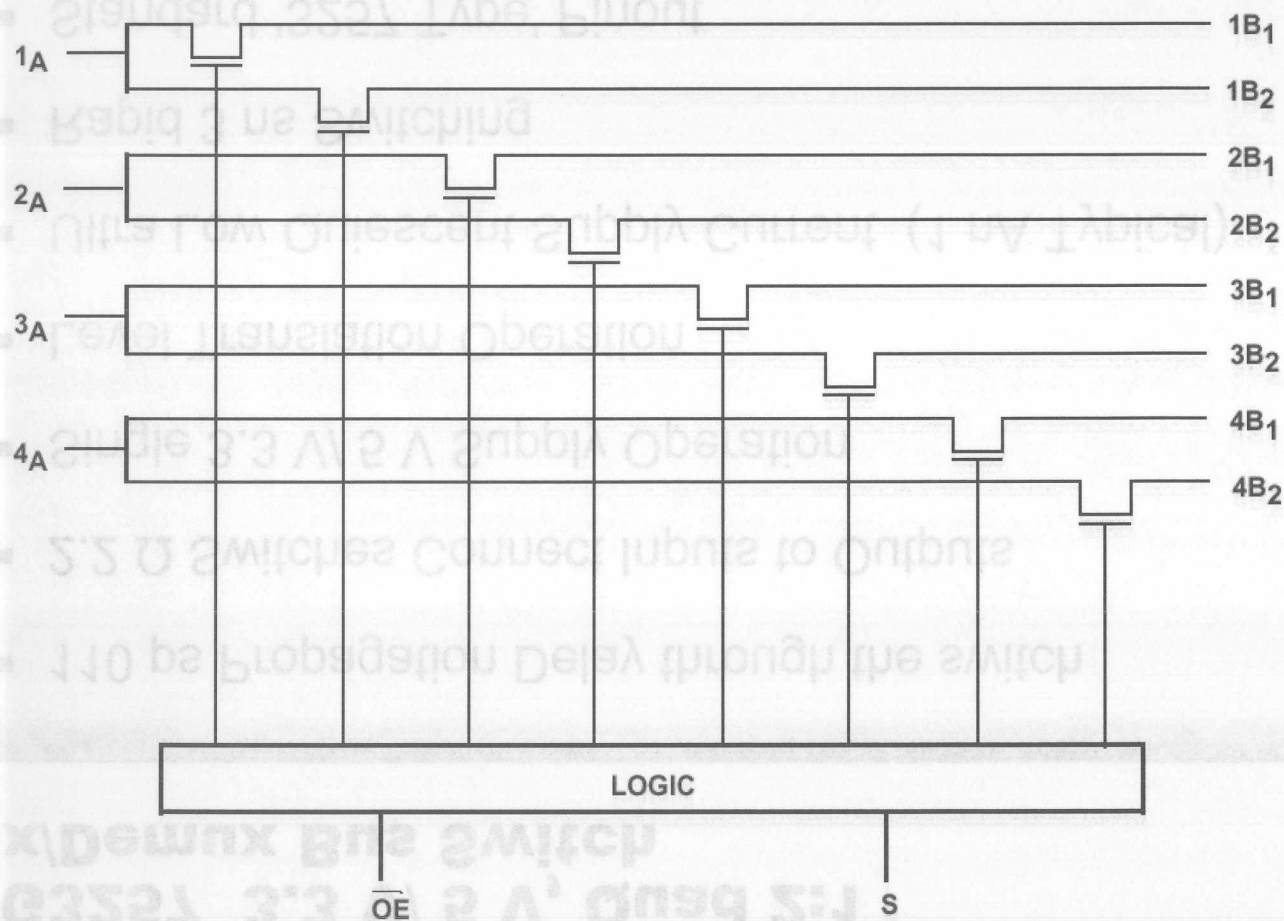
ADG3233 Low Voltage, Uni-Directional (Up/Down) Level Translation, Bypass Switch



ADG3233 Low Voltage, Uni-Directional (Up/Down) Level Translation, Bypass Switch

- Operates from 1.65 V to 3.6 V Supply Rails
- Up/Down Level Translation
- 8 lead SOT-23 and μ SOIC Packages
- Bypass or Normal Operation
- LVTTL/CMOS-Compatible Inputs
- APPLICATIONS
 - JTAG Chain Bypassing
 - Daisychain Bypassing
 - Digital Switching

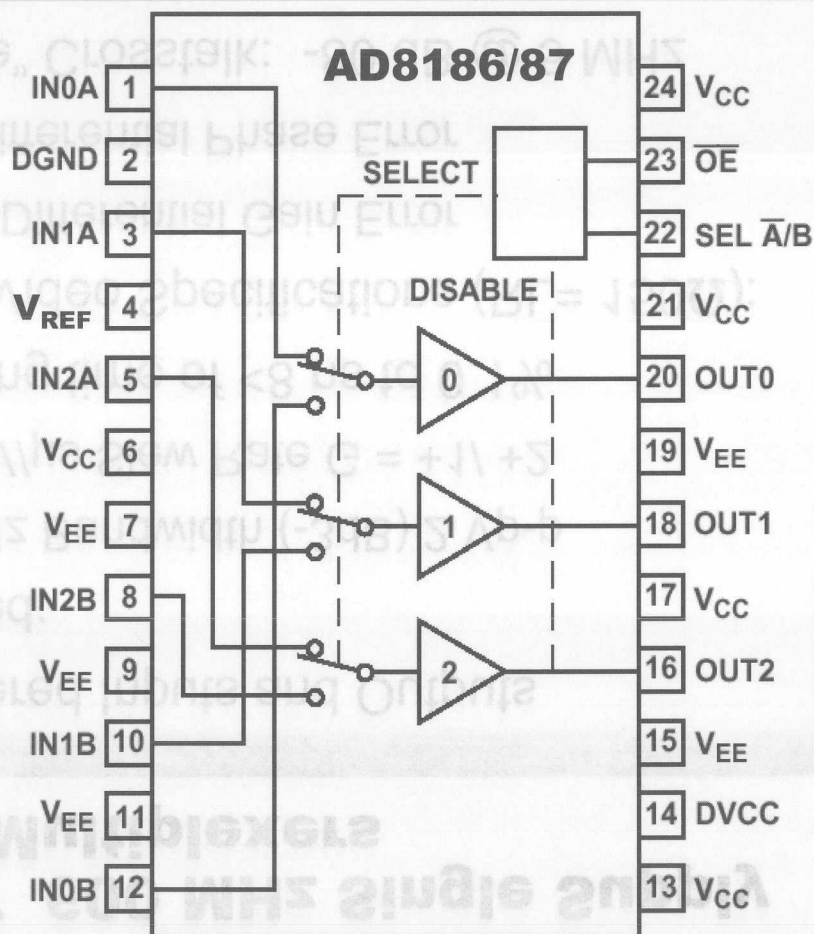
ADG3257 3.3 V/ 5 V, Quad 2:1 Mux/Demux Bus Switch



ADG3257 3.3 V/ 5 V, Quad 2:1 Mux/Demux Bus Switch

- 110 ps Propagation Delay through the switch
- 2.2 Ω Switches Connect Inputs to Outputs
- Single 3.3 V/ 5 V Supply Operation
- Level Translation Operation
- Ultra Low Quiescent Supply Current (1 nA Typical)
- Rapid 3 ns Switching
- Standard '3257 Type' Pinout
- 16 pin QSOP

AD8186/87 480 MHz Single Supply Triple 2:1 Multiplexers



TRUTH TABLE		
SEL A/B	$\bar{O}E$	OUT
0	0	High Z
1	0	High Z
1	1	INA
0	1	INB

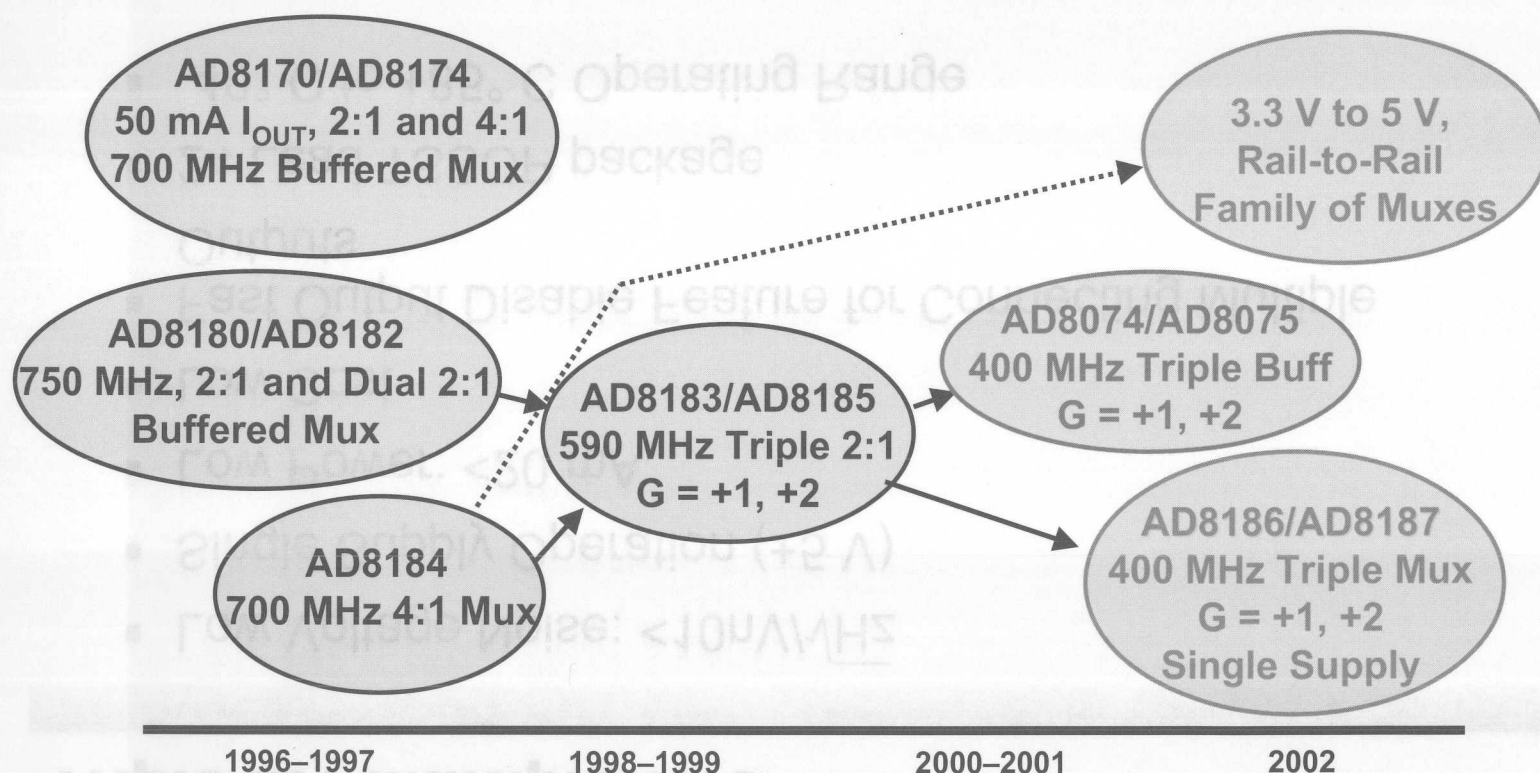
AD8186/87 600 MHz Single Supply Triple 2:1 Multiplexers

- Fully Buffered Inputs and Outputs
- High Speed:
 - 480 MHz Bandwidth (-3dB) 2 Vp-p
 - >1400 V/ μ s Slew Rate $G = +1/ +2$
- Fast Settling time of <8 ns to 0.1%
- Excellent Video Specifications ($R_L = 150\Omega$):
 - 0.01 % Differential Gain Error
 - 0.01° Differential Phase Error
- “All Hostile” Crosstalk: -80 dB @ 5 MHz
 - -50 dB @ 100 MHz
- High “OFF” Isolation of 90 dB @ 5 MHz

AD8186/87 600 MHz Single Supply Triple 2:1 Multiplexers

- Low Voltage Noise: $<10\text{nV}/\sqrt{\text{Hz}}$
- Single Supply Operation (+5 V)
- Low Power: $<20\text{ mA}$
- Low Cost
- Fast Output Disable Feature for Connecting Multiple Outputs
- 24 Lead TSSOP package
- -40° C to $+85^{\circ}\text{ C}$ Operating Range

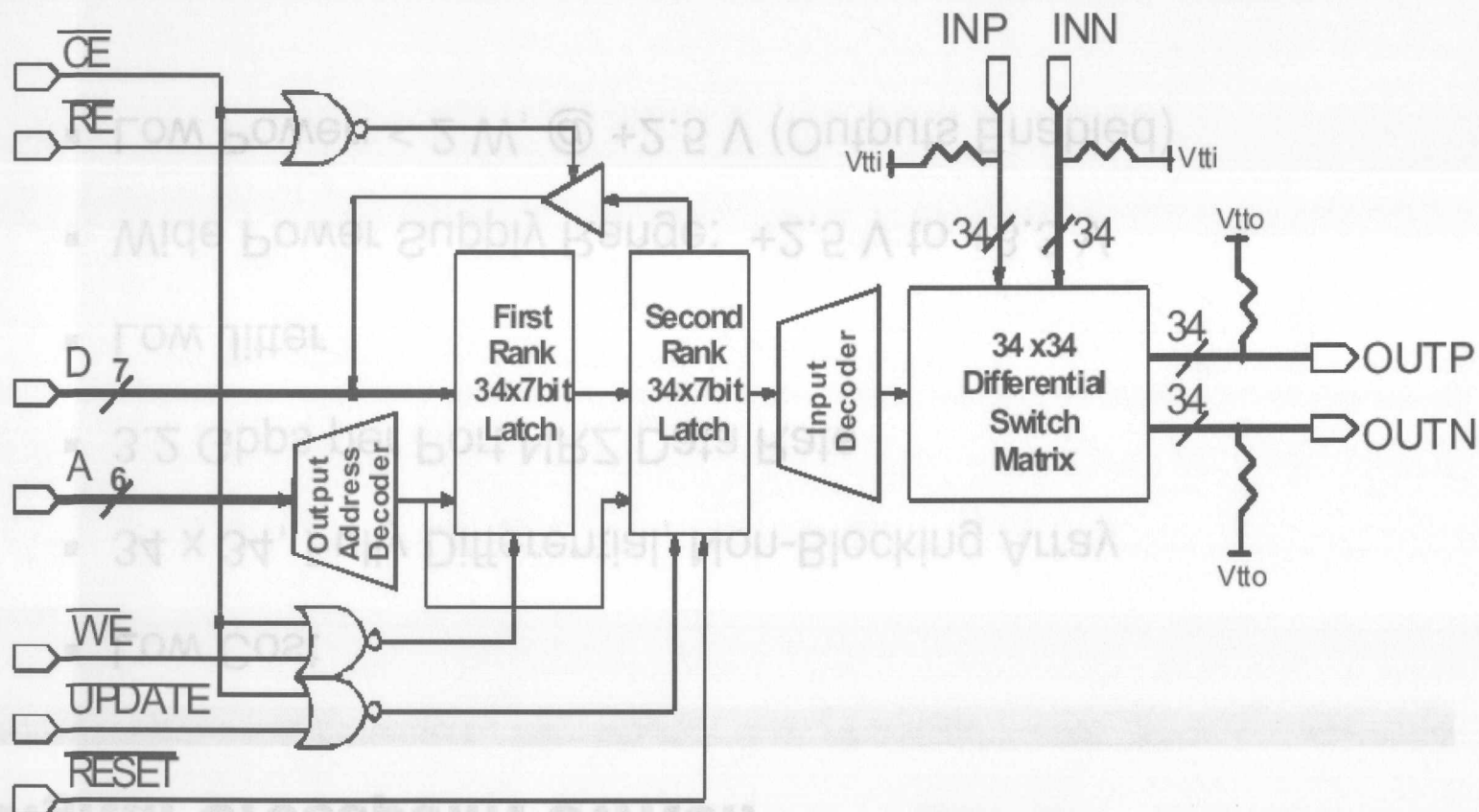
High-Speed Buffered Multiplexer Road Map



AD8152

Xstream™

34 x 34, 3.2 Gb/s Digital Crosspoint Switch



AD8152

AD8152 *Xstream*[™] 34 x 34, 3.2 Gb/s Digital Crosspoint Switch

- Low Cost
- 34 x 34, Fully Differential, Non-Blocking Array
- 3.2 Gbps per Port NRZ Data Rate
- Low Jitter
- Wide Power Supply Range: +2.5 V to +3.3 V
- Low Power: < 2 W, @ +2.5 V (Outputs Enabled)

AD8152 *Xstream*TM 34 x 34, 3.2 Gb/s Digital Crosspoint Switch

- PECL Compatible LVTTTL CMOS/TTL- Level Control Inputs
 - Drives a Backplane Directly
 - Programmable Output Swing: 200 mV -1V Differential
 - Optimize Termination Impedance
 - User-Controlled Voltage at the Load Minimize Power Dissipation
- Individual Output Disable for Busing and Building Larger Arrays
- Double Row Latch
- Available in 256-Lead BGA

• **ACQ** baeJ-022 ni eldalisVA

• **Double Row Latch**

Analysis

• **Individual Output** tending Larger

Dissipation

- **User-Controlled Voltage at the Load** Minimize Power
- **Optimize Termination Impedance**
- **Programmable Output Swing: 500 mV - 1V Differential**
- **Drives a Backplane Directly**

Inputs

• **PECL Compatible LVTTL CMOS Level Control**

Digital Crosspoint Switch
AD8125 34 x 34, 3.5 Gb/s

ADR01/02 Ultra Compact Precision 10.0 V/ 5.0 V Reference

- Ultra Compact SC70-5/ SOT23-5 Package
- Low Temperature Coefficient: 3 ppm/°C
- Long Term Stability: 50 ppm/ 1000 hr
- Line Regulation: 30 ppm/V
- Load Regulation: 50 ppm/mA
- Low Noise: 25 μ Vp-p (0.1 Hz to 10 Hz)
- Low Hysteresis: 70 ppm Typical
- Wide Operating Range
 - ADR01: 12 V to 40 V
 - ADR02: 7 V to 40 V
- Quiescent Current: 1 mA Max
- High Output Current: 10 mA
- Wide Temperature Range: -40° C to +125° C

ADR280 1.20 V Low Power Voltage Reference

- Wide Temperature Range: -40°C to $+125^{\circ}\text{C}$
- High Output Current: 10 mA
- 1.20 V Precision Output Voltage
- 80dB Ripple Rejection
- Low Noise
- Low Hysteresis: 10 ppm Typical
- Low Power
- Load Regulation: 50 ppm/V
- Compact 3-lead SOT-23 package
- Long Term Stability: 50 ppm/1000 hr
- Low Temperature Coefficient: 3 ppm/ $^{\circ}\text{C}$
- Ultra Compact SOT-23 Package

1.20 V 1.20 V Reference

ADR280/285 Ultra Compact Precision

ADR318/390/391/393/395 References in Automotive Temp Range (–40 °C to +125 °C)

- 1.800 V, 2.048 V, 2.500 V, 4.096 V & 5.000 V Outputs
- Compact SOT23-5, 3x3mm Package
- Shutdown Pin
- 25 ppm/°C Tempco
- Applications : Automotive, Fault Protection Critical Applications

ADR392/95 Precision Low Drift Reference +4.096 V / +5.0 V with Shutdown

- Initial Accuracy: ± 6 mV max
- Low T_{cvo} : 25 ppm/ $^{\circ}$ C max
- Load regulation: 80 ppm/ mA
- Line regulation: 25 ppm/ V
- Wide operating range: ($V_O + 0.3$ V) to +15 V
- Low power: 160 μ A max
 - Shutdown to less than 3 μ A max
- High output current: 5 mA
- Wide temperature range: -40° C to $+125^{\circ}$ C
- Tiny SOT23-5 package

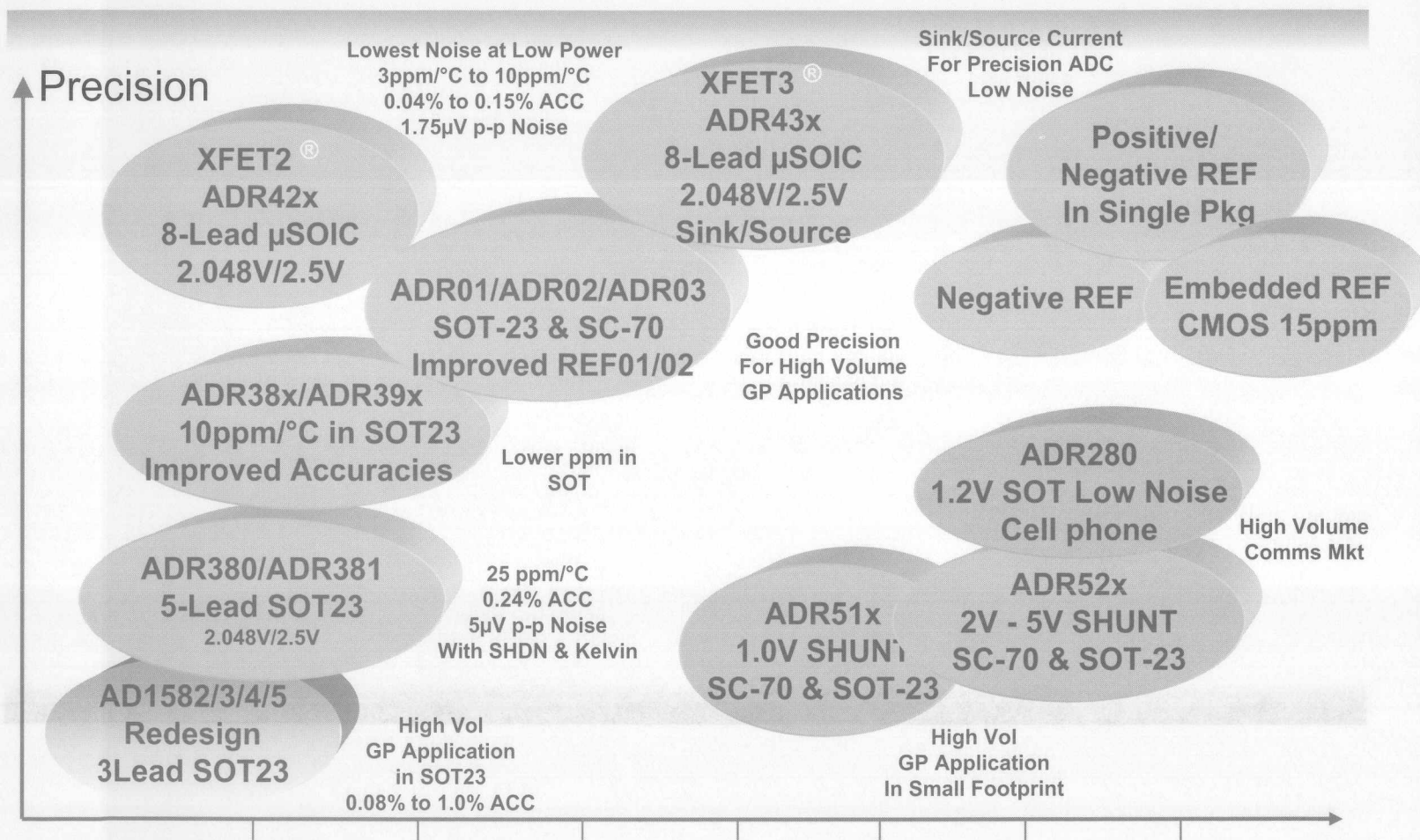
ADR42x Low Noise Precision 2.048 V/ 2.5V/ 3.0V/ 5.0V Reference

- XFET2 Technology
- 2.048 V/ 2.500 V/ 3.0 V/ 5.0 V
- Lowest Noise for “Sub-5V” Operation REF,
 - $e_n = 1.75 \text{ mVp-p}$
- Very Low Drift 3 & 8 ppm/°C max Grades
- 0.04 % and 0.2 % initial accuracy Grades
- Compact μ SOIC-8 Package
- Applications: Precision Converters

ADR510 1.0 V Ultra Precision Low Noise Shunt Voltage Reference

- Wide Operating Range: 100 μ A – 10 mA
- Initial Accuracy: 0.1% max
- Temperature Coefficient: 20 ppm/ $^{\circ}$ C max
- Output Impedance: 0.1 Ω max
- Wide temperature range: -40 $^{\circ}$ C to +85 $^{\circ}$ C
- Ultra Compact 2 x 2 mm SC-70 or SOT-23 Package

Voltage Reference Road Map



SECTION 6

Audio Products

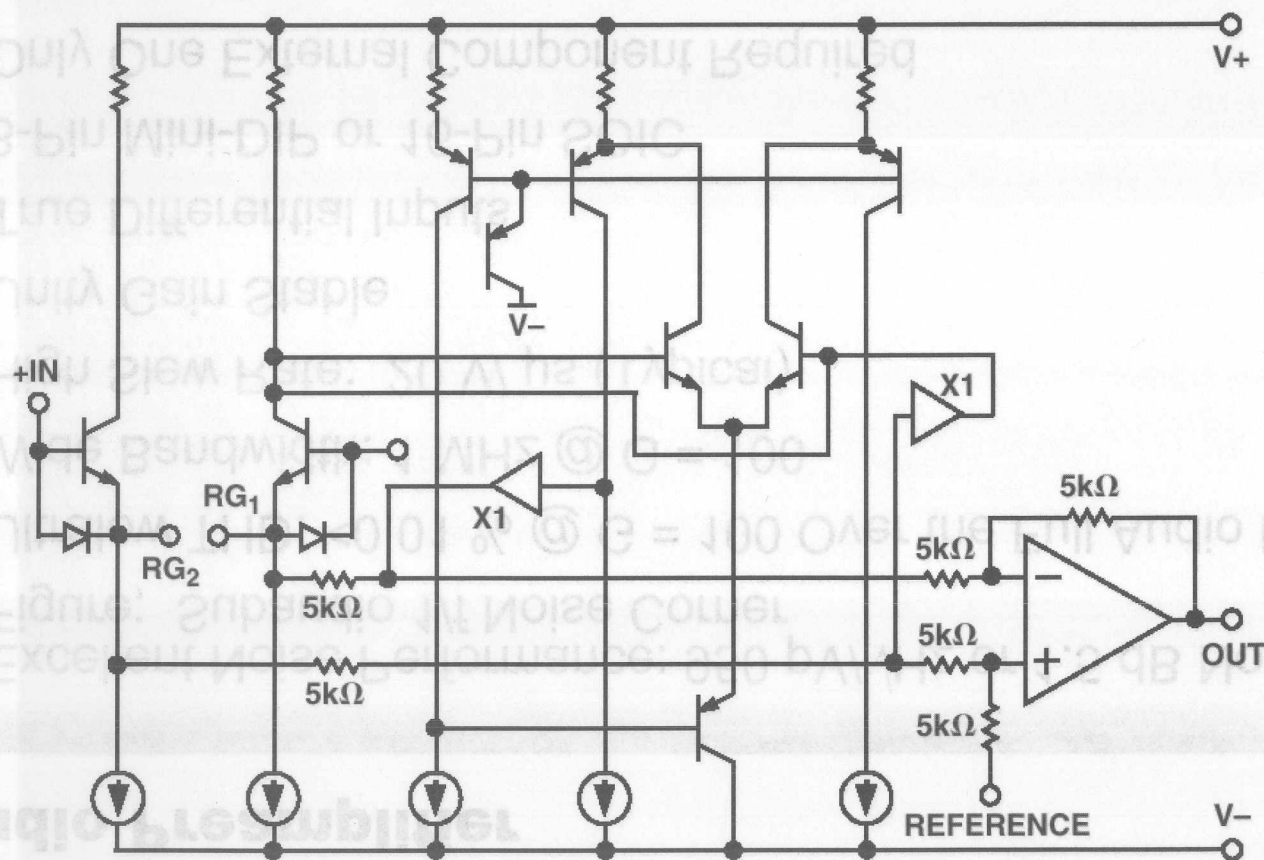
Analog Audio

Digital Audio

Analog Audio

Audio Products
SECTION 6

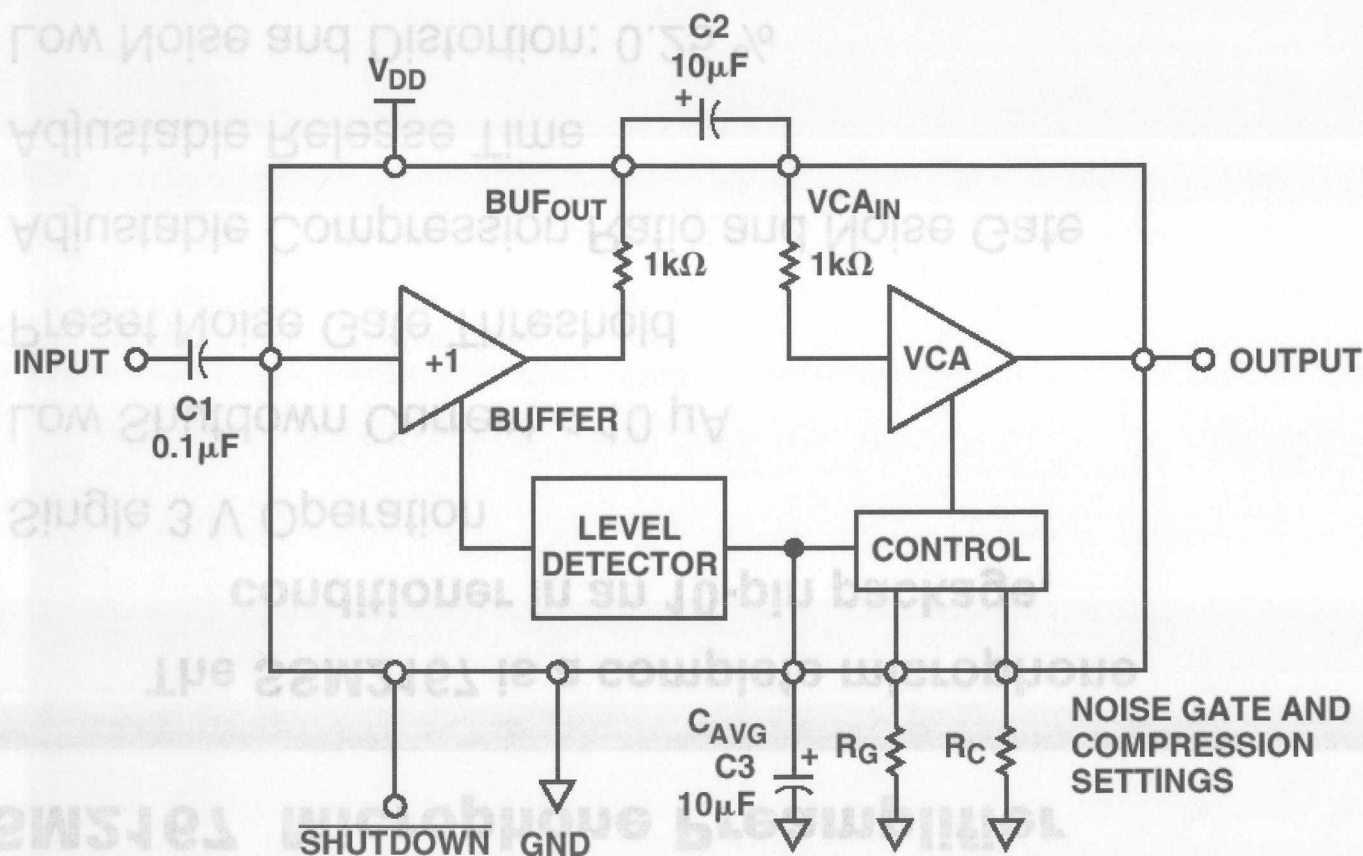
SSM2019 Self-Contained Audio Preamplifier



SSM2019 Self-Contained Audio Preamplifier

- Excellent Noise Performance: 950 pV/ $\sqrt{\text{Hz}}$ or 1.5 dB Noise Figure; Subaudio 1/f Noise Corner
- Ultralow THD: <0.01 % @ G = 100 Over the Full Audio Band
- Wide Bandwidth: 1 MHz @ G = 100
- High Slew Rate: 20 V/ μs (Typical)
- Unity Gain Stable
- True Differential Inputs
- 8-Pin Mini-DIP or 16-Pin SOIC
- Only One External Component Required
- Very Low Cost
- Extended Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Pin-for-Pin Replacement for the SSM2017

SSM2167 Microphone Preamplifier

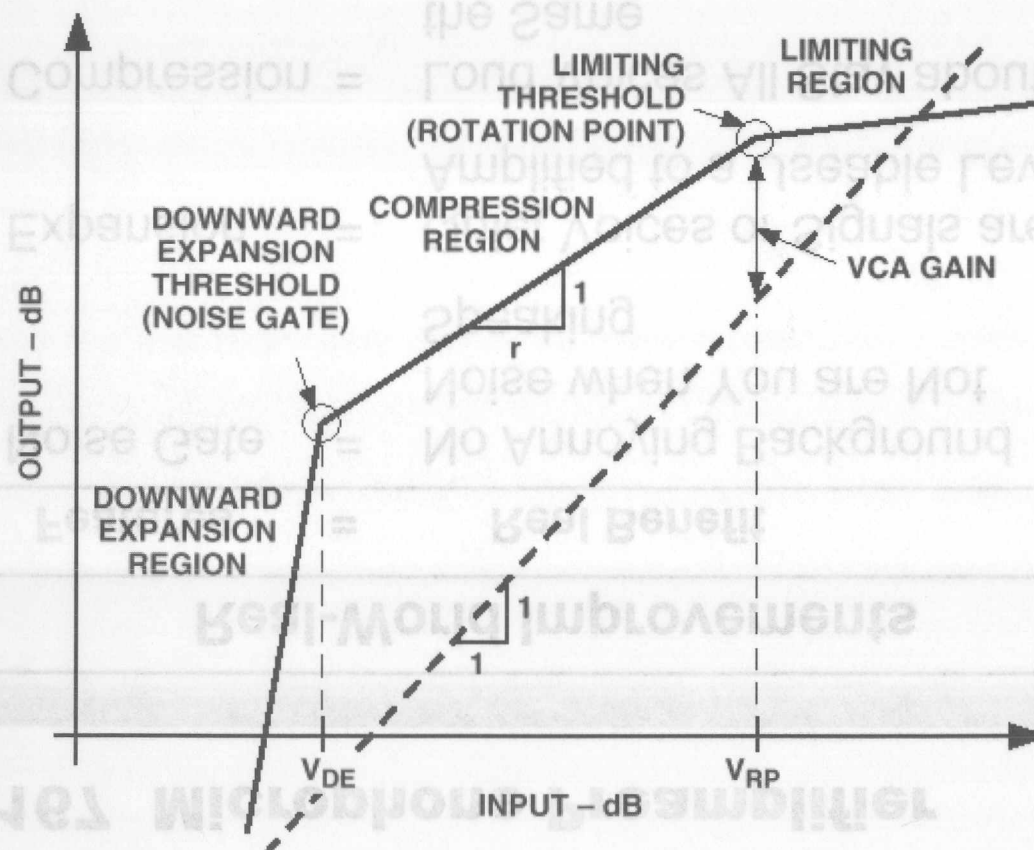


SSM2167 Microphone Preamplifier

The SSM2167 is a complete microphone conditioner in an 10-pin package.

- Single 3 V Operation
- Low Shutdown Current $< 10 \mu\text{A}$
- Preset Noise Gate Threshold
- Adjustable Compression Ratio and Noise Gate
- Adjustable Release Time
- Low Noise and Distortion: 0.25 %
- 20 kHz Bandwidth at $G = 60 \text{ dB}$
- Automatic Limiting Feature Prevents ADC Overload

SSM2167 Microphone Preamplifier Transfer Function

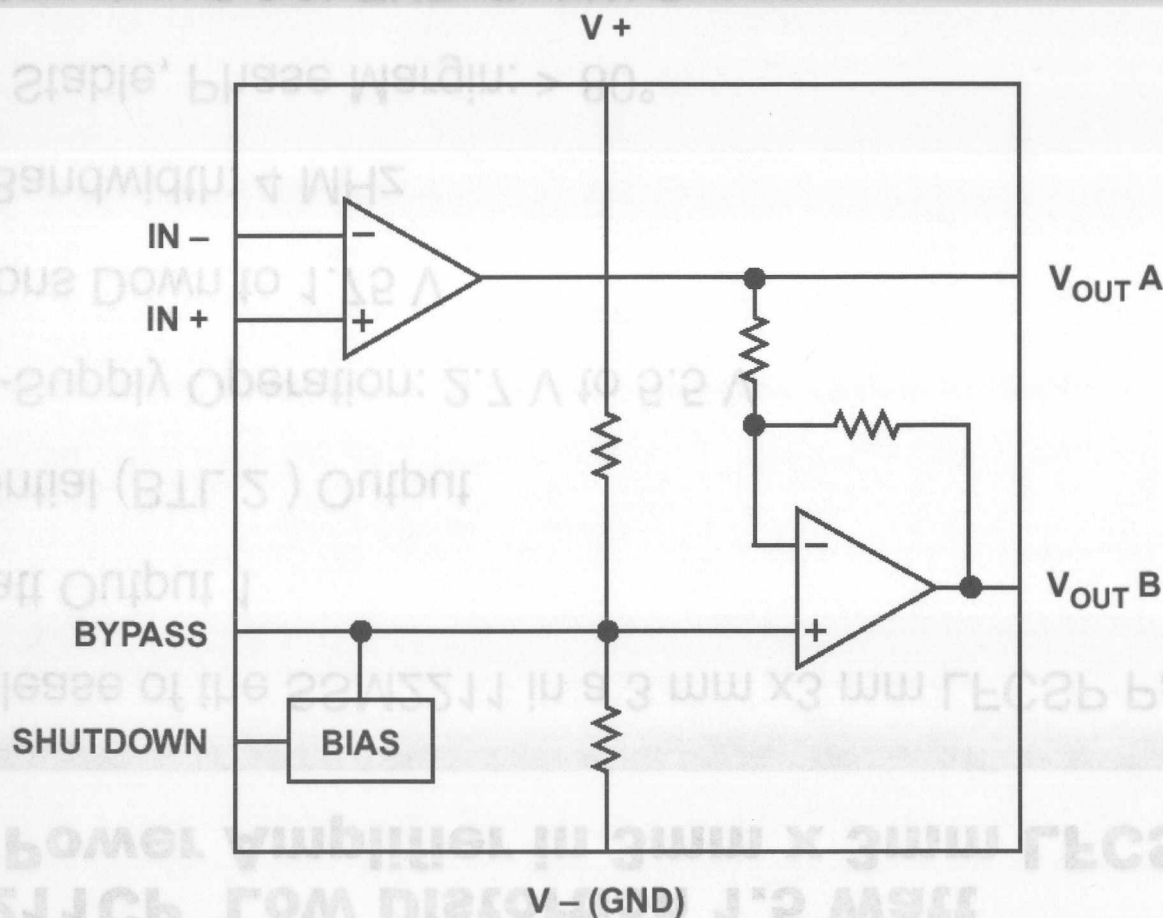


SSM2167 Microphone Preamplifier

Real-World Improvements

Features	=	Real Benefit
Noise Gate	=	No Annoying Background Noise when You are Not Speaking
Expansion	=	Quiet Voices or Signals are Amplified to a Useable Level
Compression	=	Loud Voices All Stay about the Same
Limiting	=	No Matter How Loud the Sound the Part Won't Overload

SSM2211CP Low Distortion 1.5 Watt Audio Power Amplifier in 3mm x 3mm LFCSP



SSM2211CP Low Distortion 1.5 Watt Audio Power Amplifier in 3mm x 3mm LFCSP

- Re-Release of the SSM2211 in a 3 mm x3 mm LFCSP Package
- 1.5 Watt Output 1
- Differential (BTL 2) Output
- Single-Supply Operation: 2.7 V to 5.5 V
- Functions Down to 1.75 V
- Wide Bandwidth: 4 MHz
- Highly Stable, Phase Margin: $> 80^\circ$
- Low Distortion: 0.2 % THD @ 1 W Output
- Excellent Power Supply Rejection

VD181X : VD182X : VD183X : VD184X

Digital Mixing Console

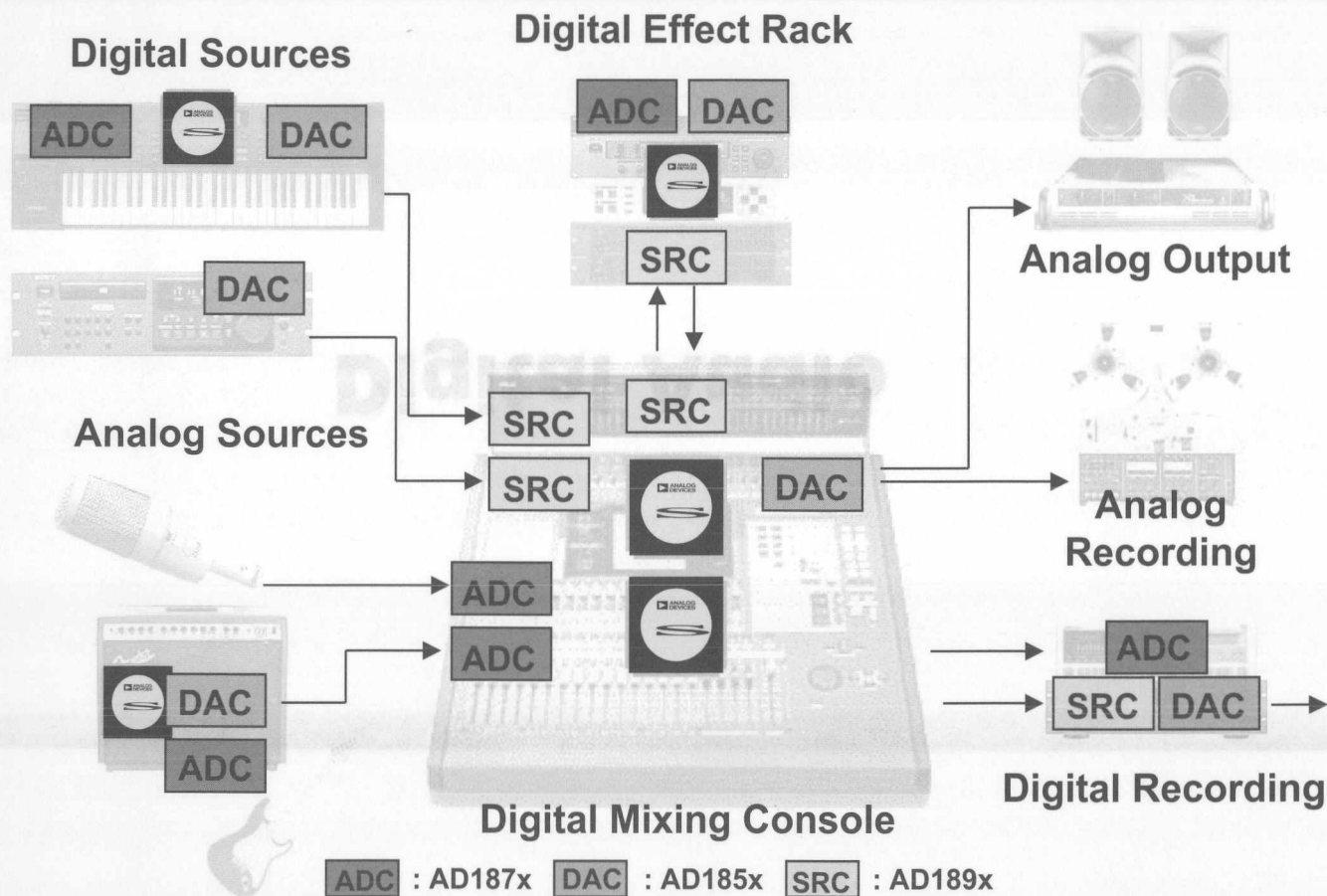
Digital Recording



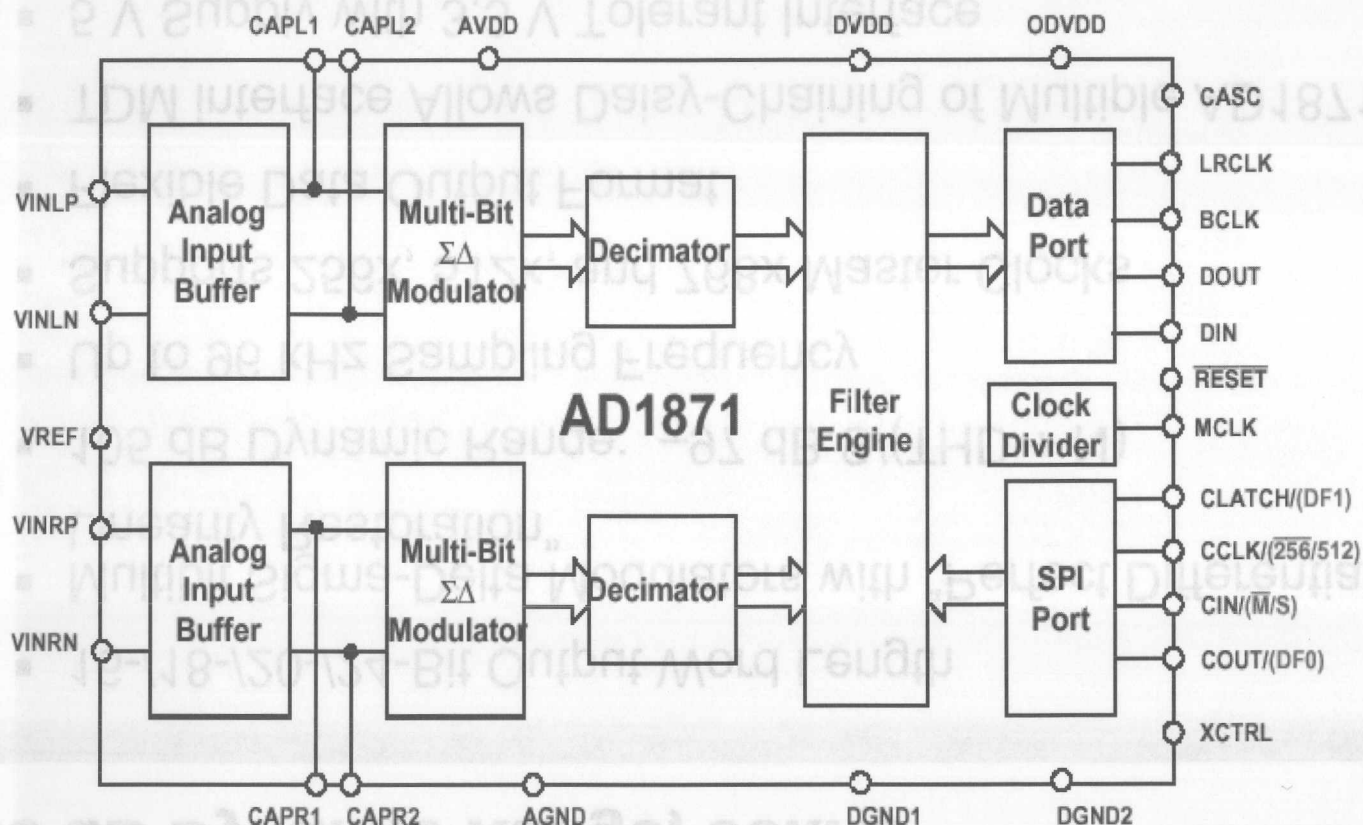
Digital Audio

Digital Recording Studio

Digital Recording Studio



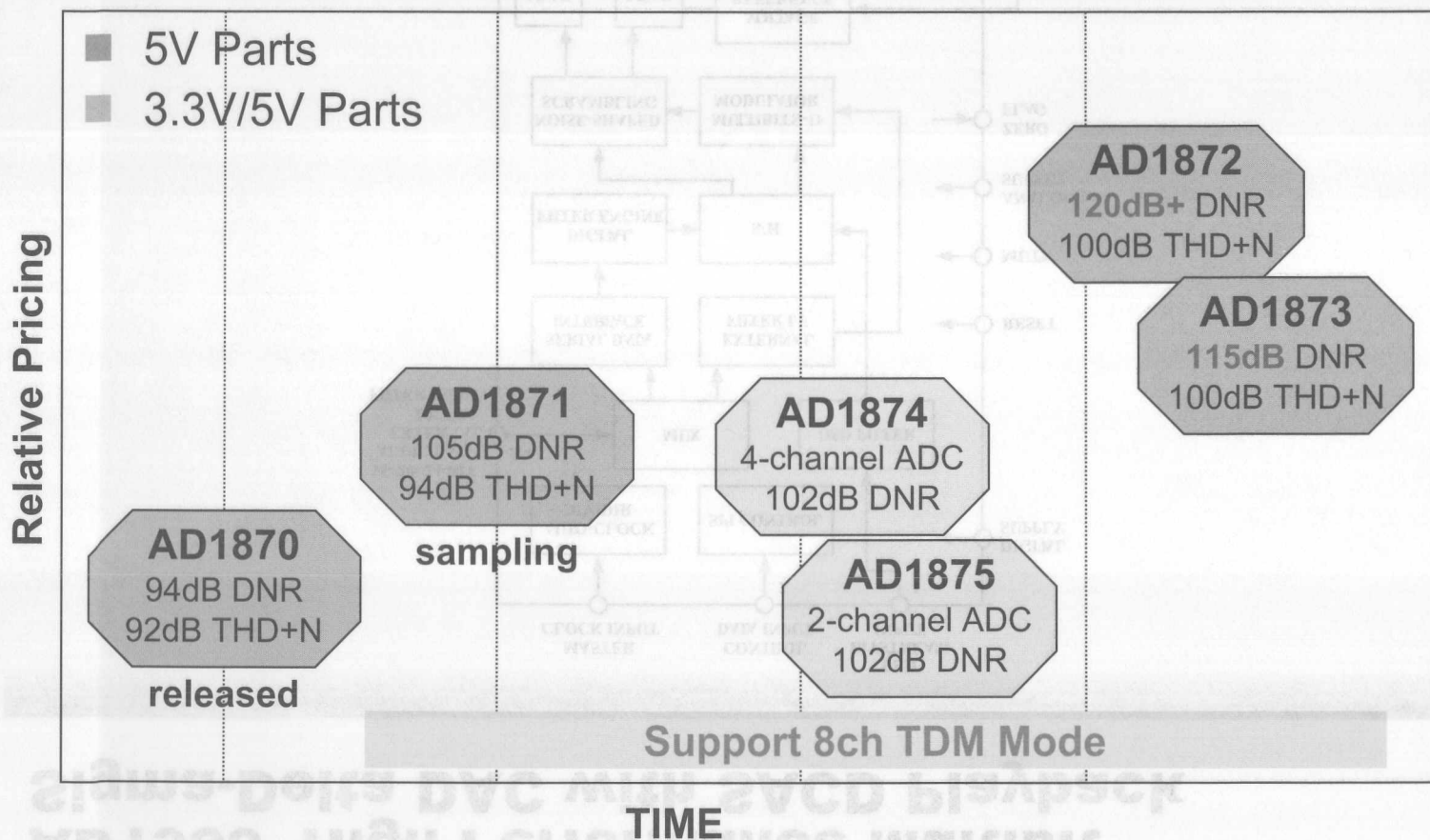
AD1871 Stereo 24-Bit ADC 96 kSPS 105 dB Dynamic Range



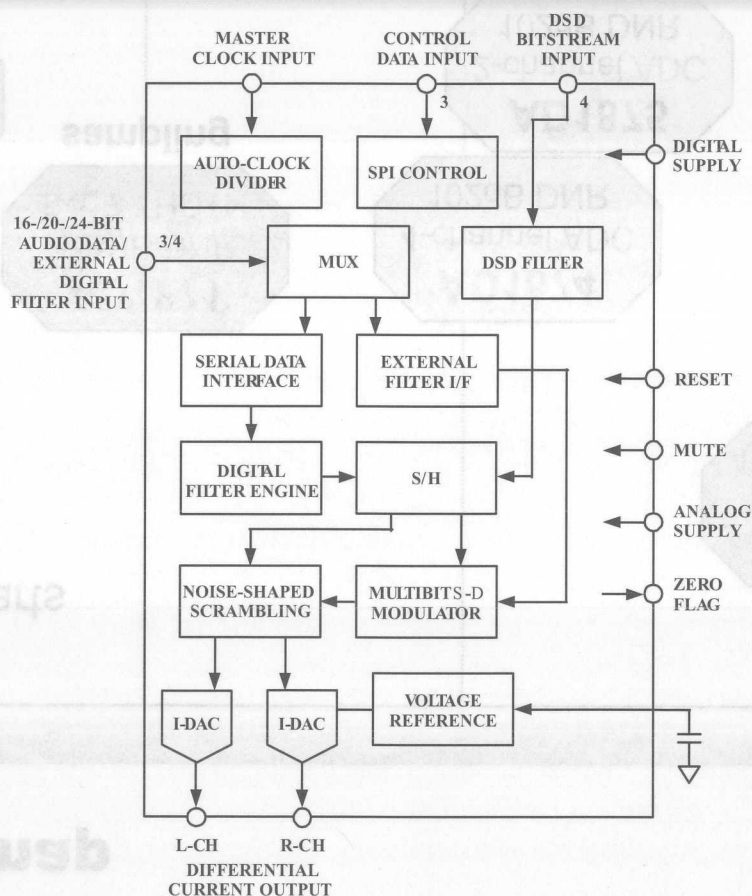
AD1871 Stereo 24-Bit ADC 105 dB Dynamic Range, 96kHz

- 16-/18-/20-/24-Bit Output Word Length
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration”
- 105 dB Dynamic Range: $-97 \text{ dB S}/(\text{THD} + \text{N})$
- Up to 96 kHz Sampling Frequency
- Supports 256x, 512x, and 768x Master Clocks
- Flexible Data Output Format
- TDM interface Allows Daisy-Chaining of Multiple AD1871
- 5 V Supply with 3.3 V Tolerant Interface

ADC Roadmap



AD1955 High Performance Multibit Sigma-Delta DAC with SACD Playback



AD1955 High Performance Multibit Sigma-Delta DAC with SACD Playback

- 5 V Power Supply Stereo Audio DAC System
- Accepts 16/ 18-/20-/24-Bit Data
- Supports 24-Bits, 192 kHz Sample Rate PCM Audio Data
- Supports SACD Bit-Stream and External Digital Filter Interface
- Accepts a Wide Range of PCM Sample Rates Including:
 - 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
- Multibit Sigma Delta Modulator with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DAC — Least Sensitive to Jitter
- Supports SACD Playback with “Bit Expansion” Filter
- Differential Current Output for Optimum Performance

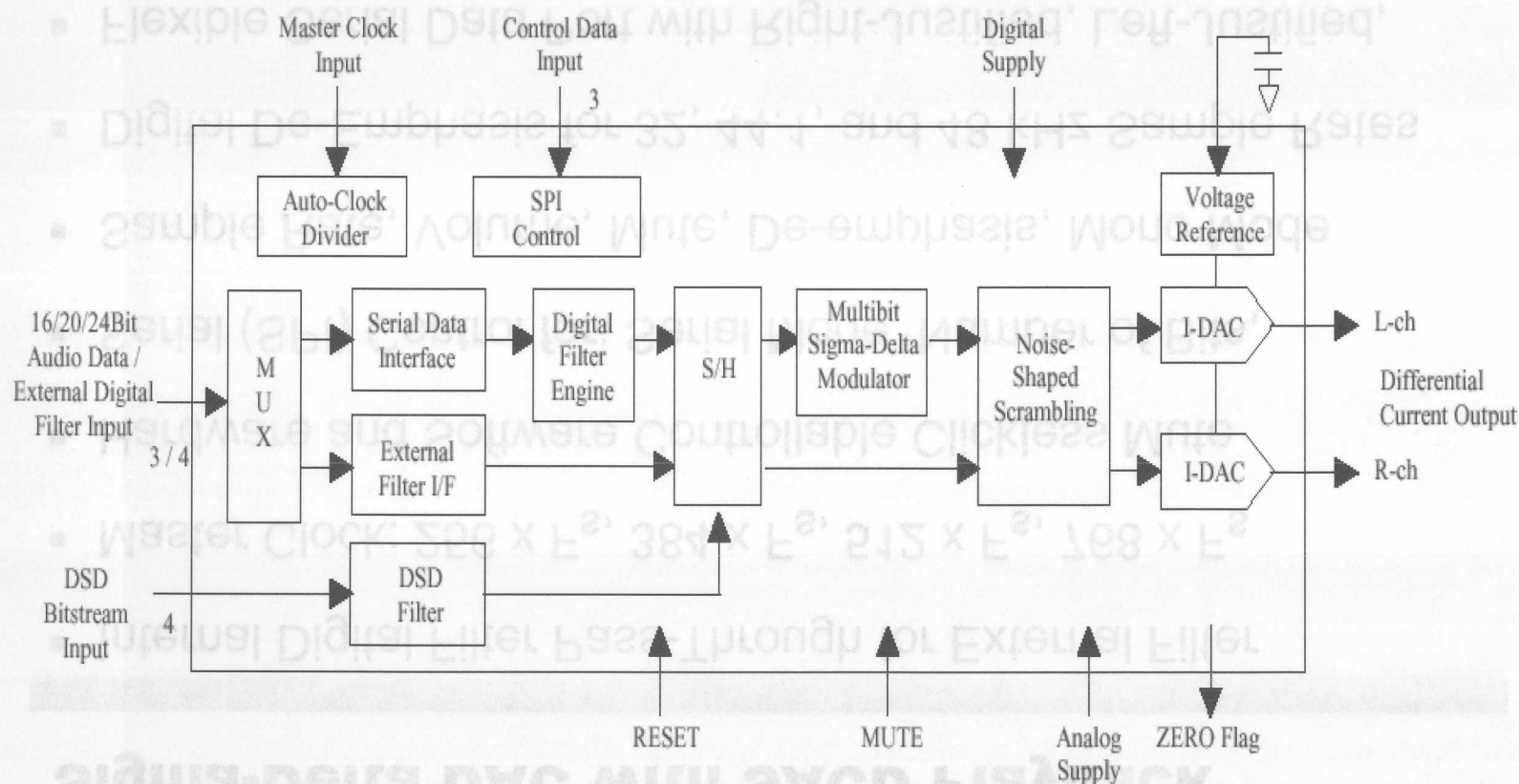
AD1955 High Performance Multibit Sigma-Delta DAC with SACD Playback

- 8.64 mA p-p Output Current with +3 dB Headroom in SACD Mode
- 120 dB SNR/DNR (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
- 123 dB SNR/DNR (Mono)
- -110 dB THD + N
- 110 dB Stopband Attenuation with ± 0.0002 dB Passband Ripple
- 8x Oversampling Digital Filter
- On-Chip Clickless Volume Control
- Supports SACD-Mute Pattern Detection
- Supports $64 f_s/128 f_s$ DSD SACD with Phase Modulation

AD1955 High Performance Multibit Sigma-Delta DAC with SACD Playback

- Internal Digital Filter Pass-Through for External Filter
- Master Clock: $256 \times F_s$, $384 \times F_s$, $512 \times F_s$, $768 \times F_s$
- Hardware and Software Controllable Clickless Mute
- Serial (SPI) Control for: Serial Mode, Number of Bits, Sample Rate, Volume, Mute, De-emphasis, Mono Mode
- Digital De-Emphasis for 32, 44.1, and 48 kHz Sample Rates
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible, and DSP Serial Port
- 28-Lead SSOP Plastic Package

AD1957 High Performance Multibit SD DAC with SACD Playback



AD1957 High Performance Multibit $\Sigma\Delta$ DAC with SACD Playback

- 5V Power Supply Stereo Audio DAC System.
- Supports 24-Bits, 192 kHz Sample Rate PCM Audio Data
- Supports SACD bit-stream and External Digital Filter Interface
- PCM Sample Rates Including: 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
- Multibit Sigma Delta Modulator with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DAC - Least Sensitive to Jitter

AD1957 High Performance Multibit $\Sigma\Delta$ DAC with SACD Playback

- Supports SACD-Mute pattern detection
- Supports 64 fs/128 fs DSD SACD with phase modulation
- SACD – PCM output level matching
- Selectable SACD digital filter cutoff frequency
- Bypass-able SACD digital volume control
- Master clock: 256 fs, 384 fs, 512 fs, 768 fs
- Hardware and Software Controllable Clickless Mute
- Serial (SPI) Control for: Serial Mode, Wordwidths (16/20/22/24), Sample Rate, Volume, Mute, De-emphasis, Mono Mode
- Digital De-emphasis for 32, 44.1, 48 KHz Sample Rates
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port

AD1957 High Performance Multibit $\Sigma\Delta$ DAC with SACD Playback

- Differential Current Output for Optimum Performance
- 8.64 mA p-p Output Current with +3 dB headroom in SACD mode
- 123 dB SNR/DNR (not muted) at 48 KHz Sample Rate (A-Weighted Stereo)
- 123 dB SNR/DNR (Mono)
- -110 dB THD+N
- 110 dB Stopband Attenuation with +/-0.0002dB Passband Ripple
- 8x Oversampling PCM Digital Filter
- On-chip Clickless Volume Control
- 28 Lead SSOP Plastic Package

AD1850 24-bit 192kHz Stereo Low-Power $\Sigma\Delta$ DAC

On-chip Clockless Volume Control

8x Oversampling PCM Digital Filter

110 dB Stopband Attenuation

-110 dB THD+N

153 dB SNR (Worst)

Measuring Stereo

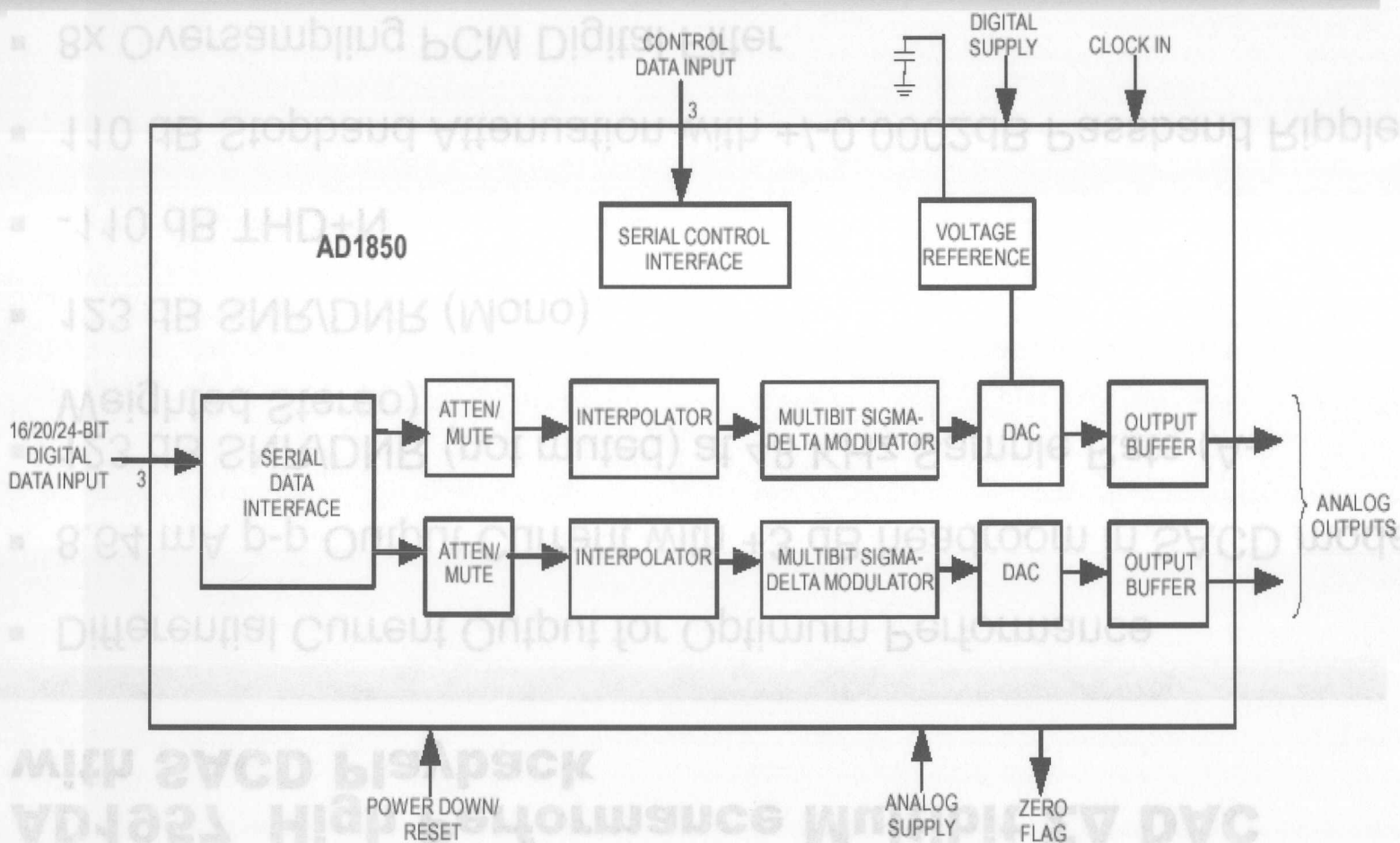
3.5% 24-bit Dither (no dither)

89 dB 0.5% Dither

Differential Current Output for Optimum Performance

with 2VCD Bias Pack

AD1850 High Performance Multibit $\Sigma\Delta$ DAC



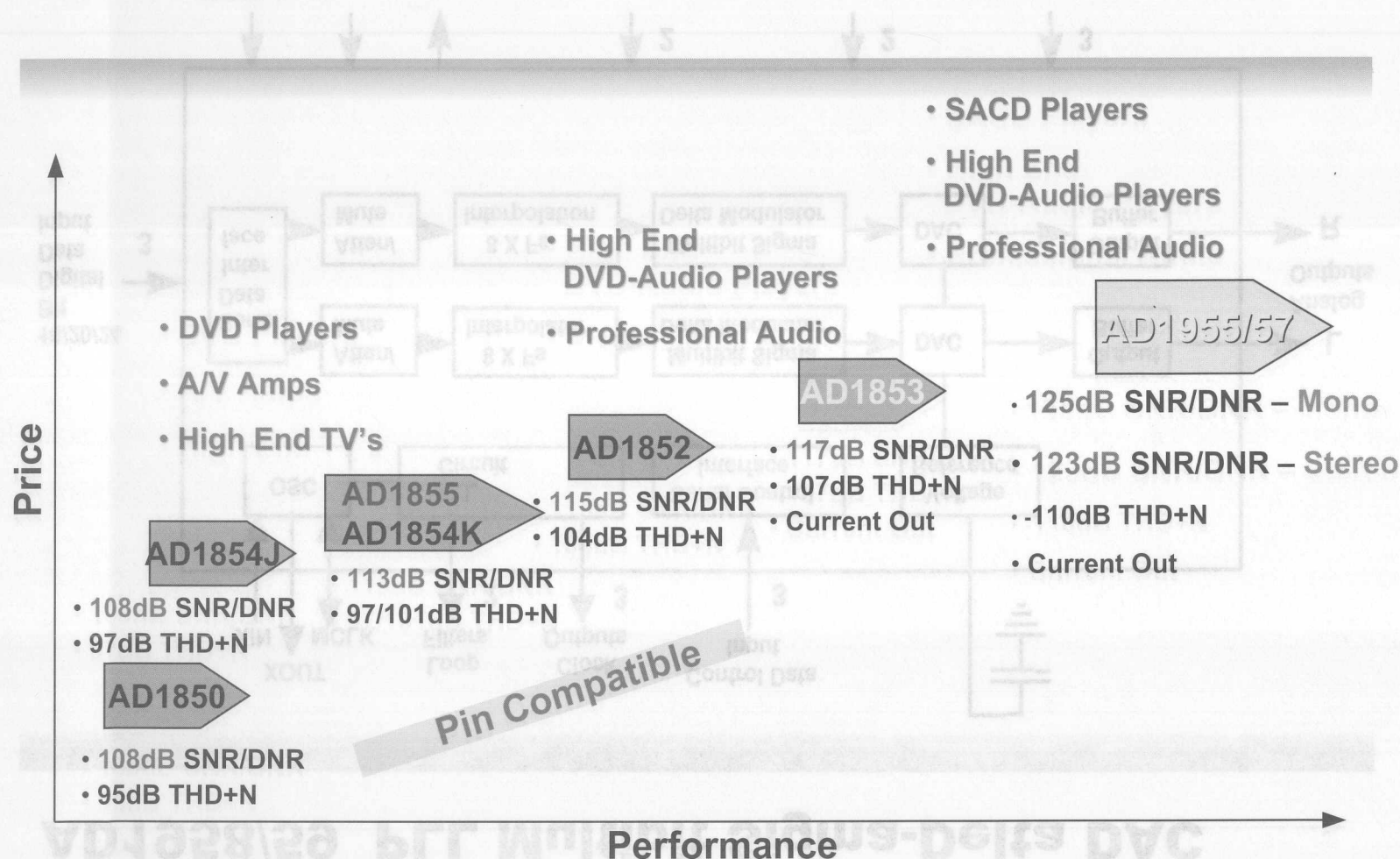
AD1850 24-bit 192kHz Stereo Low-Power $\Sigma\Delta$ DAC

- 3.3V Single Power Supply Stereo Audio DAC System
- Accepts 16-/20-/24-Bit data
- Supports Sample Rates to 192 kHz
- 106dB SNR & DNR at 48kHz Sample Rate (A-weighted stereo, not muted)
- -94 dB THD+N
- Linear Interpolator
- 70 dB Stopband Attenuation, ± 0.01 dB Passband Ripple
- Single-Ended Output for Ease of Use
- Full-Scale Output: 2.8 Vp-p

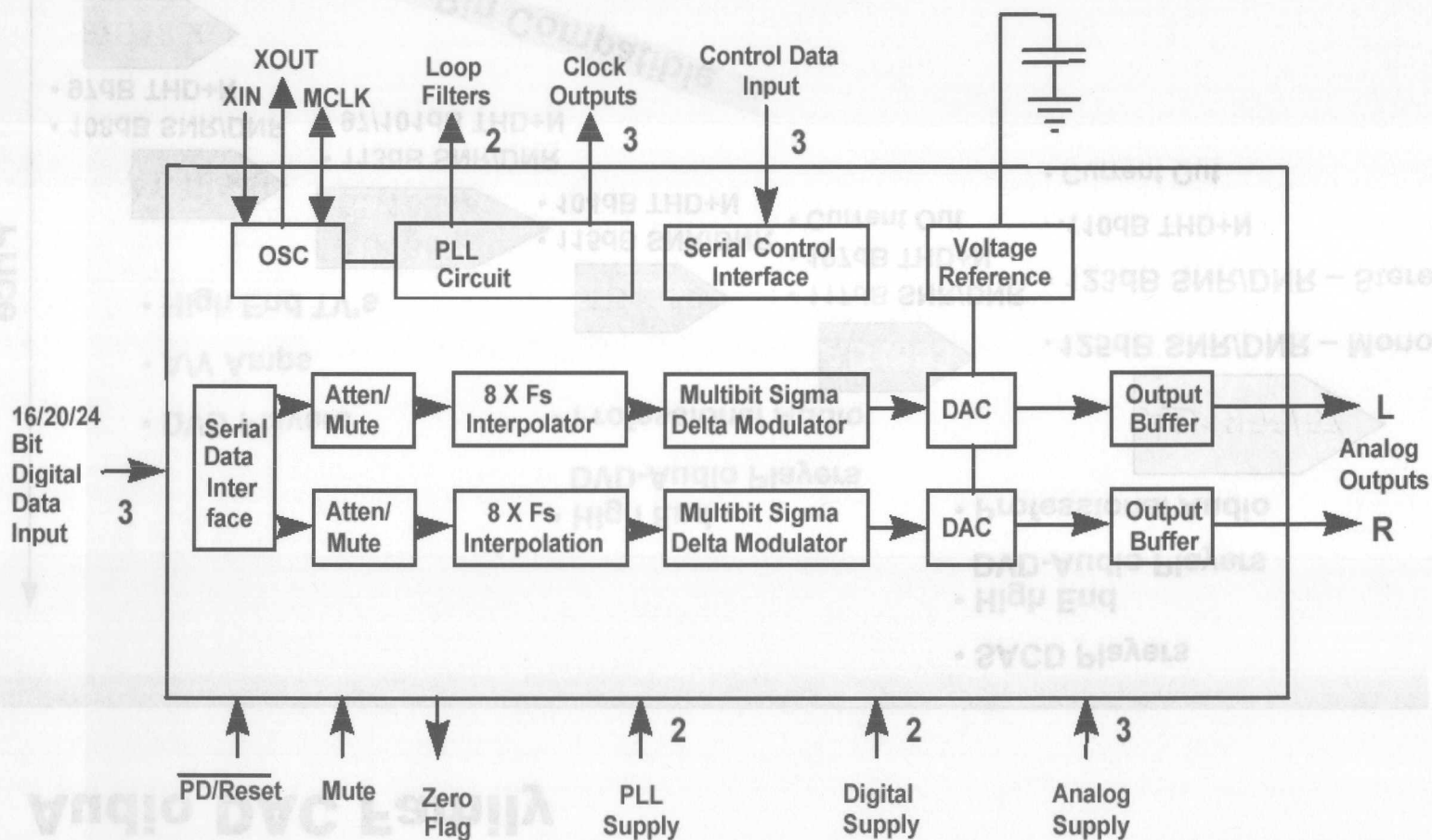
AD1850 24-bit 192kHz Stereo Low-Power $\Sigma\Delta$ DAC

- All Modes & Features are SPI-Controllable
- Flexible Serial Data Port with Left-Justified, Right-Justified, I²S-Compatible Serial Port Modes
- Supports 256/ 384/ 512/ 768 x Fs Master Clocks
- Zero-Input Flag Hardware Output
- Digital De-Emphasis Processing
- On-Chip Volume Control – 96dB range with 0.375dB/step
- Clickless Mute Control
- 16-pin SSOP package

Audio DAC Family



AD1958/59 PLL Multibit Sigma-Delta DAC



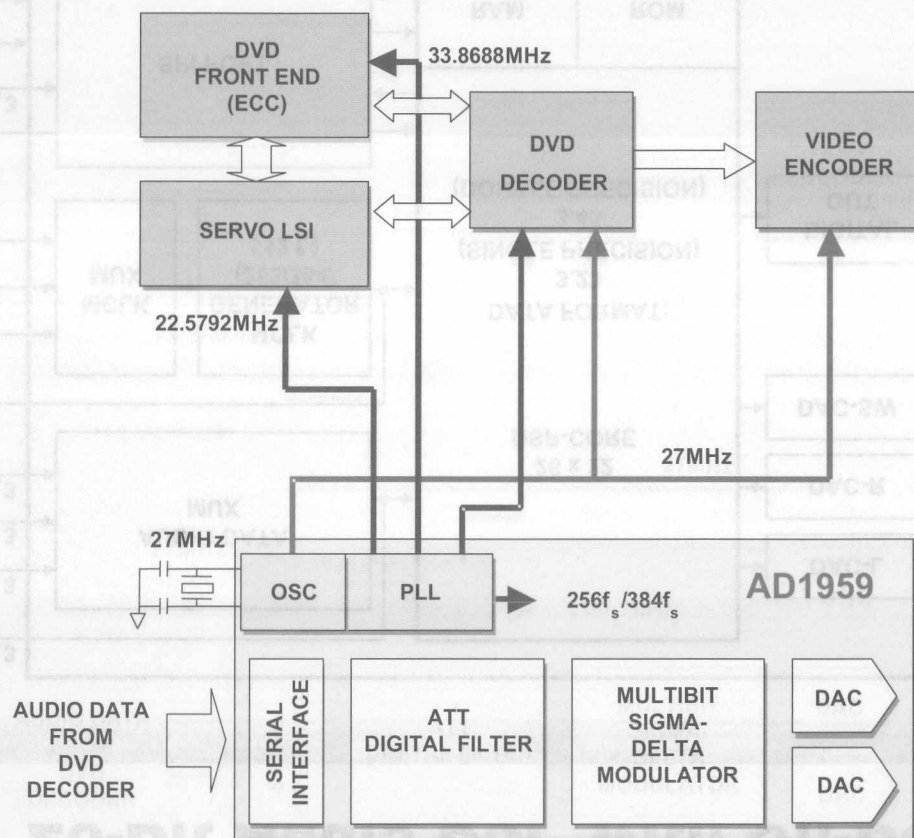
AD1958/59 PLL Multibit Sigma-Delta DAC

- Accepts 16-/18-/20-/24-Bit Data
- Supports up to 24-Bit 192 kSPS Sample Rate
- Multibit Sigma-Delta Modulator with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling for Reduced Jitter Sensitivity
- 108 dB (A-Weighted) SNR at 48 kSPS (Not Muted)
- 75 dB Stopband Attenuation
- Flexible Serial Data Port (Left Justified, Right Justified, I²S, and DSP Modes)
- Programmable Fractional-N PLL (<100 pS RMS Clock Jitter)
- Single +5 V Supply

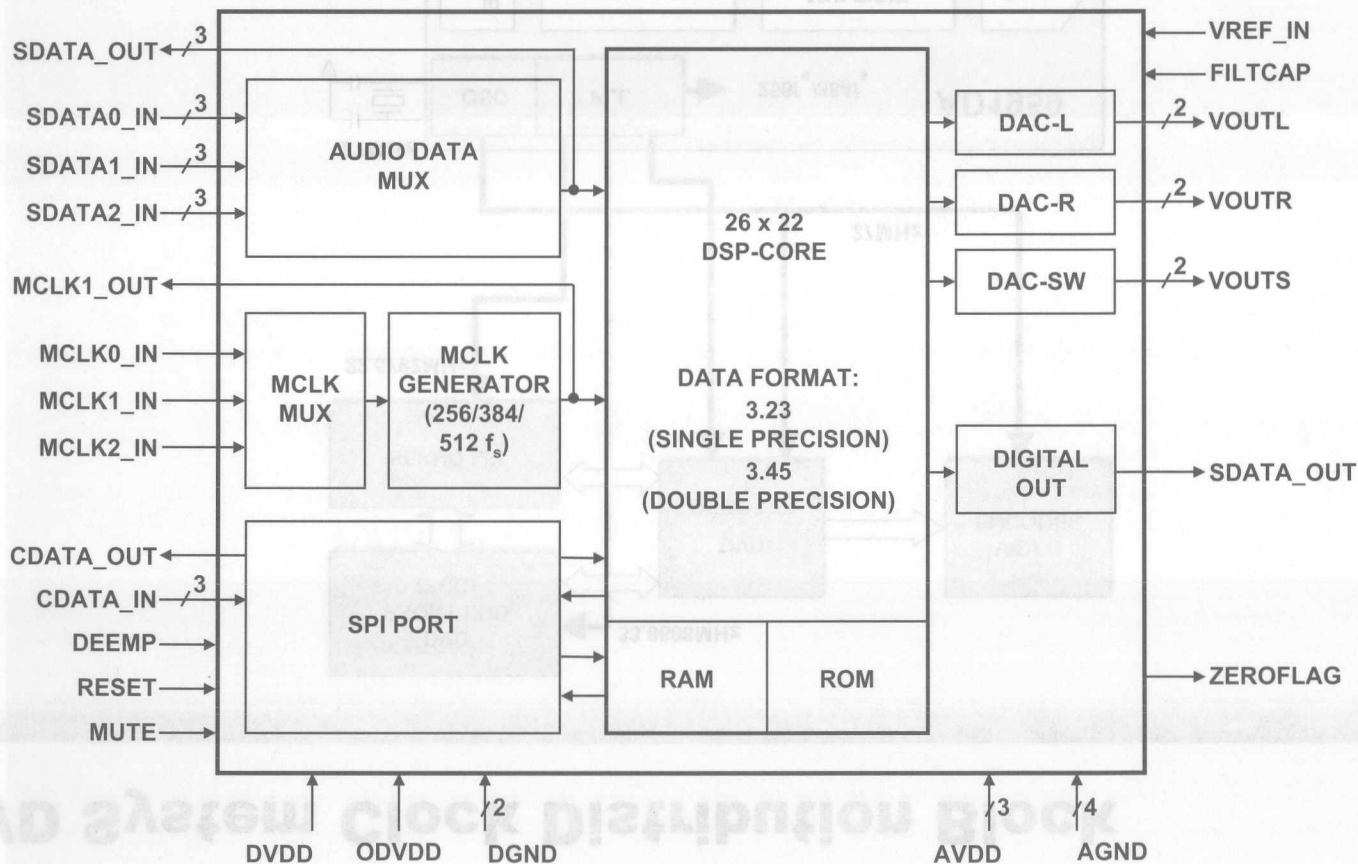
Why PLL DAC?

- DVD/MPEG2 System is Running at 27 MHz System Clock. This Clock is also Used for Video Master Clock
- Audio Master Clock Needs to Synchronize with Video Master Clock
- Audio Clock Frequency is Multiple of Sampling Frequency (f_s) Such As $256 f_s$ / $384 f_s$ (16.9344 MHz, etc.), But this Frequency Cannot Be Generated By Simple Divider from 27 MHz Master Clock
- PLL Generate Audio Master Clock Synchronized with 27 MHz System Clock with Very Low Jitter Performance for High Sound Quality
- Integration of DAC and PLL Is the BEST Solution for System Performance and Price Point of View

DVD System Clock Distribution Block



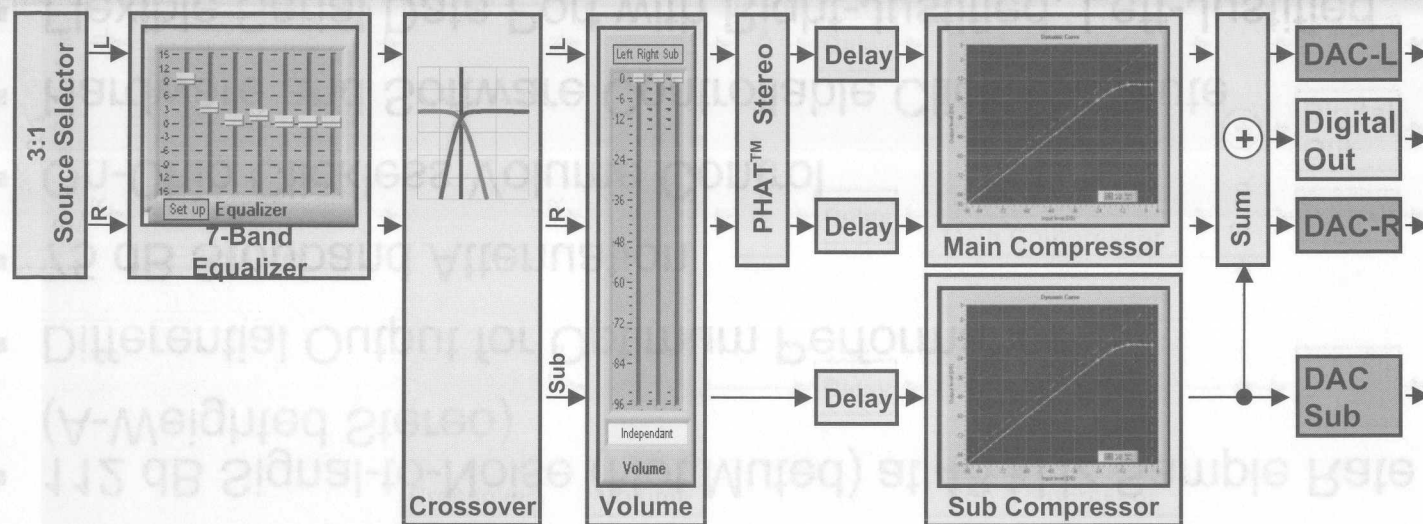
AD1954 26-Bit Audio DSP with On-Board DACs



AD1954 26-Bit Audio DSP with On-Board DACs

- On Board 3-Channel DAC
 - 2-channel left/right
 - 1-channel subwoofer
- 112 dB Signal-to-Noise (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
- Differential Output for Optimum Performance
- 75 dB Stopband Attenuation
- On-Chip Clickless Volume Control
- Hardware and Software Controllable Clickless Mute
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S Compatible, and DSP Serial Port Modes
- 44-Pin MQFP or 48-Pin TQFP Plastic Package

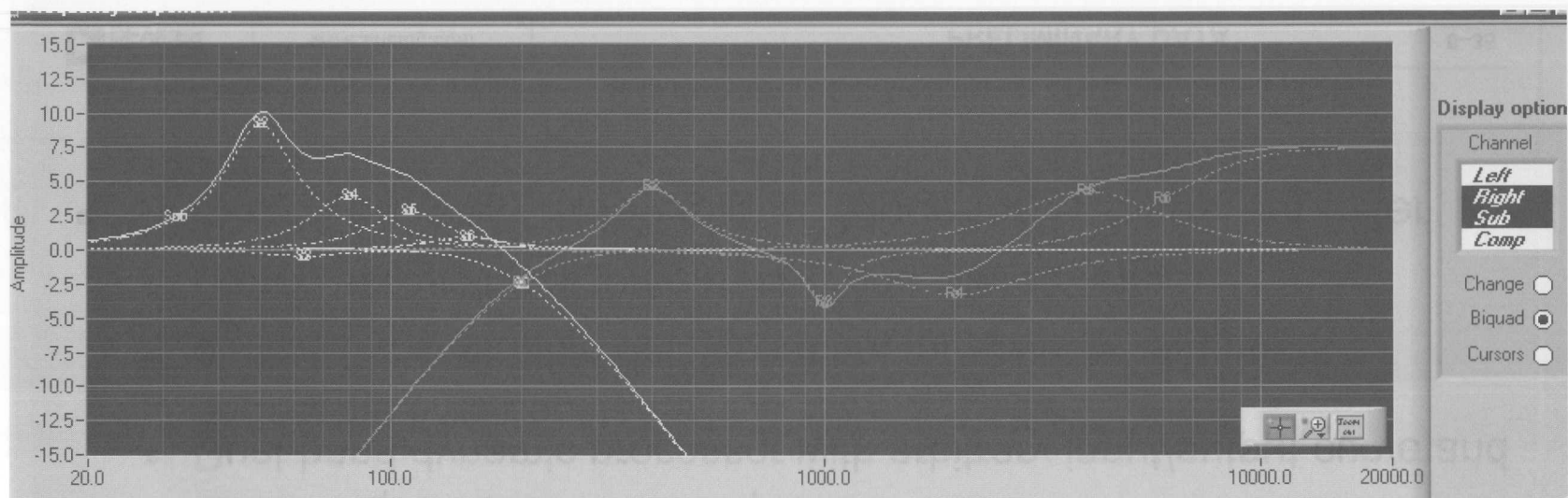
AD1954 26-Bit Audio DSP with On-Board DACs



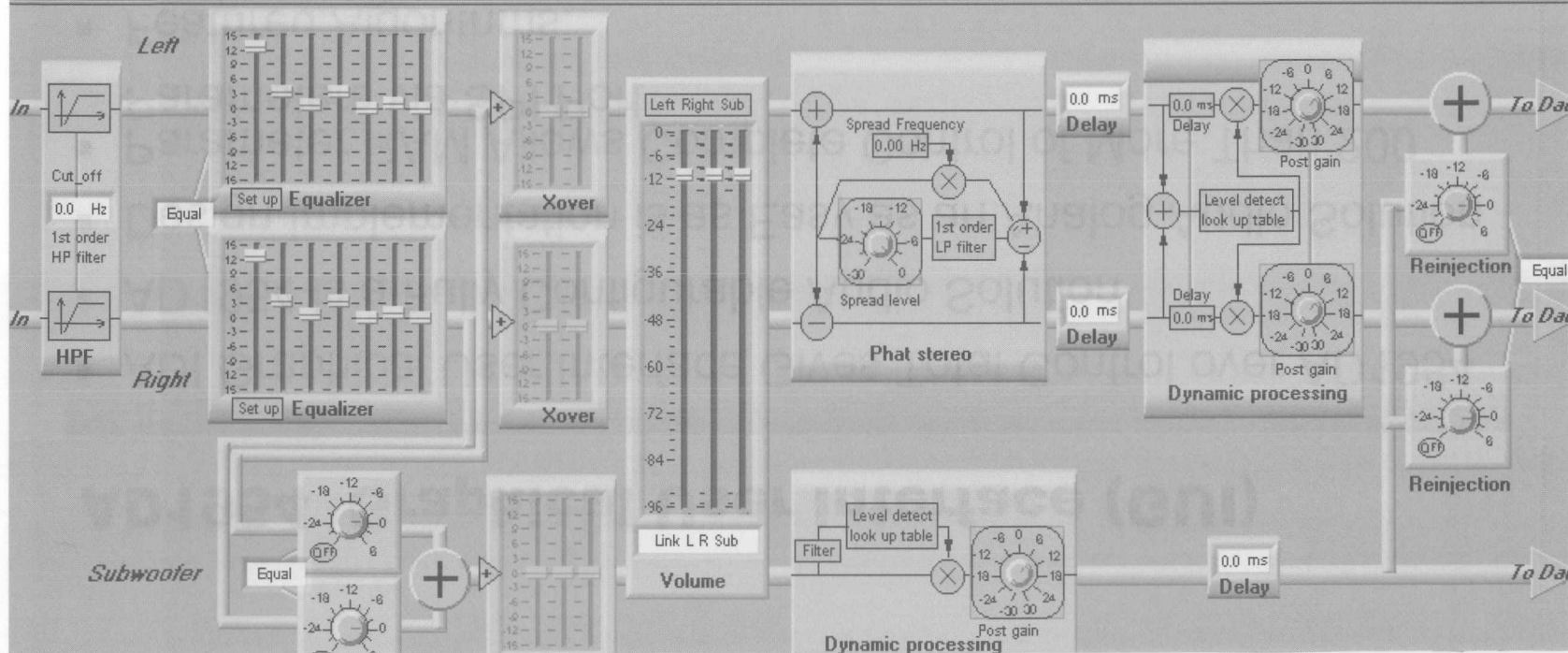
- Configuration is Optimized for 2.0 and 2.1 Systems
- Applications are:
 - Home stereo minisystems
 - PC multimedia speakers
 - Car audio systems
 - DTV

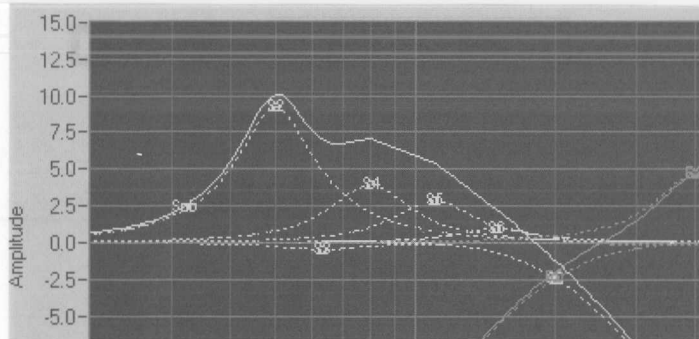
AD1954 Graphical User Interface (GUI)

- ADI Graphical User Interface Gives Total Control over AD1954
- AD1954 is a Fully Configurable Audio Solution
- Design Implementation is as Easy as an Analog Audio Solution
- Parameter RAM Allows Complete Control of More Than 200 Parameters via SPI Port
- Featured Algorithms:
 - Seven biquad filter sections per channel
 - Dual-band dynamic processor with arbitrary input/output curve and adjustable time constants
 - 0 ms – 6 ms variable delay/channel for speaker alignment
 - Stereo spreading algorithm for “Wide Stereo” effect
- SPI Port Features “Safe-Upload” Mode for Transparent Filter Updates



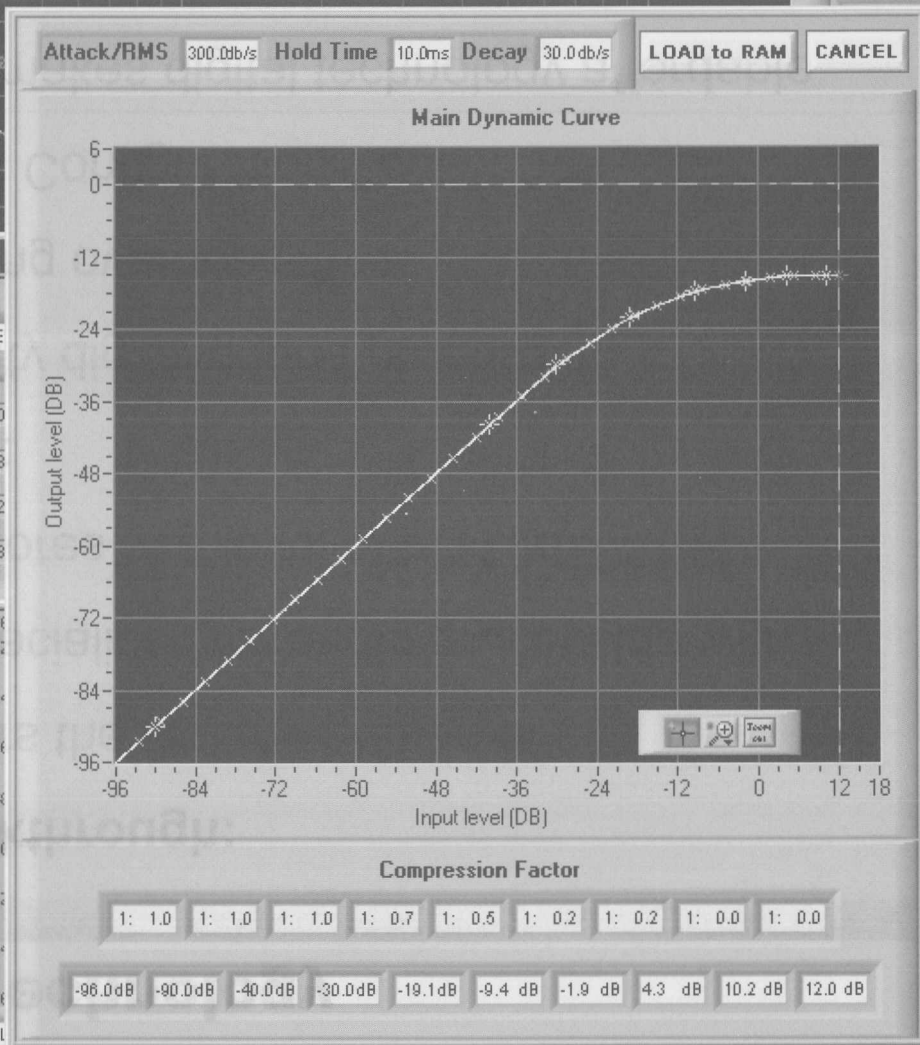
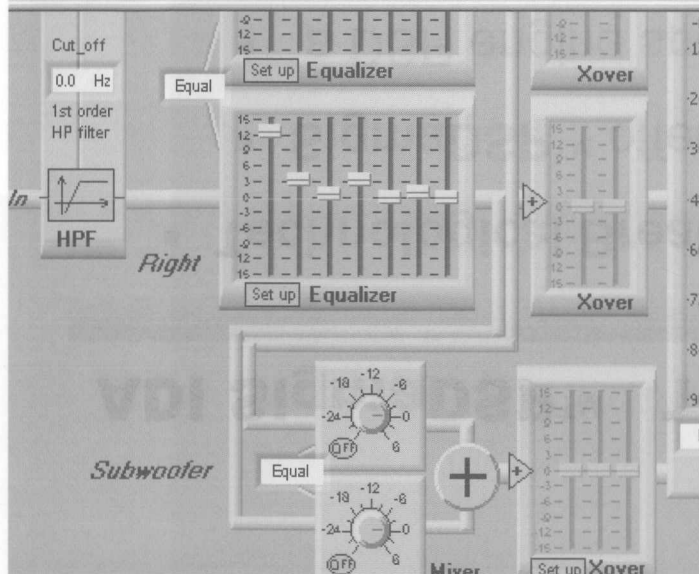
Set up audio parameters





Filter Set up

	Biquad Cell 1	Biquad Cell 2	Biquad Cell 3	Biquad Cell 4
Sub	Bessel	Peaking EQ	Peaking EQ	Peaking EQ
LINKS	Low pass filter			
Load mode	Gain ▲ 0.0 dB	Gain ▲ 0.0 dB	Gain ▲ 0.0 dB	Gain ▲ 0.0 dB
to Buffer	Cut off Frequency	Freq ▲ 50 Hz	Freq ▲ 63 Hz	Freq ▲ 80 Hz
	High ▲ 200 Hz	Q ▲ 2.00	Q ▲ 2.00	Q ▲ 2.00
Load RAM	24db/oct	Boost ▲ 9.2 dB	Boost ▲ 0.0 dB	Boost ▲ 0.0 dB



Volume **Dynamic processing** **Post gain** **Delay**

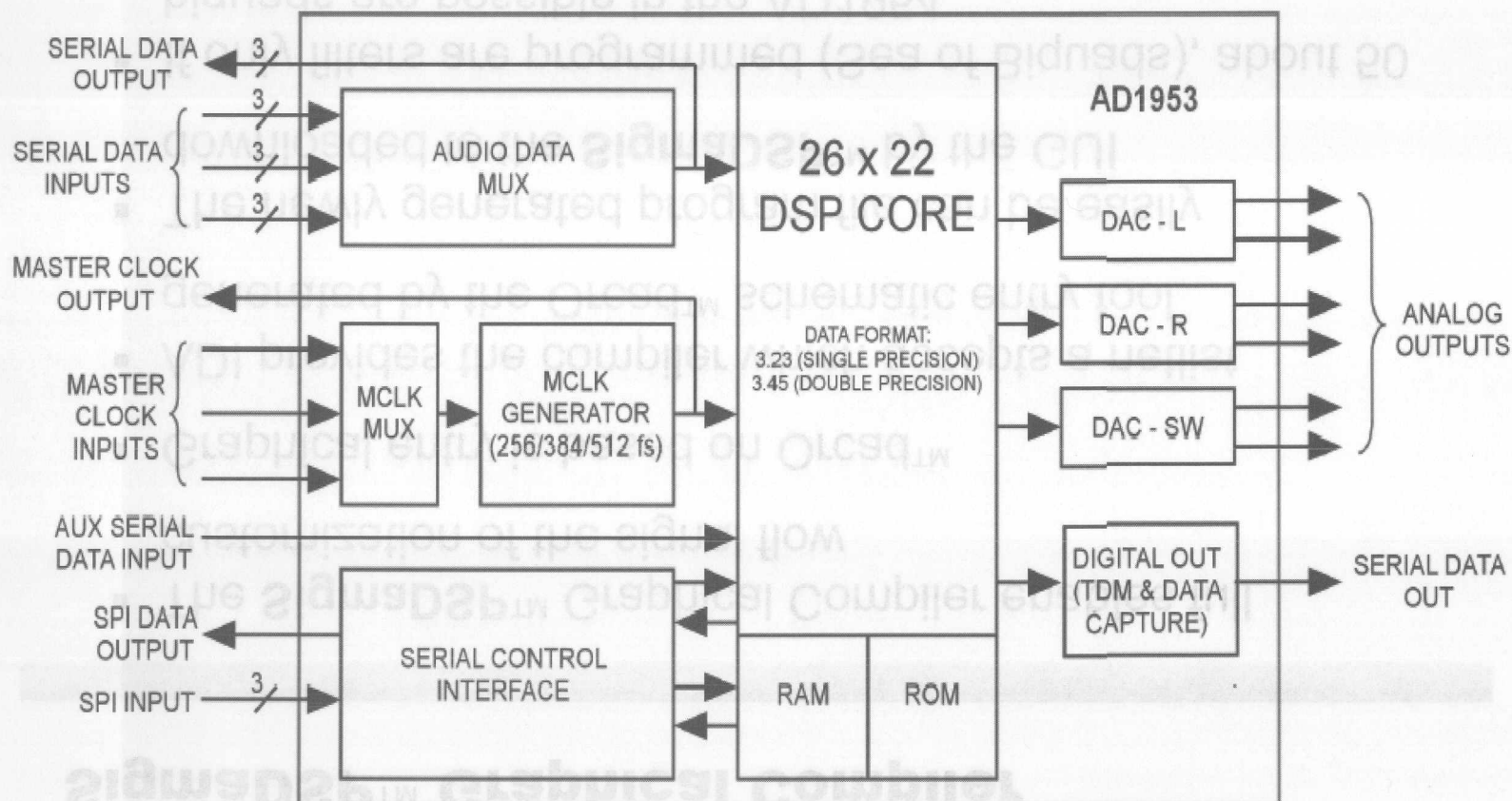
ADI SigmaDSP™ Technology

- **Technological Breakthrough:**
 - **SigmaDSP™** offers the first integration of
 - a DSP engine specialized for audio processing with
 - audio converter cores at a level of **> 110dB SNR.**
- **SigmaDSP Features:**
 - Professional-quality digital sound processing
 - ZERO programming overhead
 - Intuitive Graphical Configuration Tool
 - A price point that makes digital technology affordable

SigmaDSP™ Graphical Compiler

- The **SigmaDSP™** Graphical Compiler enables full customization of the signal flow
- Graphical entry is based on Orcad™
- ADI provides the compiler which accepts a netlist generated by the Orcad™ schematic entry tool
- The newly generated program file can be easily downloaded to the **SigmaDSP™** by the GUI
- If only filters are programmed (Sea of Biquads), about 50 biquads are possible in the AD1954
- The next generation of **SigmaDSP™** will double the MIPS

AD1953 Three channel, 24-Bit Signal Processing DAC



AD1953 Three channel, 24-Bit Signal Processing DAC

- 5 V 3-channel Audio DAC System
- 7 Biquad Filter sections per channel
- Dual Dynamic Processor with arbitrary input/output curve and adjustable time constants
- “PHAT™ Stereo” Spreading Algorithm for wide stereo effect
- 0 – 6 ms variable delay/channel for speaker alignment
- Differential Output for Optimum Performance
- 112 dB Signal-to-Noise (not muted) at 48 kHz Sample Rate (A-Weighted Stereo)
- 75 dB Stopband Attenuation

AD1953 Three channel, 24-Bit Signal Processing DAC

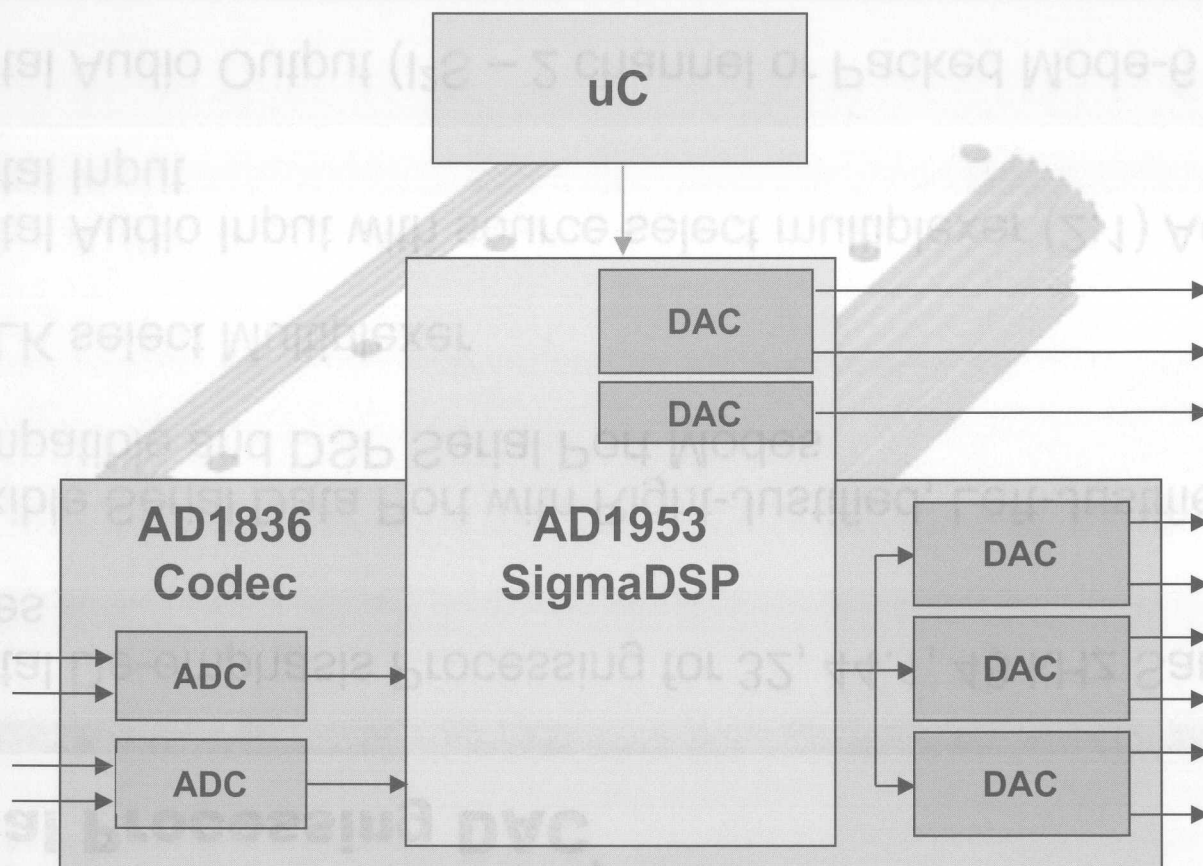
- Program RAM allows complete new program download via SPI port
 - SPI port features “Safe-Upload” mode for transparent filter updates
- 256-word Parameter RAM
- 512-word Program Memory
- 512 instructions per audio sample
- Two control registers allow complete control of modes and memory transfers
- On-chip Clickless Volume Control (8 total)
- Hardware and Software Controllable Clickless Mute

AD1953 Three channel, 24-Bit Signal Processing DAC

- Digital De-emphasis Processing for 32, 44.1, 48 kHz Sample Rates
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- MCLK select Multiplexer
- Digital Audio Input with source select multiplexer (2:1) Auxiliary Digital Input
- Digital Audio Output (I²S – 2 channel or Packed Mode-6 channel)
- 48-Lead LQFP Plastic Package

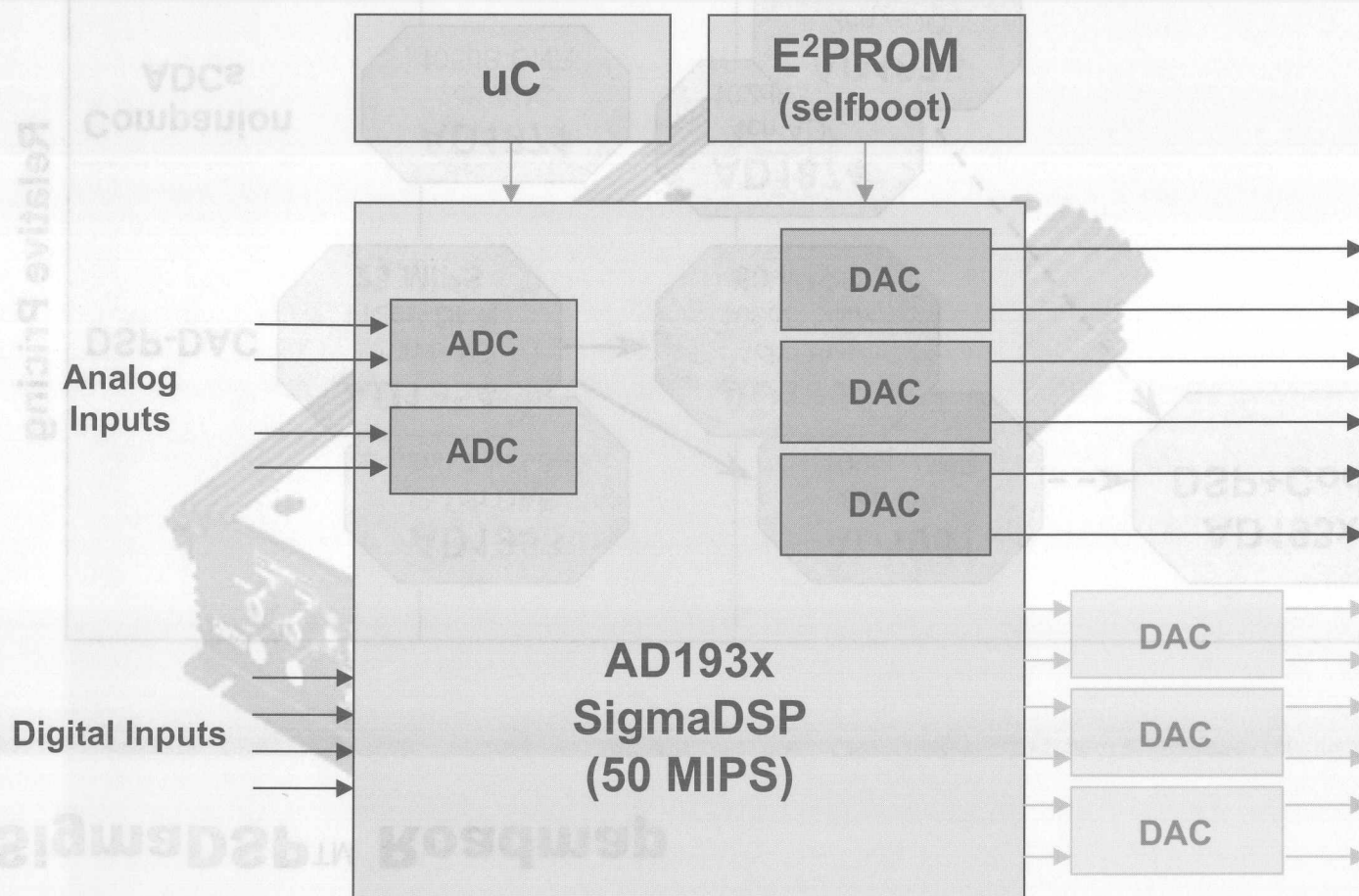
AD1953 + AD1836 Audio System

4 Analog In, (up to) 9 Analog Out, 25 SDSP-MIPS

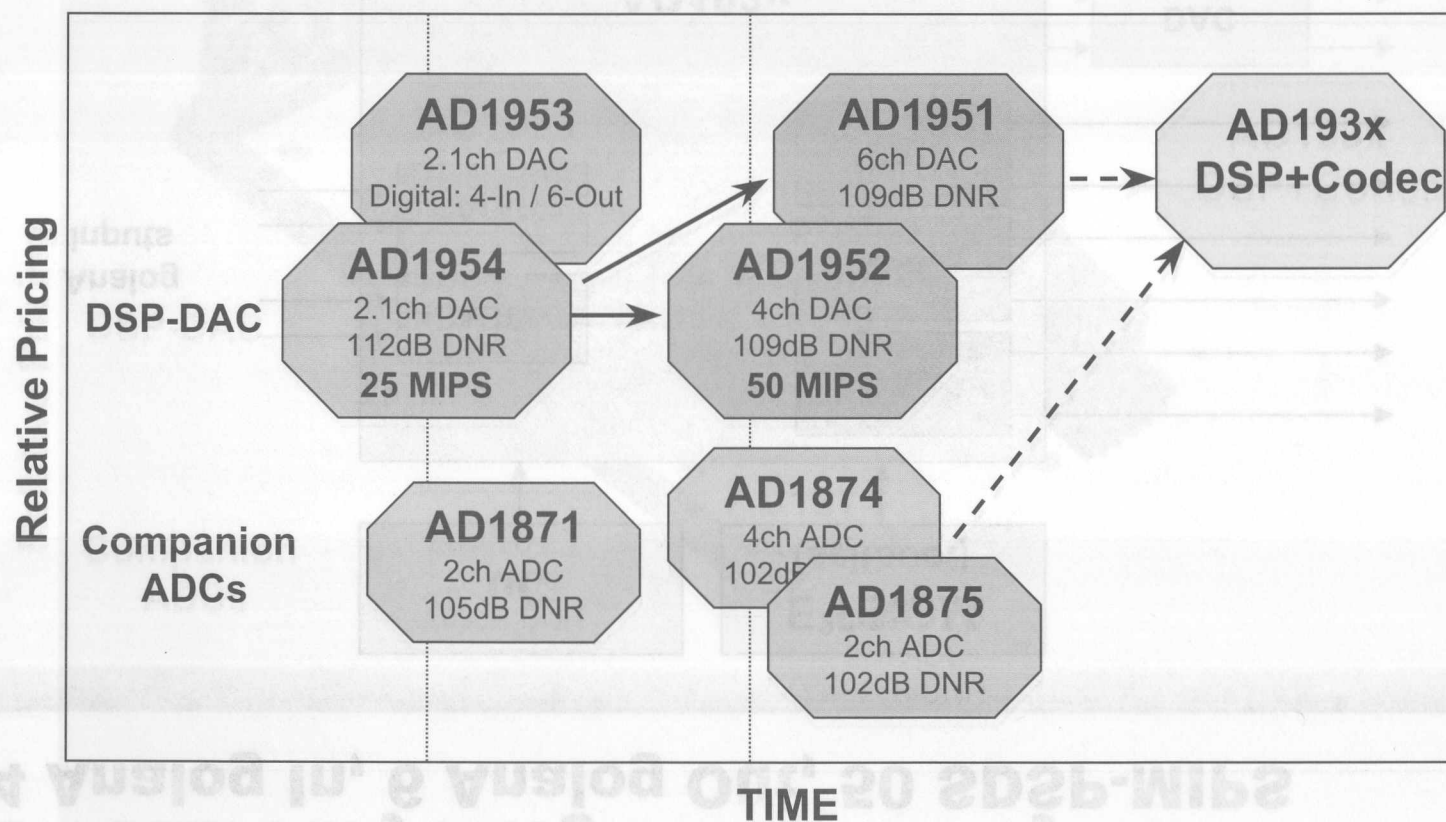


2nd Gen: Fully integrated Audio System

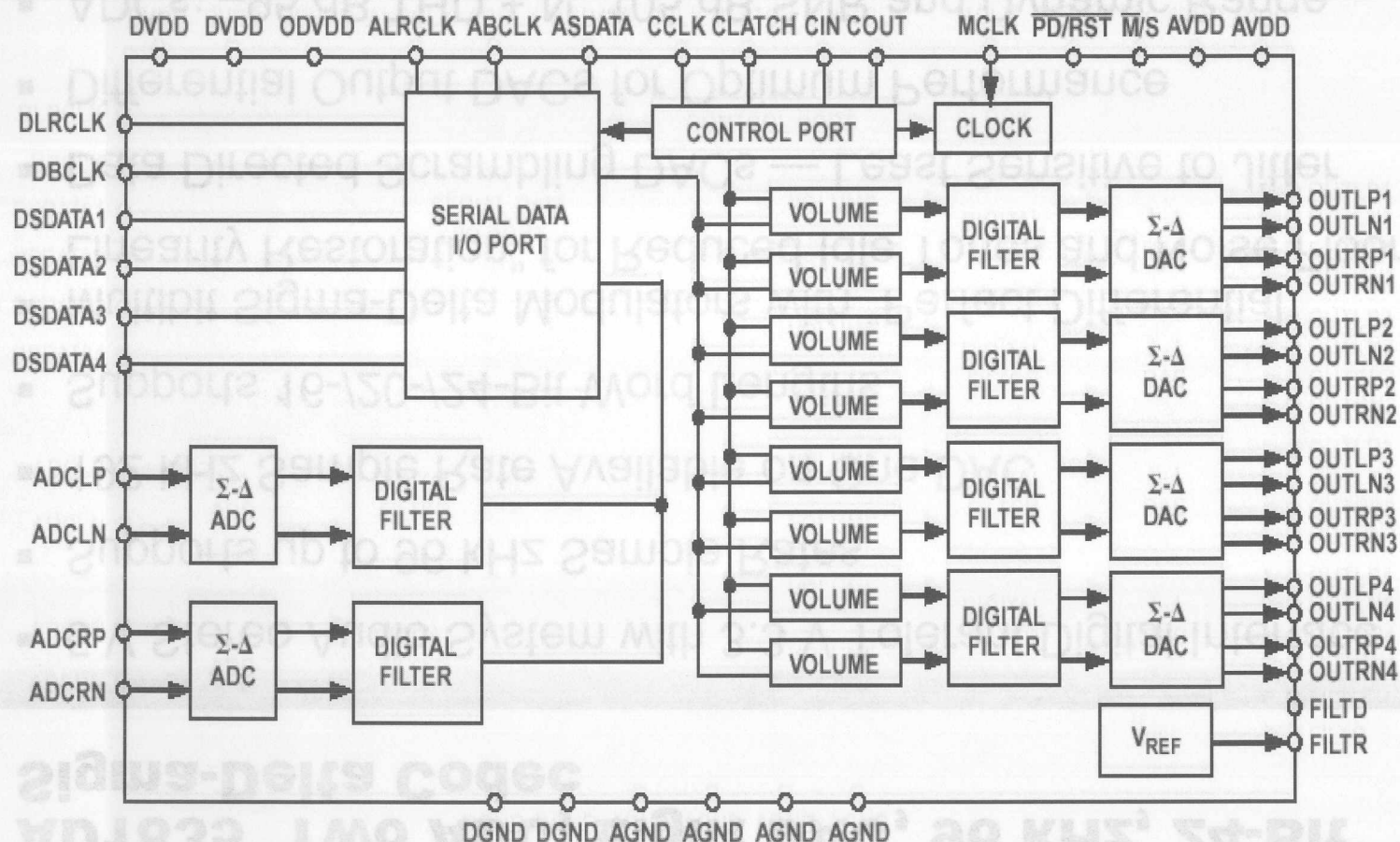
4 Analog In, 6 Analog Out, 50 SDSP-MIPS



SigmaDSP™ Roadmap



AD1835 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec



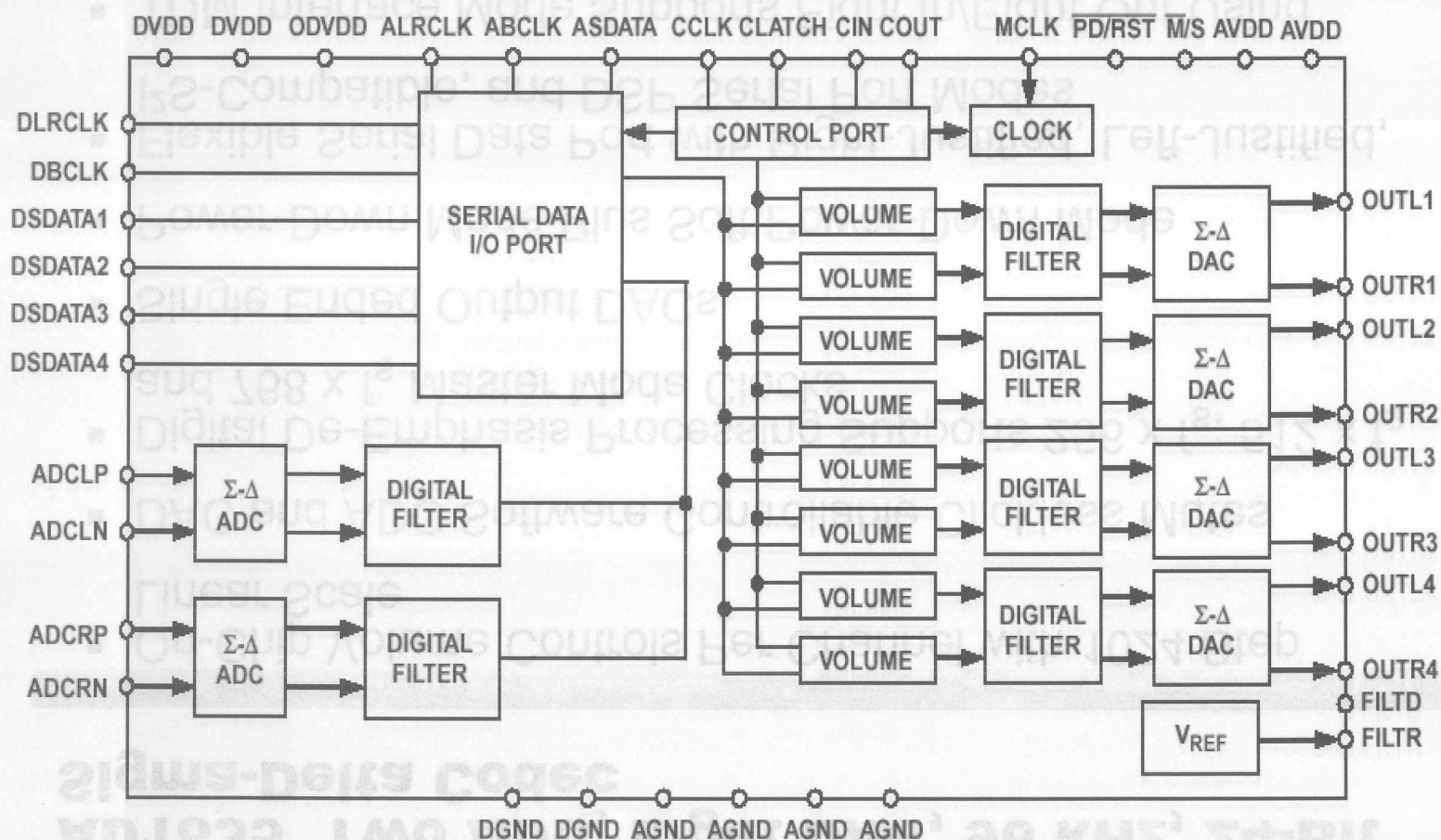
AD1835 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports up to 96 kHz Sample Rates
- 192 kHz Sample Rate Available on One DAC
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs — Least Sensitive to Jitter
- Differential Output DACs for Optimum Performance
- ADCs: -95 dB THD + N, 105 dB SNR and Dynamic Range
- DACs: -95 dB THD + N, 108 dB SNR and Dynamic Range

AD1835 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024 Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing Supports $256 \times f_s$, $512 \times f_s$, and $768 \times f_s$ Master Mode Clocks
- Single Ended Output DACs
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible, and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using Single SHARC SPORT
- 52-Lead MQFP Plastic Package

AD1837 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec



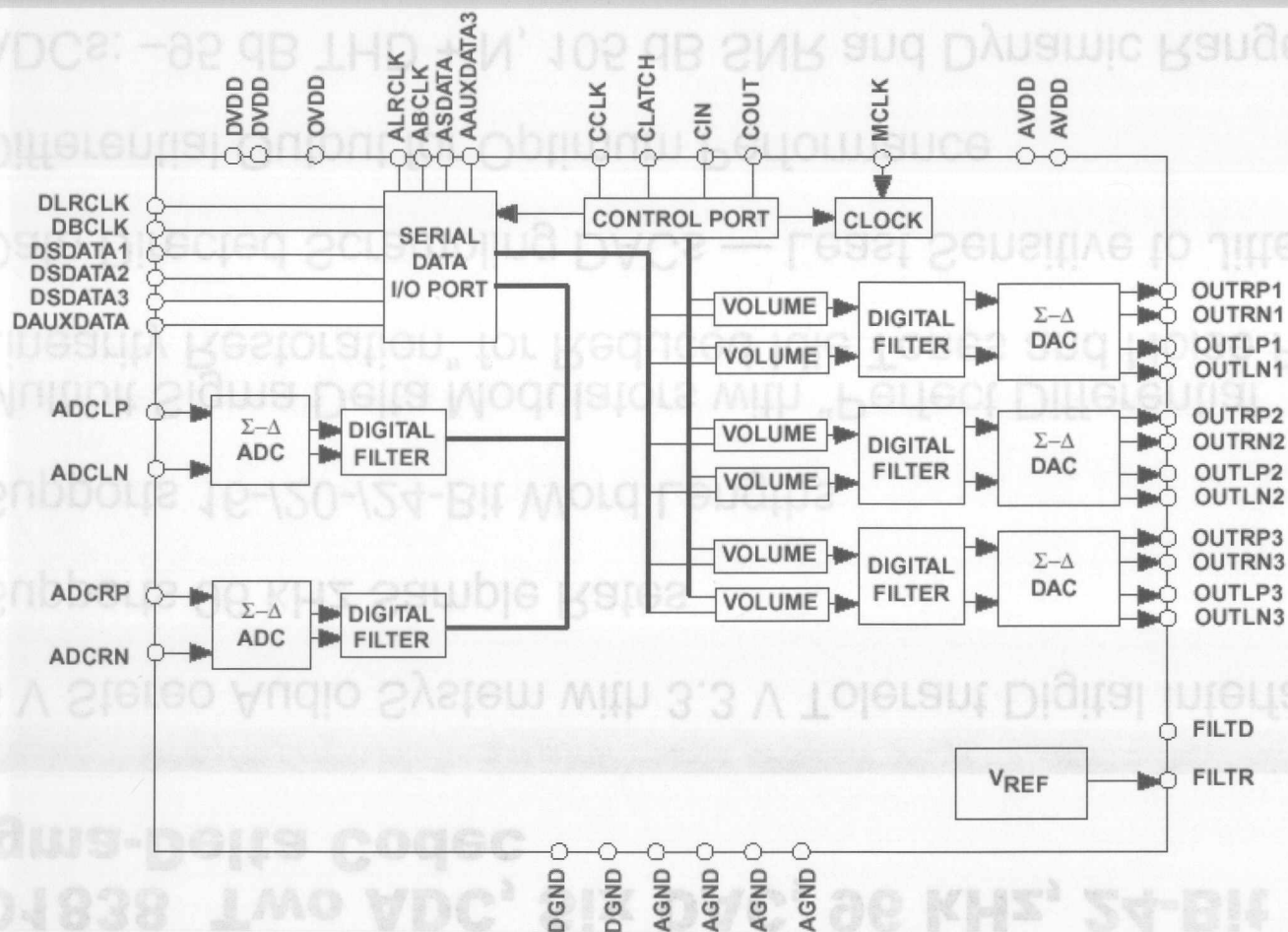
AD1837 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports up to 96 kHz Sample Rates
- 192 kHz Sample Rate Available on one DAC
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs — Least Sensitive to Jitter
- Single Ended Outputs
- ADCs: -95 dB THD + N, 105 dB SNR and 105 dB Dynamic Range
- DACs: -92 dB THD + N, 108 dB SNR and 107 dB Dynamic Range

AD1837 Two ADC, Eight DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024 Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports $256 \times f_s$, $512 \times f_s$, and $768 \times f_s$ Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using Single SHARC SPORT
- 52-Lead MQFP Plastic Package

AD1838 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec



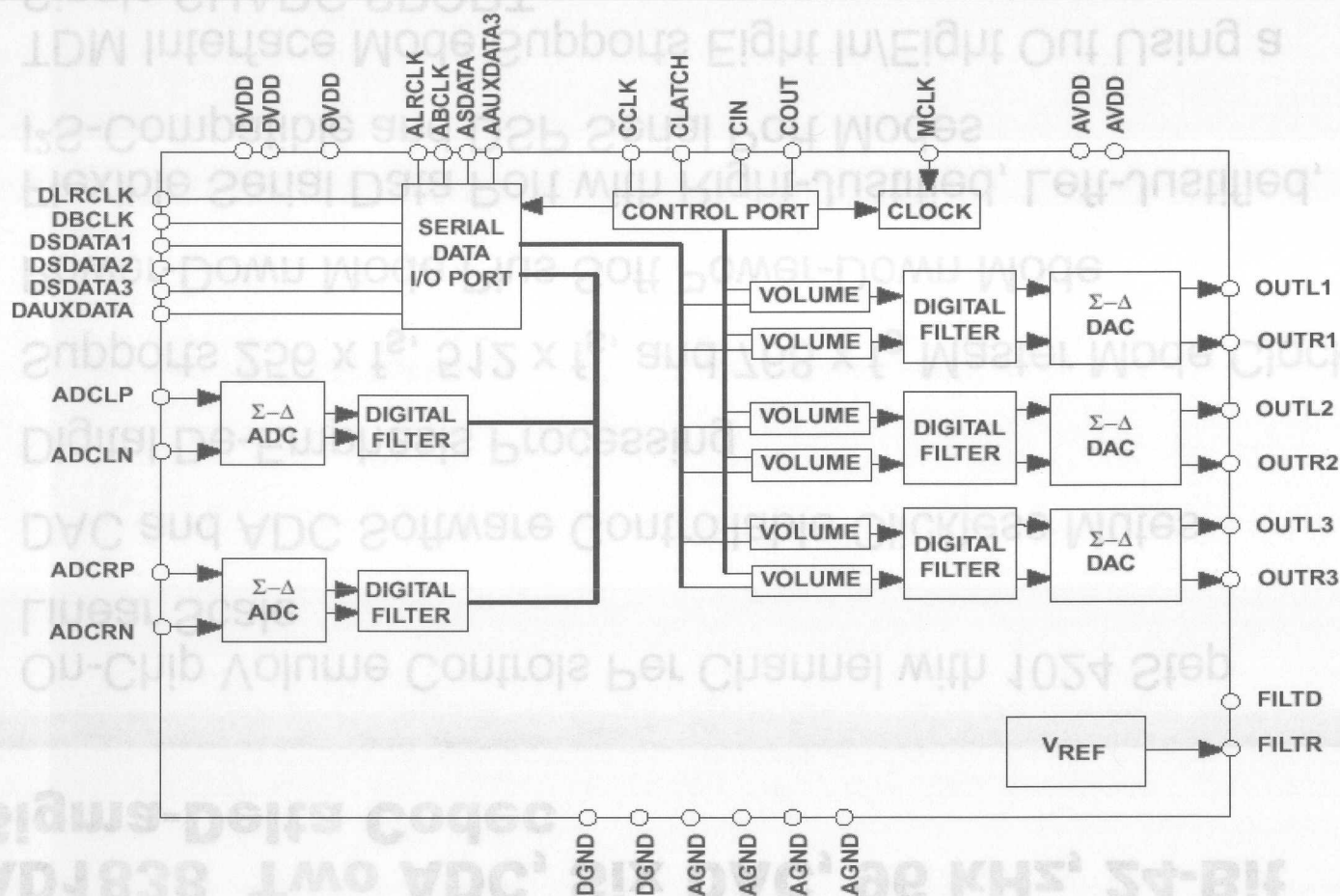
AD1838 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs — Least Sensitive to Jitter
- Differential Output for Optimum Performance
- ADCs: -95 dB THD + N, 105 dB SNR and Dynamic Range
- DACs: -95 dB THD + N, 108 dB SNR and Dynamic Range

AD1838 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-Chip Volume Controls Per Channel with 1024 Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports $256 \times f_s$, $512 \times f_s$, and $768 \times f_s$ Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using a Single SHARC SPORT
- 52-Lead MQFP Plastic Package

AD1839 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec



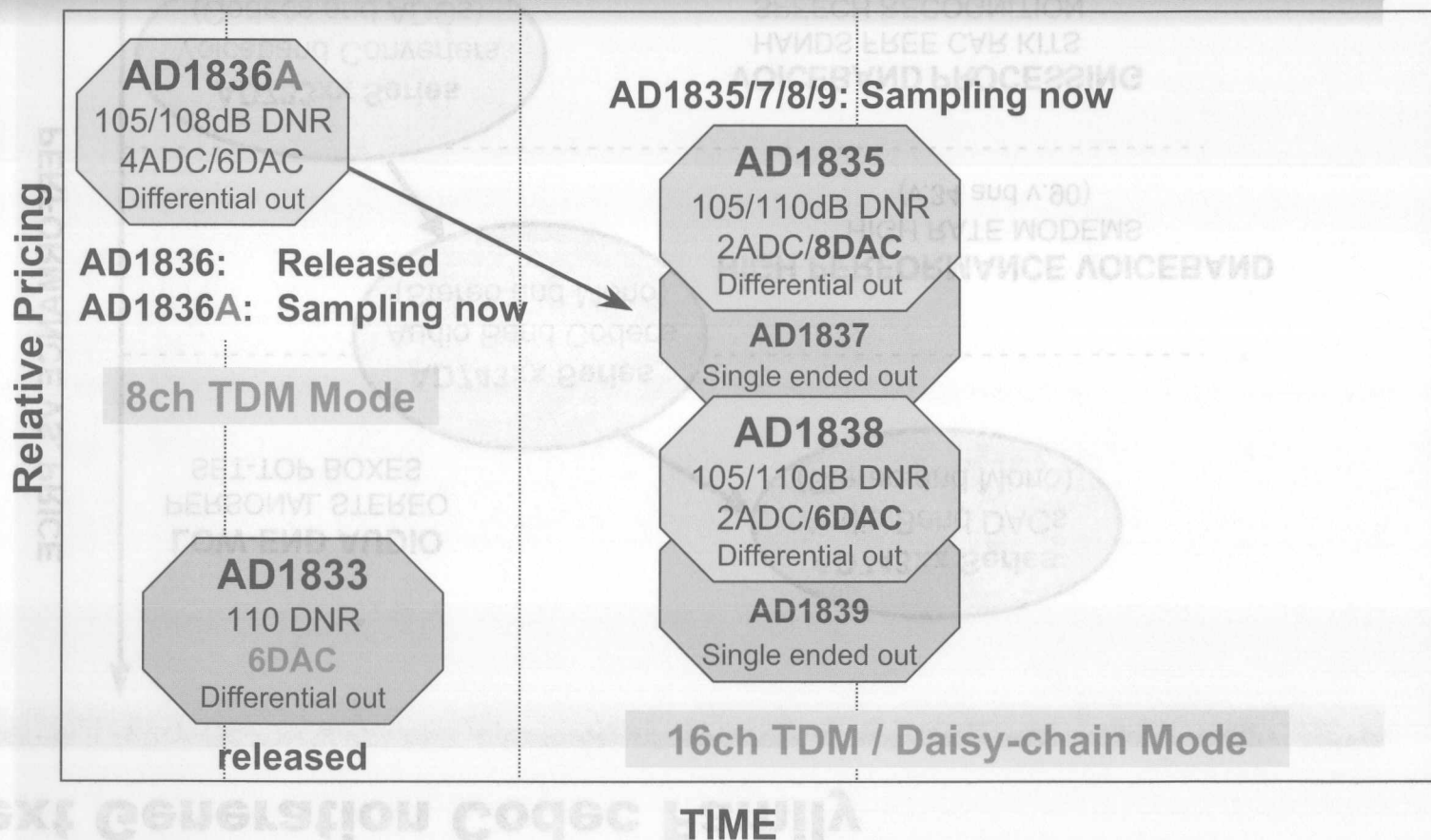
AD1839 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma Delta Modulators with “Perfect Differential Linearity Restoration” for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs — Least Sensitive to Jitter
- Differential ADC Inputs
- Single-Ended DAC Outputs
- ADCs: -95 dB THD + N, 105 dB SNR and Dynamic Range
- DACs: -92 dB THD + N, 108 dB SNR and Dynamic Range

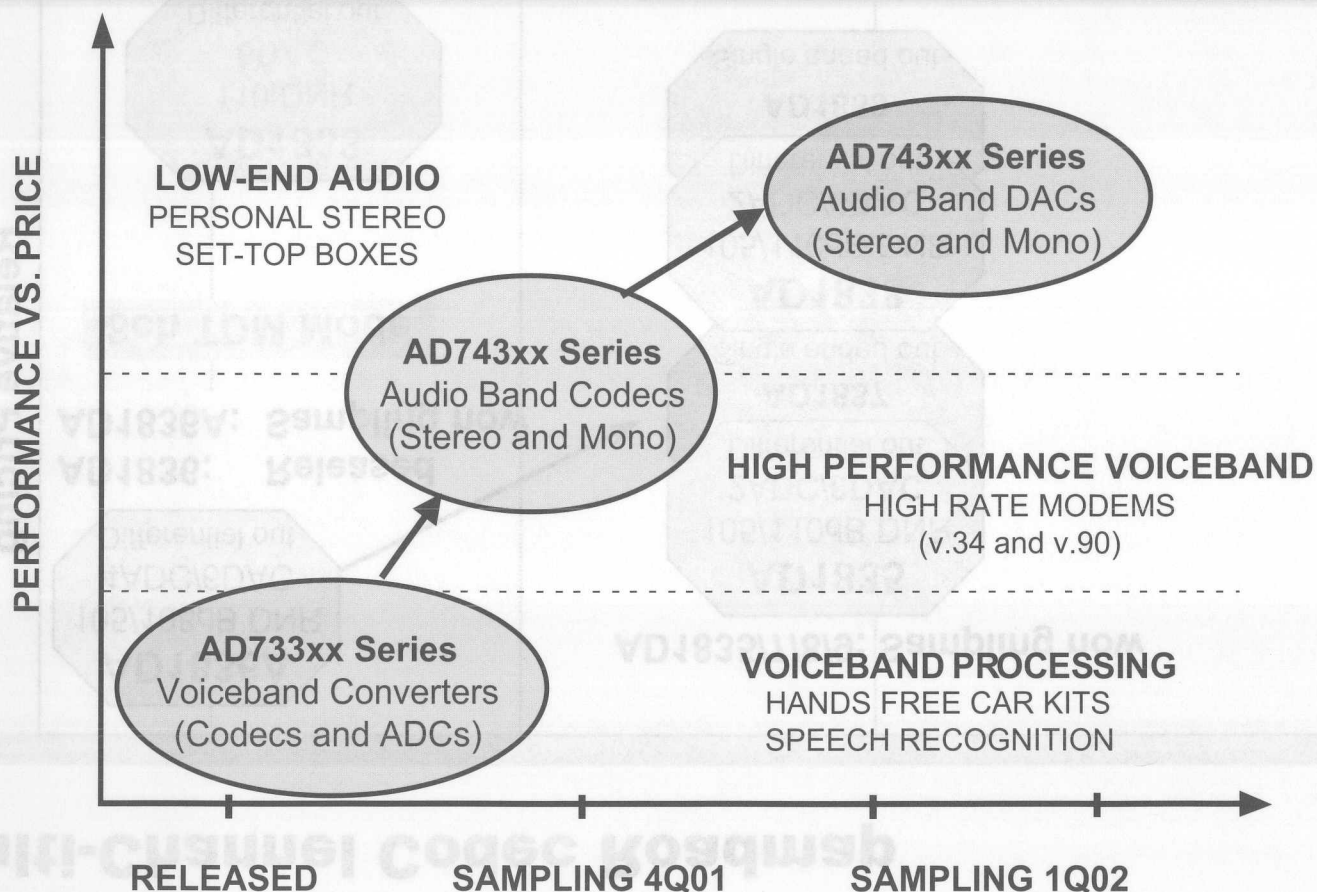
AD1839 Two ADC, Six DAC, 96 kHz, 24-Bit Sigma-Delta Codec

- On-chip Volume Controls Per Channel with 1024 Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports $256 \times f_s$, $512 \times f_s$, and $768 \times f_s$ Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
- TDM Interface Mode Supports Eight In/Eight Out Using a Single SHARC SPORT
- 52-Lead MQFP Plastic Package

Multi-Channel Codec Roadmap



Next Generation Codec Family

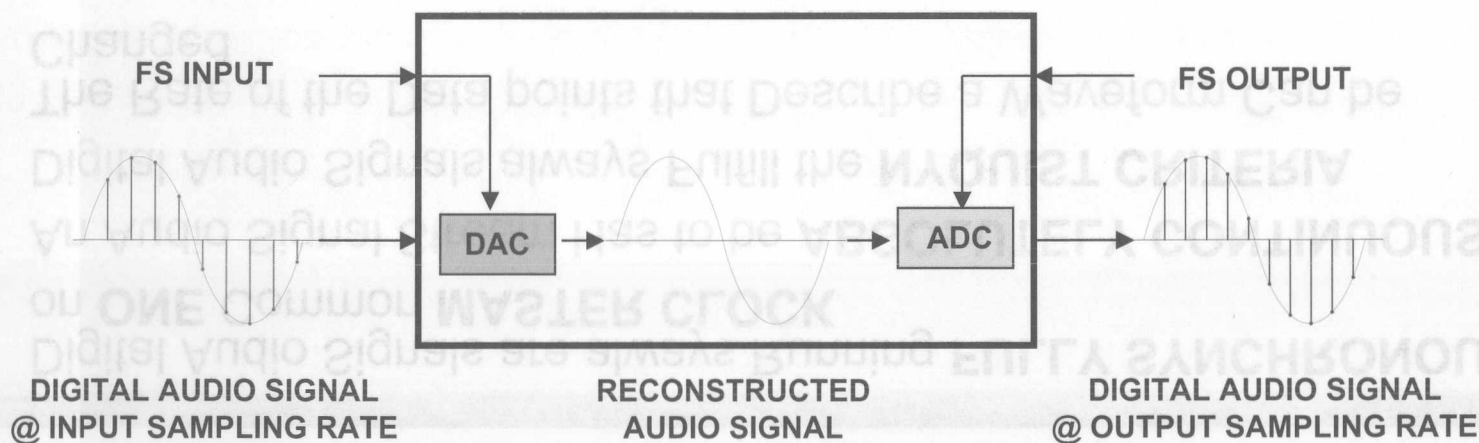


Digital Audio A Fully Synchronous Signal

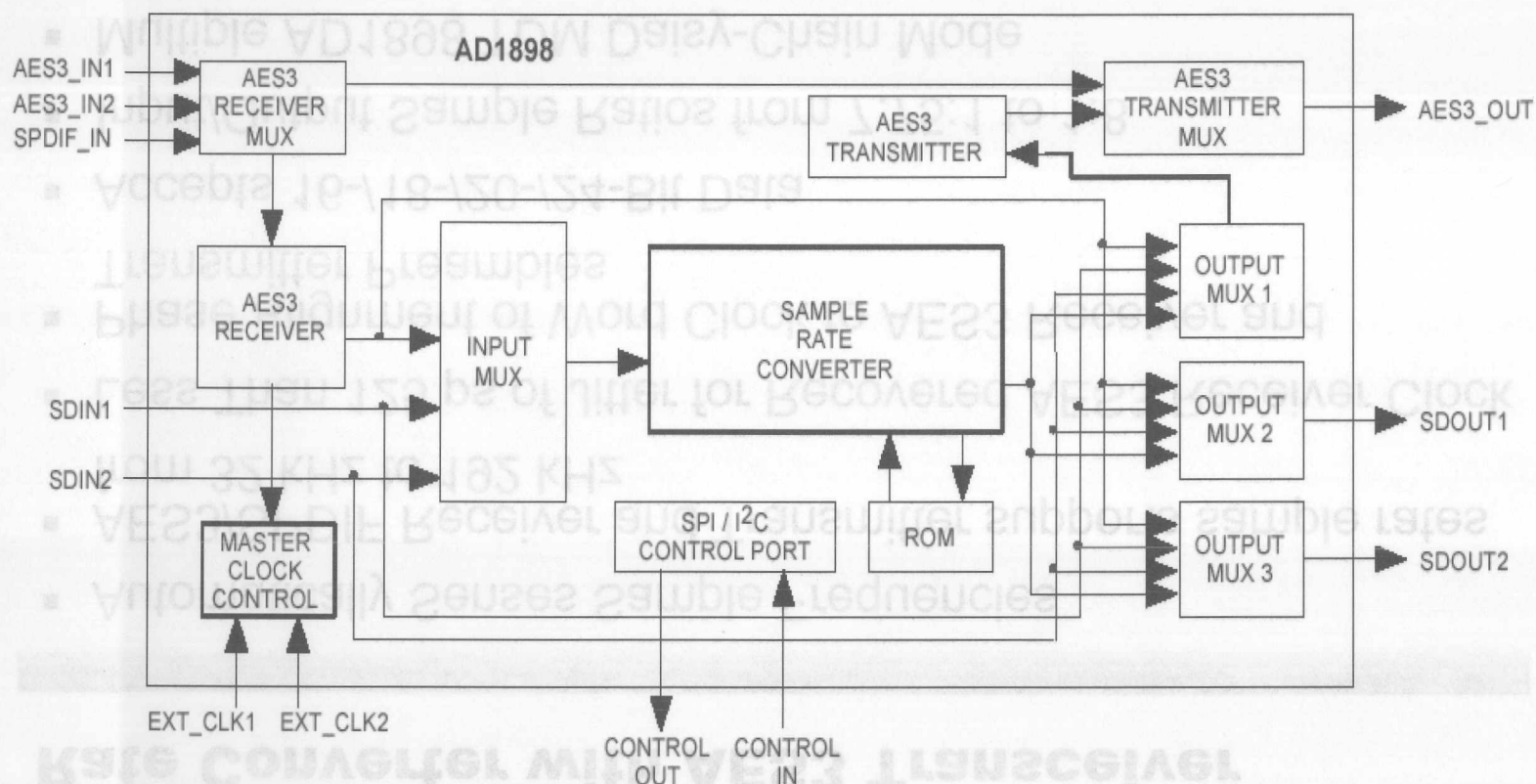
- Digital Audio Signals are always Running **FULLY SYNCHRONOUS** on **ONE** Common **MASTER CLOCK**
- An Audio Signal Stream Has to be **ABSOLUTELY CONTINUOUS**
- Digital Audio Signals always Fulfill the **NYQUIST CRITERIA**
- The Rate of the Data points that Describe a Waveform Can be Changed
- When Changed, an Entirely New Stream of Data Has to be Calculated
- This New Stream of Data is Entirely Different Data, But Describes Exactly the Same Waveform
- If the New Sampling Rate is Lower Than the Original Sampling Rate, the Audio Waveform Has to be Bandlimited to $F_{S_{new}}/2$ (Because of Nyquist)

Model of a Sample Rate Converter

- A SRC is a **FULLY DIGITAL ENGINE !!!**
- However, one way of thinking about it is:
 - It reconstructs the signal, just like a DAC would do
 - It resamples the signal, just like an ADC would do



AD1898 192 kHz Stereo Asynchronous Sample Rate Converter with AES3 Transceiver



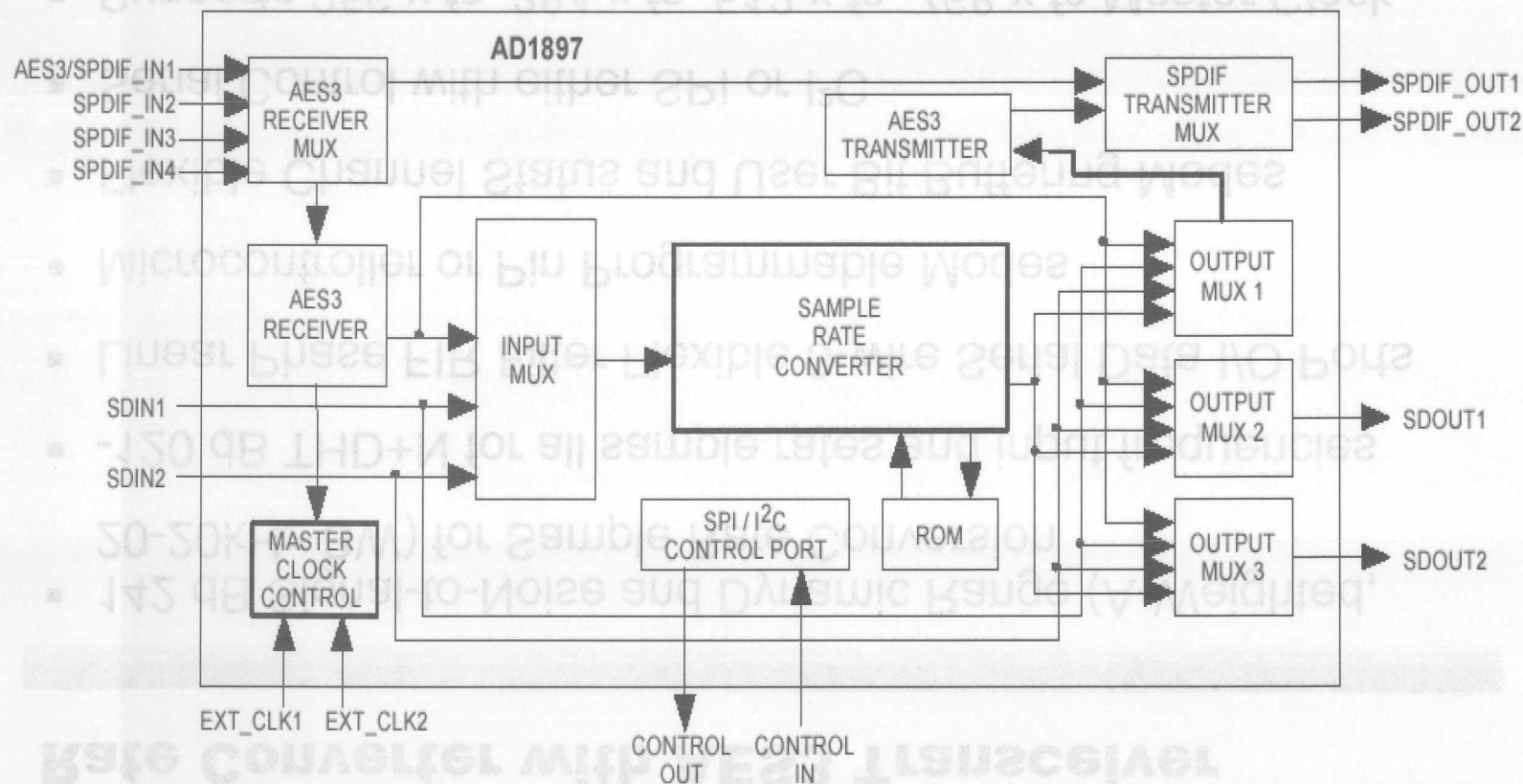
AD1898 192 kHz Stereo Asynchronous Sample Rate Converter with AES3 Transceiver

- Automatically Senses Sample Frequencies
- AES3/SPDIF Receiver and Transmitter supports sample rates from 32 kHz to 192 kHz
- Less Than 125 ps of Jitter for Recovered AES3 Receiver Clock
- Phase Alignment of Word Clock to AES3 Receiver and Transmitter Preambles
- Accepts 16-/18-/20-/24-Bit Data
- Input/Output Sample Ratios from 7.75:1 to 1:8
- Multiple AD1898 TDM Daisy-Chain Mode
- Multiple AD1898 Matched-Phase Mode
- Two AES3 Differential Inputs, One S/PDIF Input
- One AES3 Differential Output

AD1898 192 kHz Stereo Asynchronous Sample Rate Converter with AES3 Transceiver

- 142 dB Signal-to-Noise and Dynamic Range (A-Weighted, 20-20kHz BW) for Sample Rate Conversion
- -120 dB THD+N for all sample rates and input frequencies
- Linear Phase FIR Filter Flexible 3-wire Serial Data I/O Ports
- Microcontroller or Pin Programmable Modes
- Flexible Channel Status and User Bit Buffering Modes
- Serial Control with either SPI or I²C
- Supports 256 x fs, 384 x fs, 512 x fs, 768 x fs Master Clock
- 52 pin MQFP package

AD1897 192 kHz Stereo Asynchronous Sample Rate Converter with AES3 Transceiver



AD1897 192 kHz Stereo Asynchronous Sample Rate Converter with AES3 Transceiver

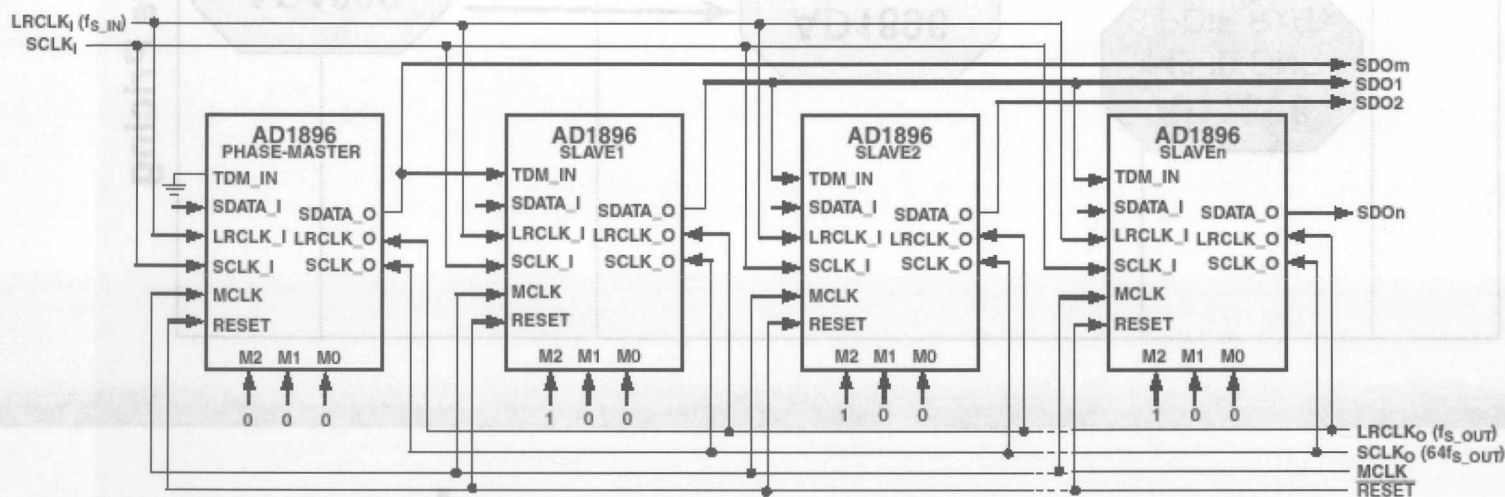
- Automatically Senses Sample Frequencies
- AES3/SPDIF Receiver and Transmitter supports sample rates from 32kHz to 192kHz
- Less Than 125 ps of Jitter for Recovered AES3 Receiver Clock
- Phase Alignment of Word Clock to AES3 Receiver and Transmitter Preambles
- Accepts 16-/18-/20-/24-Bit Data
- Input/Output Sample Ratios from 7.75:1 to 1:8
- Multiple AD1897 TDM Daisy-Chain Mode
- Multiple AD1897 Matched-Phase Mode
- Four S/PDIF Inputs (One Differential, Three Single-Ended)
- Two S/PDIF Outputs

AD1897 192 kHz Stereo Asynchronous Sample Rate Converter with AES3 Transceiver

- Flexible 3-wire Serial Data I/O Ports
- Flexible Channel Status and User Bit Buffering Modes
- Serial Control with either SPI or I²C
- 128 dB Signal-to-Noise and Dynamic Range (A-Weighted, 20-20kHz BW) for Sample Rate Conversion
- -118 dB THD+N for all Sample Rates and Input Frequencies
- Linear Phase FIR Filter
- Supports 256 x fs, 384 x fs, 512 x fs, 768 x fs Master Clock
- 48 pin LQFP package

So What is Phase Match Mode?

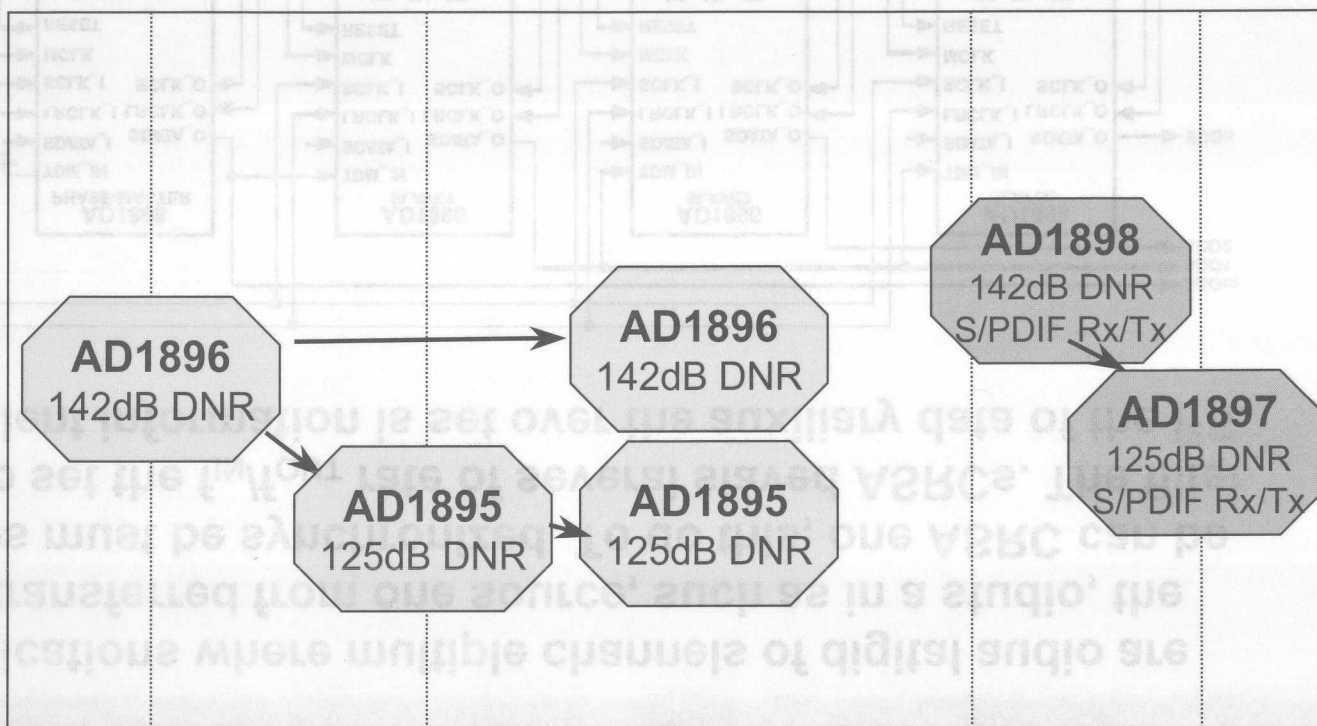
In applications where multiple channels of digital audio are being transferred from one source, such as in a studio, the sources must be synchronized. To do this, one ASRC can be used to set the f_{IN}/f_{OUT} rate of several slaved ASRCs. The filter coefficient information is set over the auxiliary data of the I²S.



PHASE-MATCH MODE CONFIGURATION

SRC Roadmap

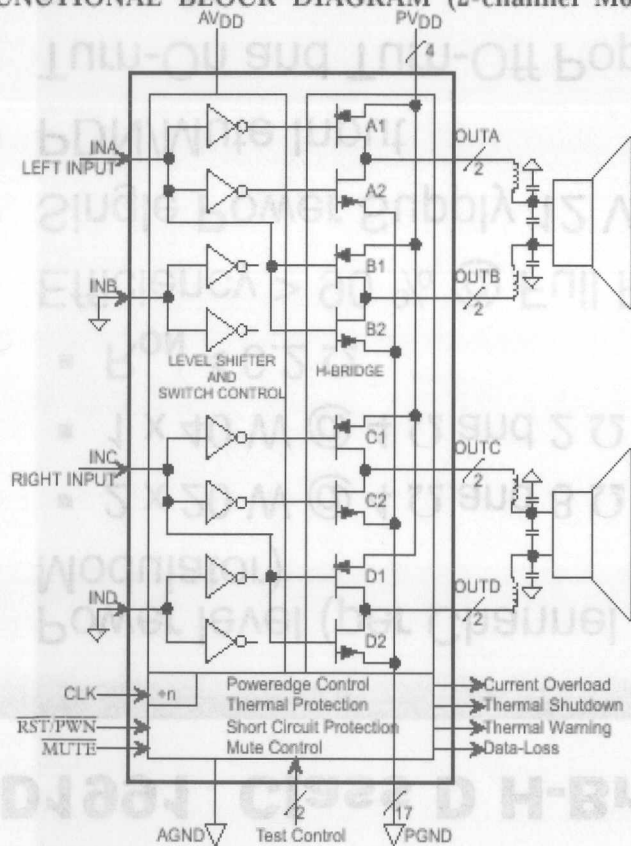
Relative Pricing



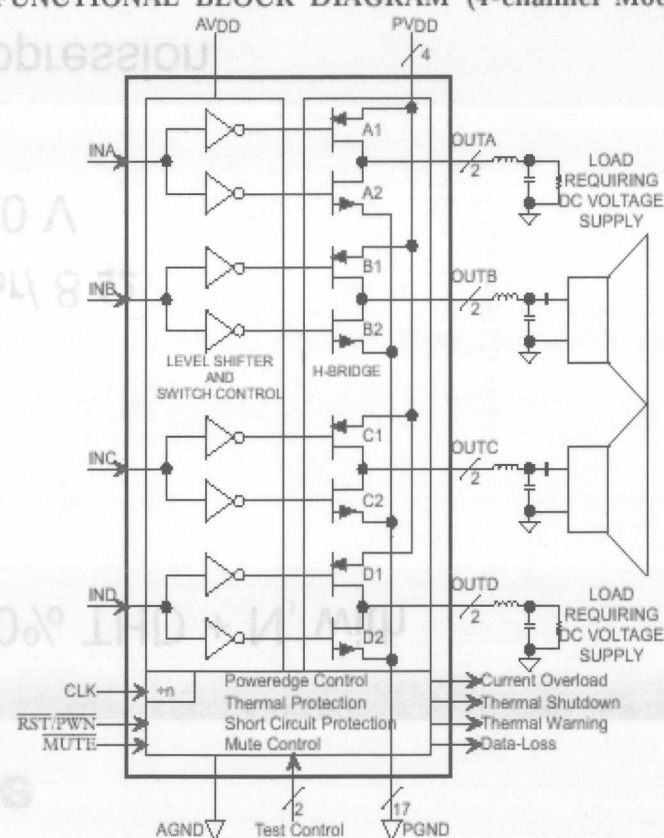
TIME

AD1991 Class-D H-Bridge

FUNCTIONAL BLOCK DIAGRAM (2-channel Mode)



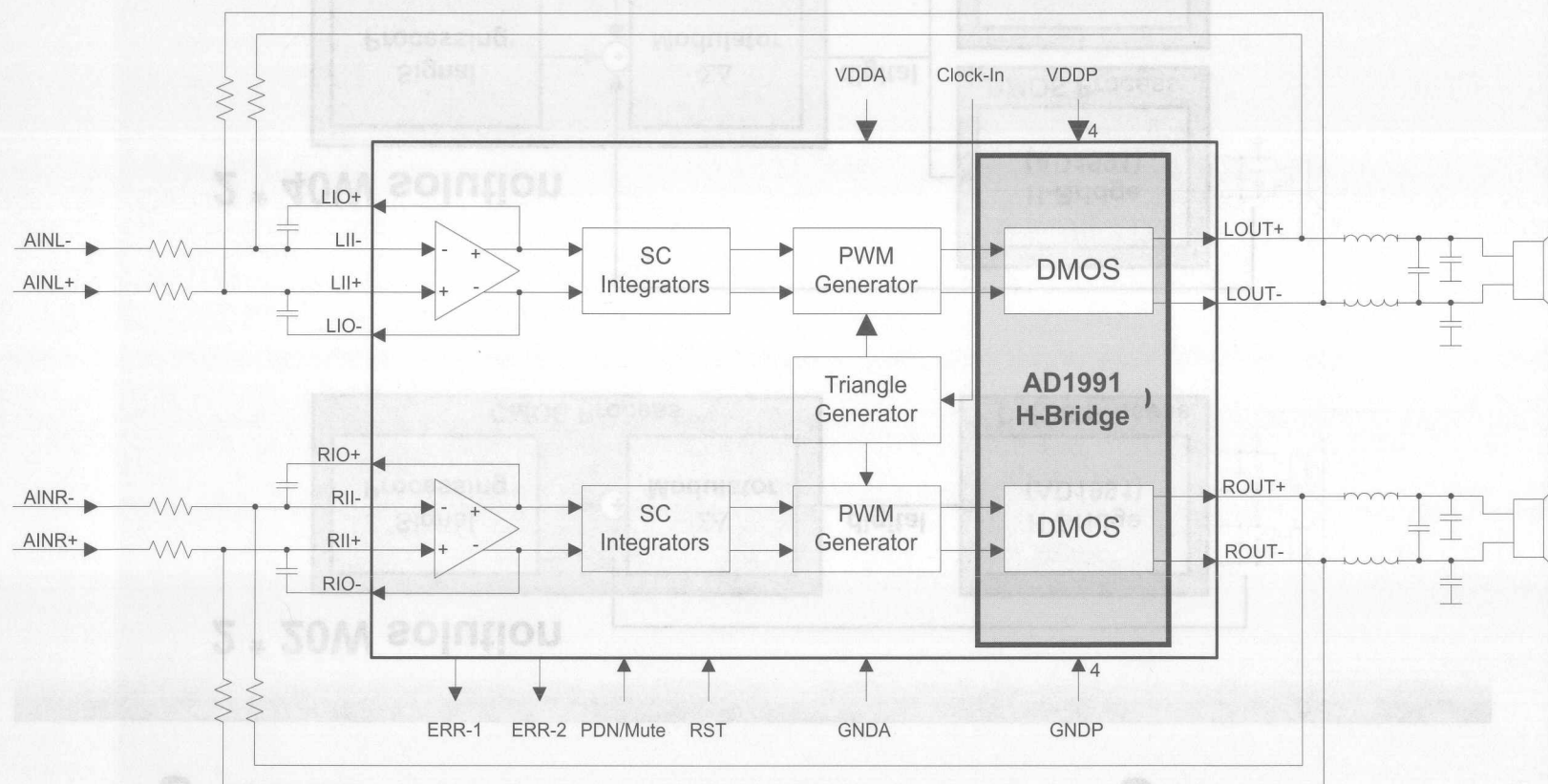
FUNCTIONAL BLOCK DIAGRAM (4-channel Mode)



AD1991 Class D H-Bridge

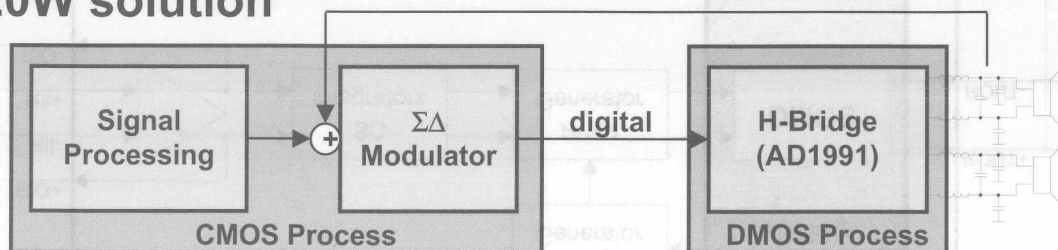
- Power level (per Channel @ 10% THD + N, with Modulator)
 - 2 x 20 W @ 4 Ω and 8 Ω
 - 1 x 40 W @ 4 Ω and 2 Ω
 - $R_{ON} < 0.2 \Omega$
- Efficiency > 90 % @ Full Power/ 8 Ω
- Single Power Supply 12 V – 20 V
- PDN/Mute Input
- Turn-On and Turn-Off Pop Suppression
- Short Circuit Warning and Protection
- Over-Temperature Warning and Protection
- 2-Channel Bridged Outputs (BTL) or 4-Channel Single Ended or 1-Channel High Current BTL

High performance Class-D solution

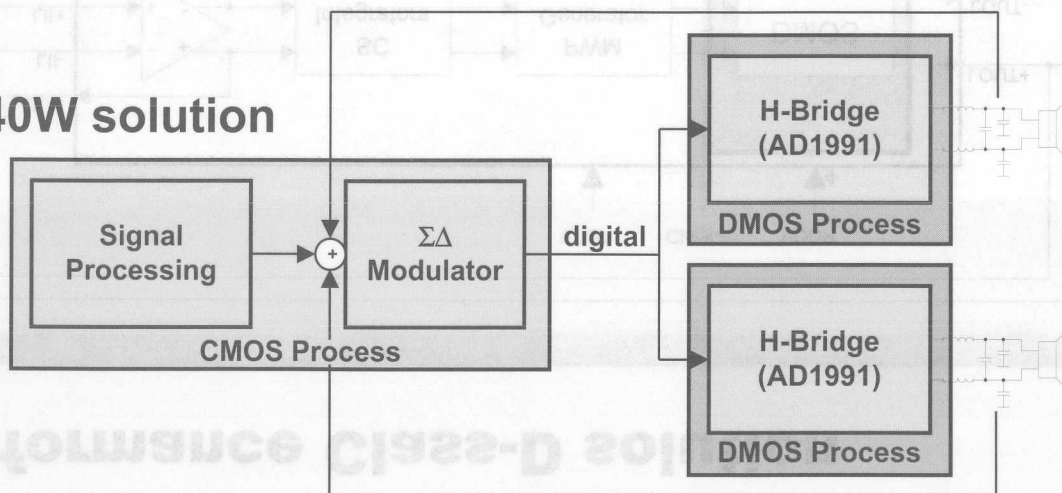


Integration of Modulator and H-Bridge

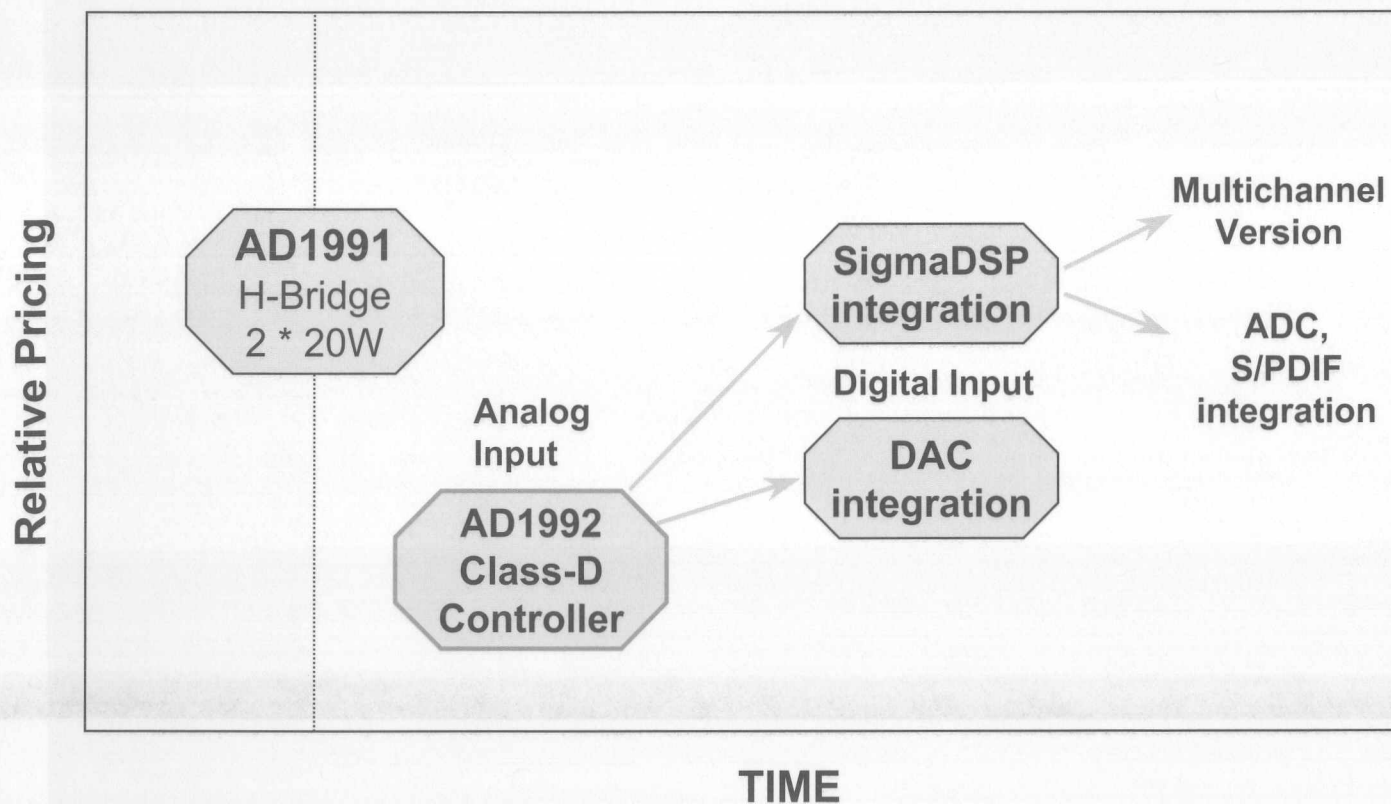
2 * 20W solution



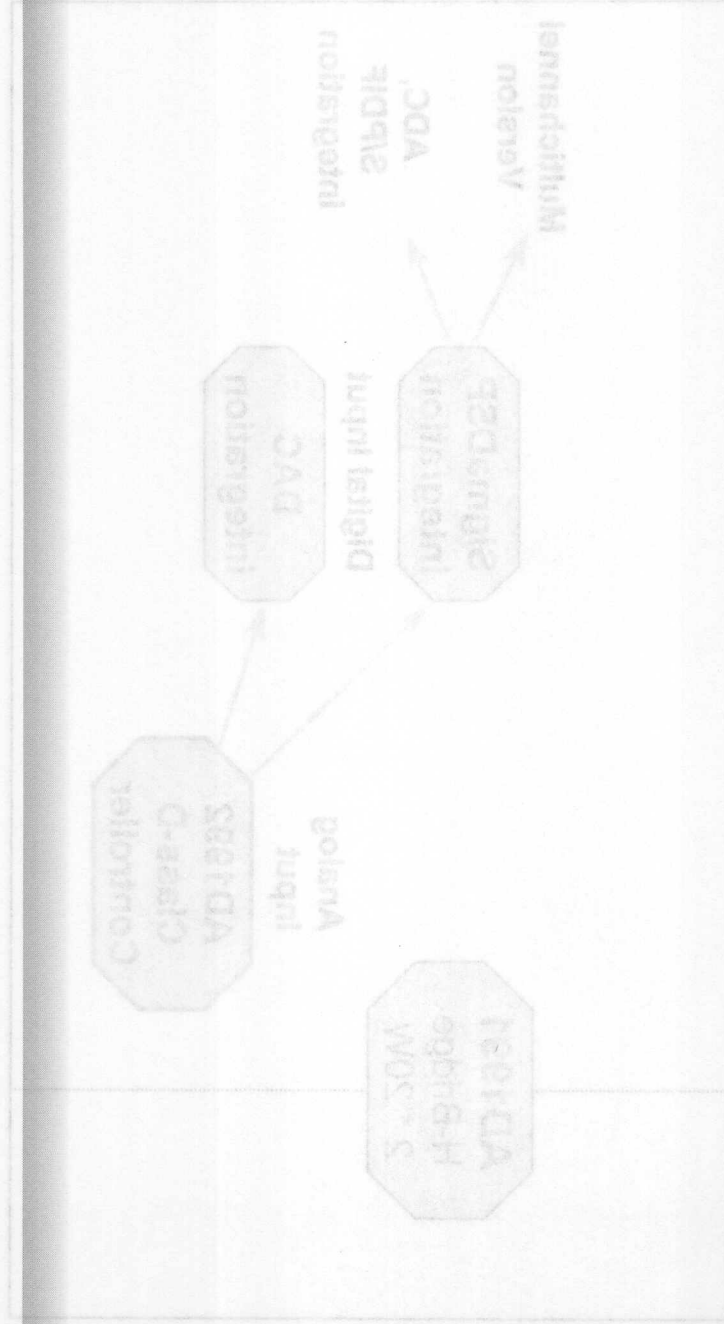
2 * 40W solution



Class-D Product Roadmap



TIME

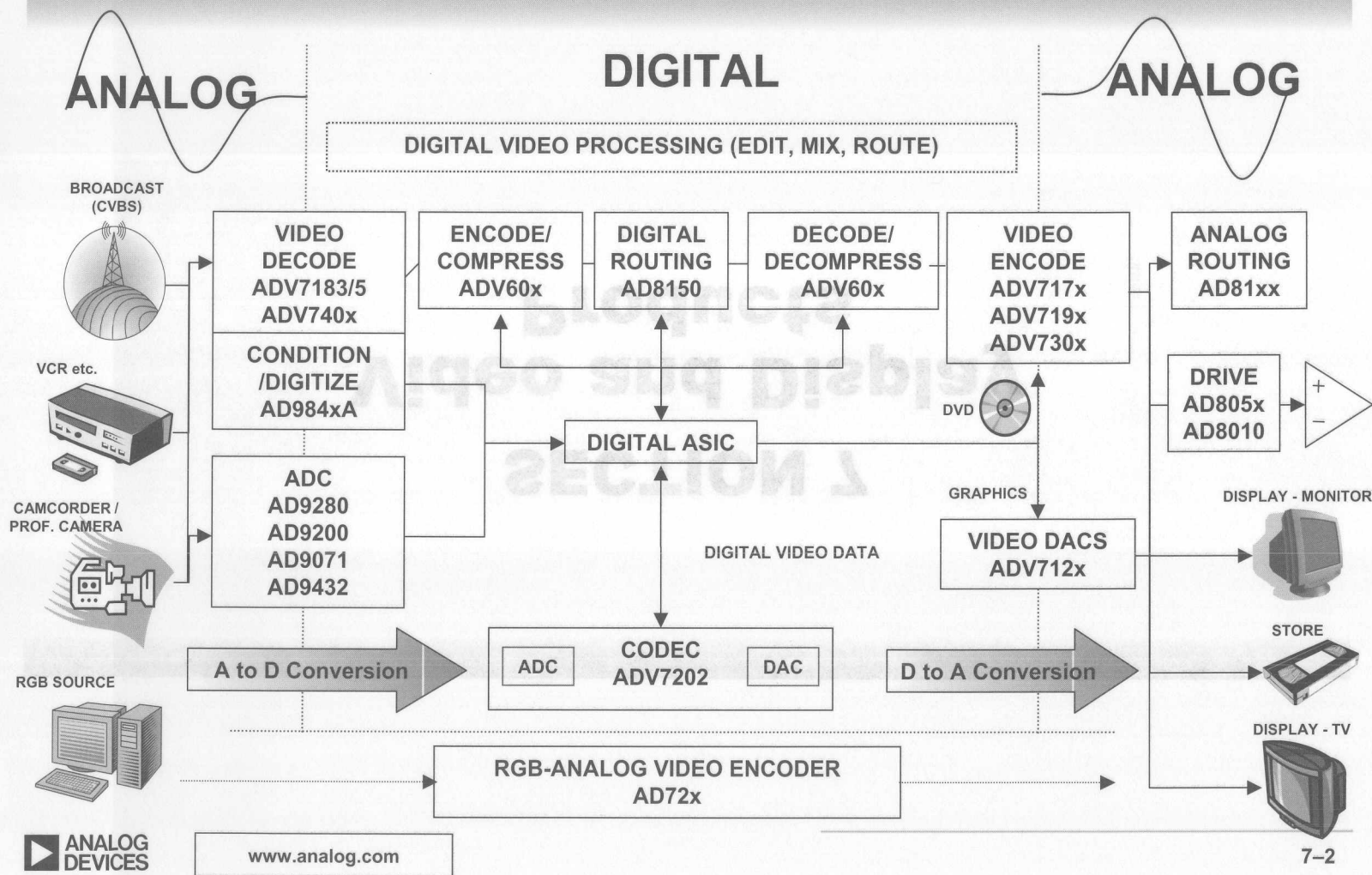


Class-D Product Roadmap

SECTION 7

Video and Display Products

Where ADI Participates:





www.analog.com

1-800-343-7300

Digital Video Decoders

component video compatible with NTSC, PAL, SECAM, and YUV analog and digital television signals into digital CCIR-601 4:2:2. A Digital Video Decoder converts CVBS, S-Video, and YUV

What Are Digital Video Decoders?



www.analog.com

7-3

What Are Digital Video Decoders?

A Digital Video Decoder converts CVBS, S-Video, and YUV analog baseband television signals into digital CCIR-656 4:2:2 component video compatible with NTSC, PALB/D/G/H/I, PAL M, or PAL N.

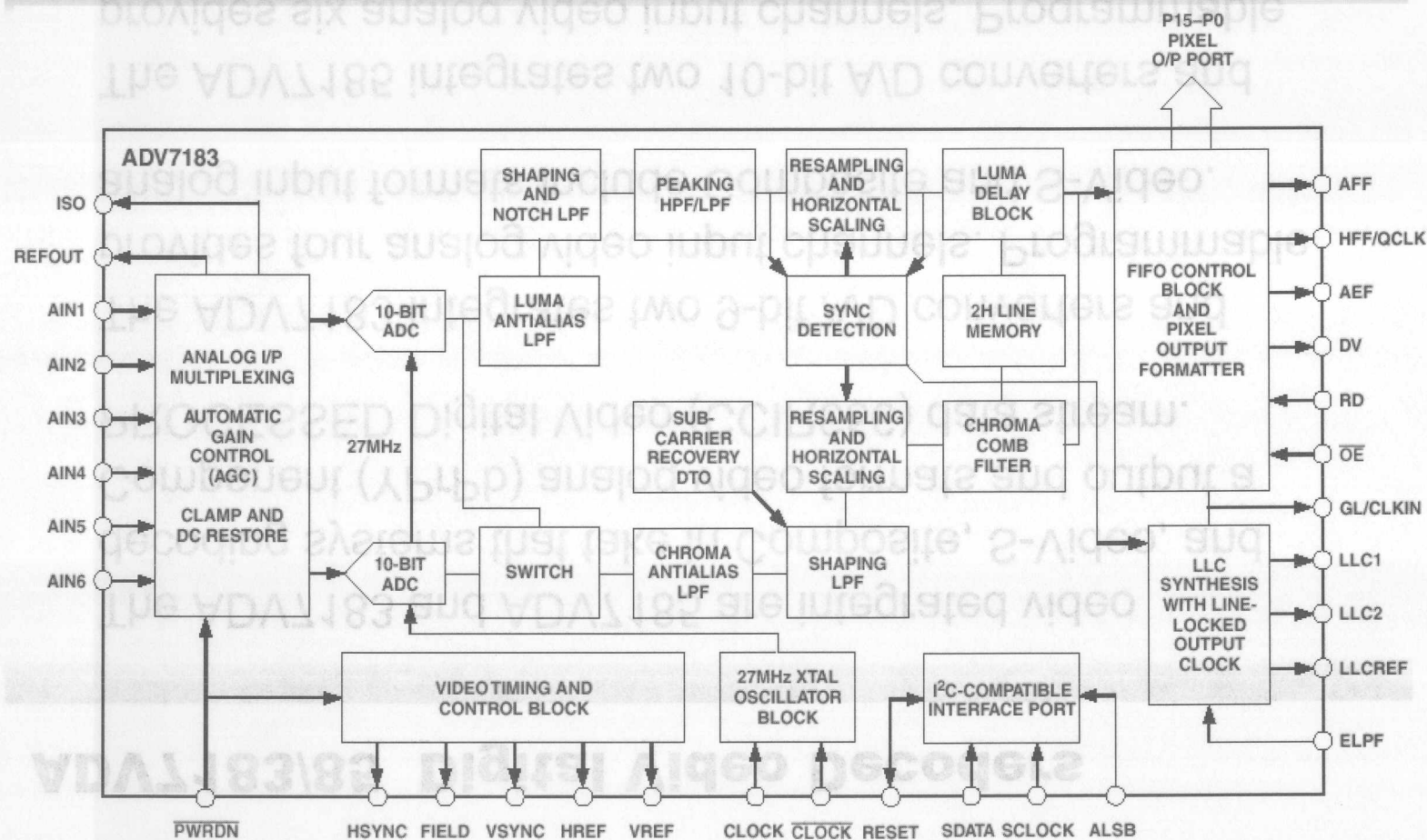
ADV7183/85 Digital Video Decoders

The ADV7183 and ADV7185 are integrated video decoding systems that take in Composite, S-Video, and Component (YPrPb) analog video formats and output a PROCESSED Digital Video (CCIR656) data stream.

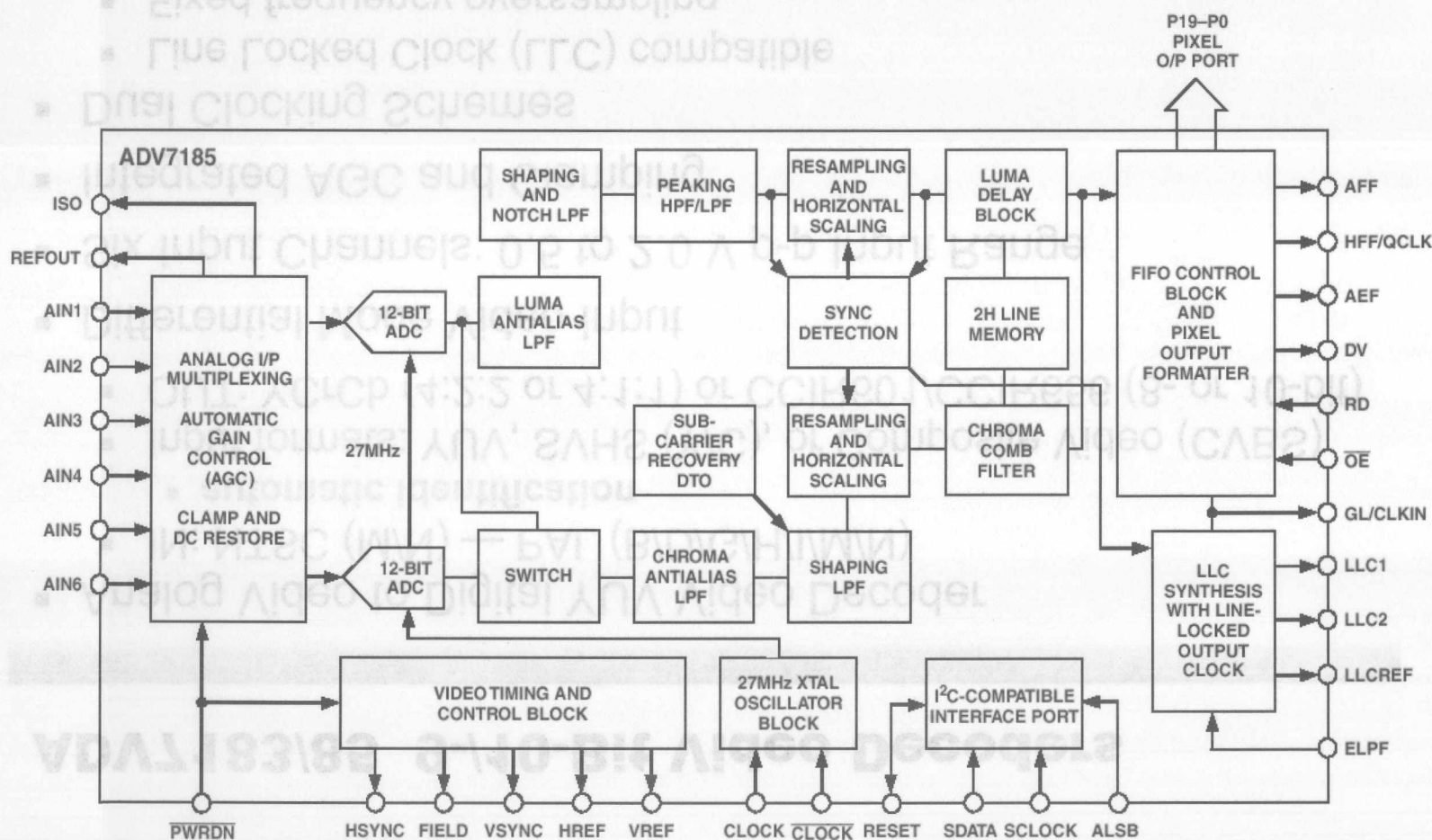
The ADV7183 integrates two 9-bit A/D converters and provides four analog video input channels. Programmable analog input formats include Composite and S-Video.

The ADV7185 integrates two 10-bit A/D converters and provides six analog video input channels. Programmable analog input formats include Composite, S-Video, and Component (YPrPb).

ADV7183 Video Decoder Block Diagram



ADV7185 Video Decoder Block Diagram



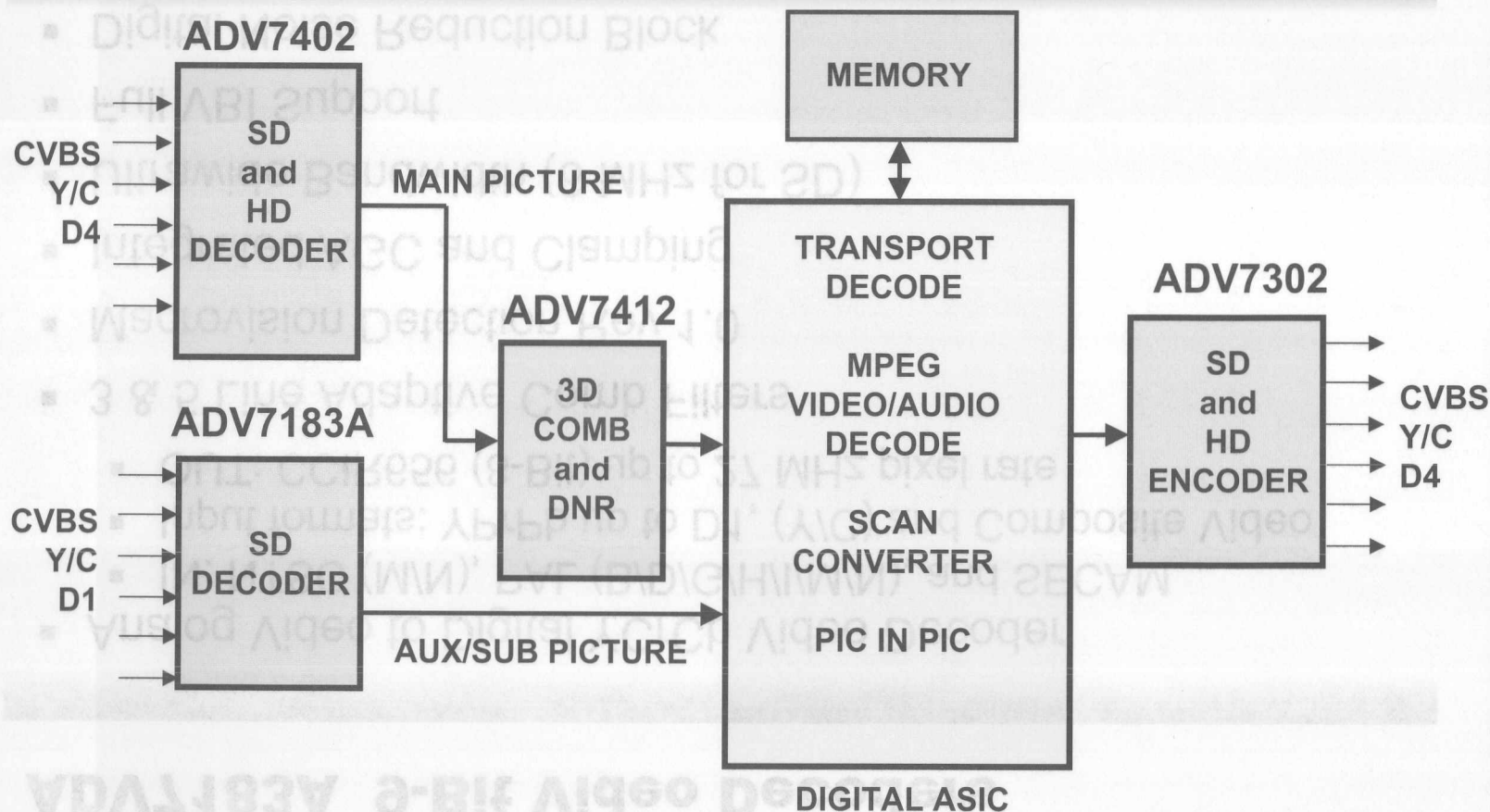
ADV7183/85 9-/10-Bit Video Decoders

- Analog Video to Digital YUV Video Decoder
 - IN: NTSC (M/N) — PAL (B/D/G/H/I/M/N)
 - **automatic identification**
 - Input formats: YUV, SVHS (Y/C), or Composite Video (CVBS)
 - OUT: YCrCb (4:2:2 or 4:1:1) or CCIR601/CCIR656 (8- or 10-bit)
- Differential Mode Video Input
- Six Input Channels: 0.5 to 2.0 V p-p Input Range
- Integrated AGC and Clamping
- Dual Clocking Schemes
 - Line Locked Clock (LLC) compatible
 - Fixed frequency oversampling
- Adaptive Digital Line Length Tracking
- On-Chip Video Timing Generator

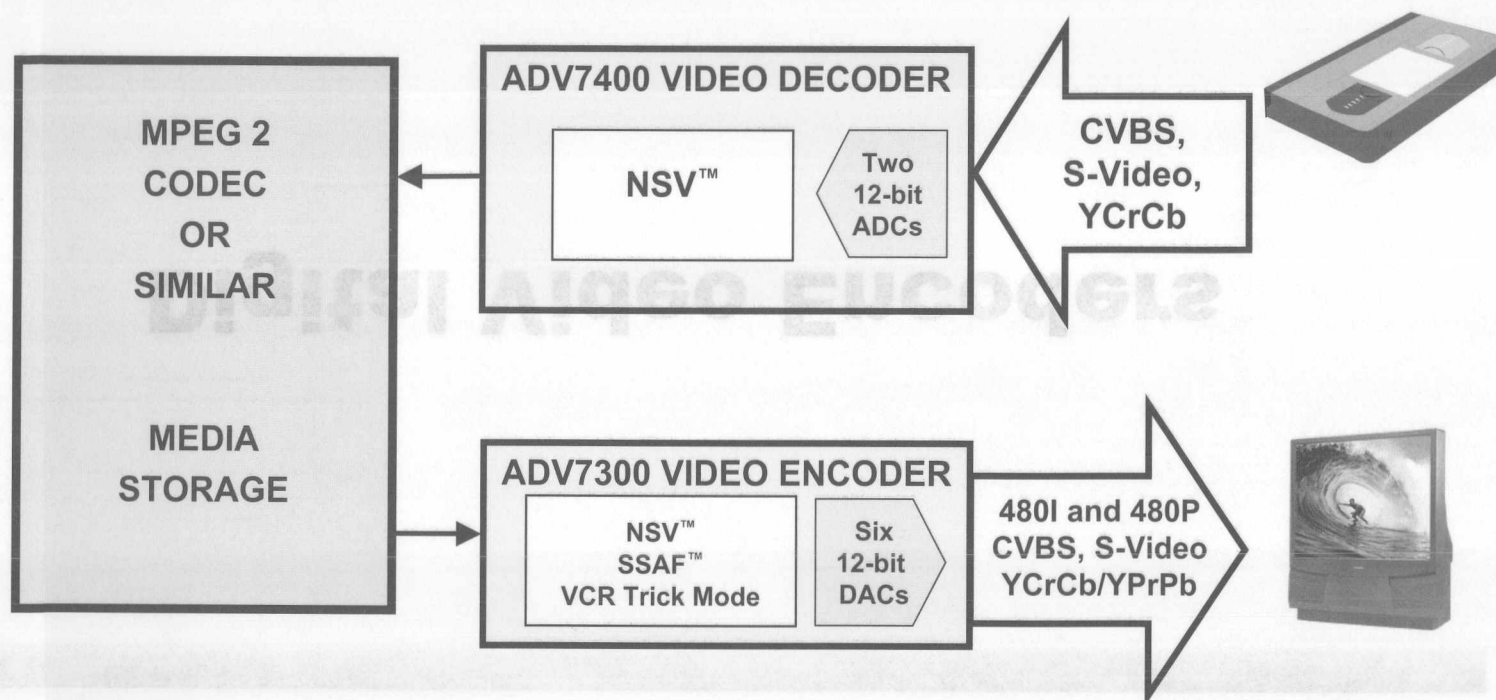
ADV7183A 9-Bit Video Decoders

- Analog Video to Digital YCrCb Video Decoder
 - IN: NTSC (M/N), PAL (B/D/G/H/I/M/N), and SECAM
 - Input formats: YPrPb up to D1, (Y/C) and Composite Video
 - OUT: CCIR656 (8-Bit) up to 27 MHz pixel rate
- 3 & 5 Line Adaptive Comb Filters
- Macrovision Detection Rev 1.0
- Integrated AGC and Clamping
- Ultrawide Bandwidth (6 MHz for SD)
- Full VBI Support
- Digital Noise Reduction Block
- SNR Measurement for Efficient Compression
- RGB SCART Input Support for Europe

Digital TV Application



Professional Video Recording





Digital Video Encoders

Professional Video Recording

What Are Digital Video Encoders?

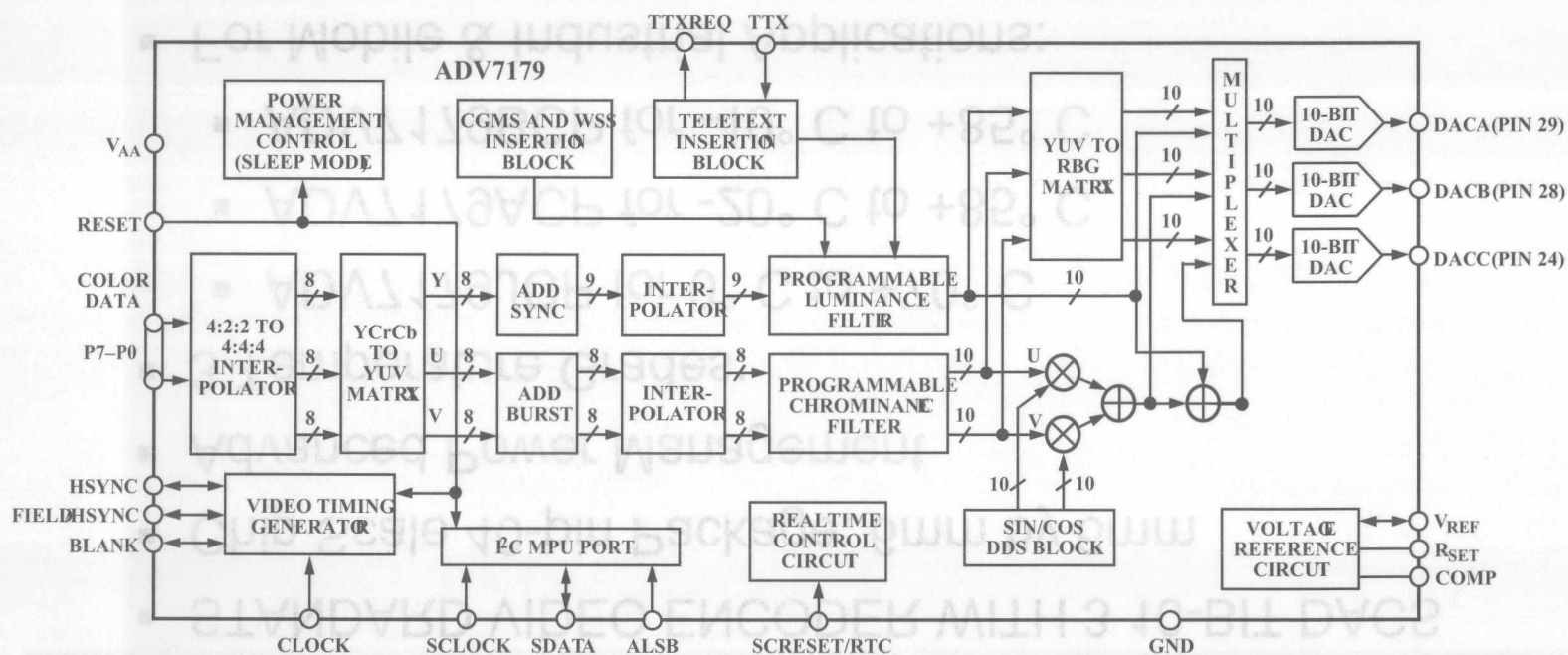
A Digital Video Encoder converts Digital Component Video Data (CCIR-601 4:2:2 for example) into a standard analog baseband television signal compatible with NTSC, PAL B/D/G/H/I, PAL M, or PAL N. In addition to the Composite output signal, there is often the facility to output S-VHS Y/C, RGB, or YUV Video.

- Direct Broadcast Satellite (DVB)
- Set-top boxes' integrated receiver decoders
- Anywhere a TV Connects with a Digital Source

Where are (Digital) Video Encoders Used?

- Anywhere a TV Connects with a Digital Source
 - Set-top boxes, integrated receiver decoders
 - Direct Broadcast Satellite (DVB)
 - Cable set-top box systems
 - Web browsers/internet boxes
 - PCs with TV tuners
 - Video CD, DVD, digital camcorder
 - Professional video
 - Multimedia PC

ADV7179/74 Chip Scale PAL/NTSC Video Encoder with Advanced Power Management



ADV7179/74 Chip Scale PAL/NTSC Video Encoder with Advanced Power Management

- STANDARD VIDEO ENCODER WITH 3 10-BIT DACS
- Chip Scale 40-pin Package: 6mm by 6mm
- Advanced Power Management
- 3 Temperature Grades:
 - ADV7179JCP for 0° C to +70° C
 - ADV7179ACP for -20° C to +85° C
 - ADV7179BCP for -40° C to +85° C
- For Mobile & Industrial Applications:
 - GSM mobile phones
 - Car Infotainment
 - PDA's & DSC's

ADV7179/74 Chip Scale PAL/NTSC Video Encoder with Advanced Power Management

- ITU-R² BT601/656 YCrCb to PAL/NTSC Video Encoder
- High Quality 10-Bit Video DACs
- SSAF (Super Sub-Alias Filter)
- Advanced Power Management Features CGMS (Copy Generation Management System) WSS (Wide Screen Signalling)
- Simultaneous Y,U,V,C Output Format
 - NTSC-M,PAL-M/N ,PAL-B/D/G/H/I,PAL-60
- Single 27 MHz Clock Required (x2 Oversampling)
- 80 dB Video SNR
- 32-Bit Direct Digital Synthesizer for Color Subcarrier
- Macrovision 7.1 (ADV7174 only)

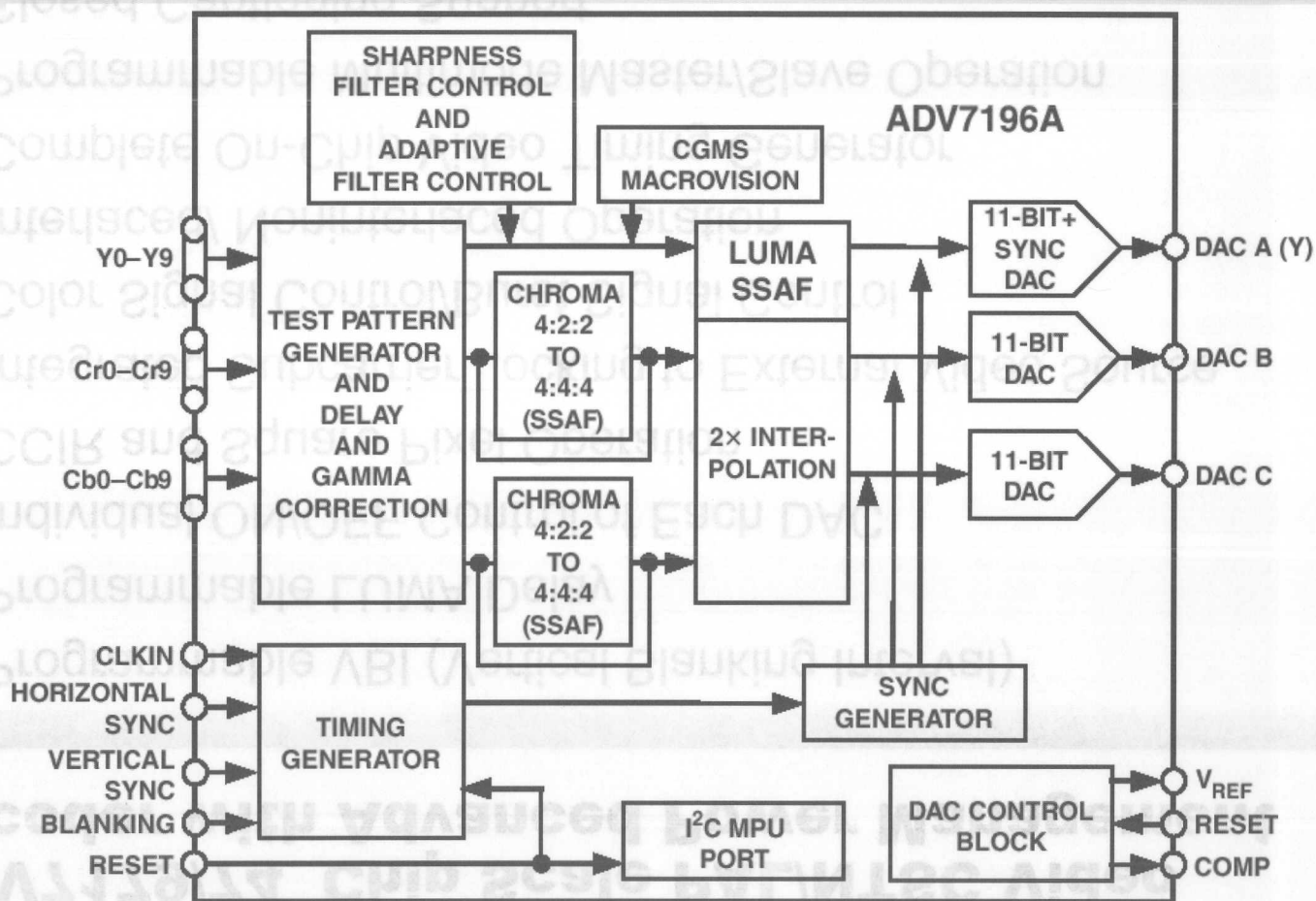
ADV7179/74 Chip Scale PAL/NTSC Video Encoder with Advanced Power Management

- Multistandard Video Output Support:
 - Composite (CVBS)
 - Component S-Video (Y/C)
- Video Input Data Port Supports:
 - CCIR-656 4:2:2 8-Bit Parallel Input Format
- Programmable Simultaneous Composite and S-Video or RGB (SCART)/YUV Video Outputs
- Programmable Luma Filters (Low-Pass [PAL/NTSC]) Notch, Extended (SSAF, CIF, and QCIF)
- Programmable Chroma Filters (Low-Pass [0.65 MHz, 1.0 MHz, 1.2 MHz and 2.0 MHz], CIF and QCIF)
- On-Board Color Bar Generation
- On-Board Voltage Reference
- Single Supply 3.3 V Operation
- Small 40-Lead 6 mm X 6 mm LFSCP Package

ADV7179/74 Chip Scale PAL/NTSC Video Encoder with Advanced Power Management

- Programmable VBI (Vertical Blanking Interval)
- Programmable LUMA Delay
- Individual ON/OFF Control of Each DAC
- CCIR and Square Pixel Operation
- Integrated Subcarrier Locking to External Video Source
- Color Signal Control/Burst Signal Control
- Interlaced/ Noninterlaced Operation
- Complete On-Chip Video Timing Generator
- Programmable Multimode Master/Slave Operation
- Closed Captioning Support
- Teletext Insertion Port (PAL-WST)
- 2-Wire Serial MPU Interface (I²C® -Compatible and Fast I²C)

ADV7196A HDTV Video Encoder Block Diagram



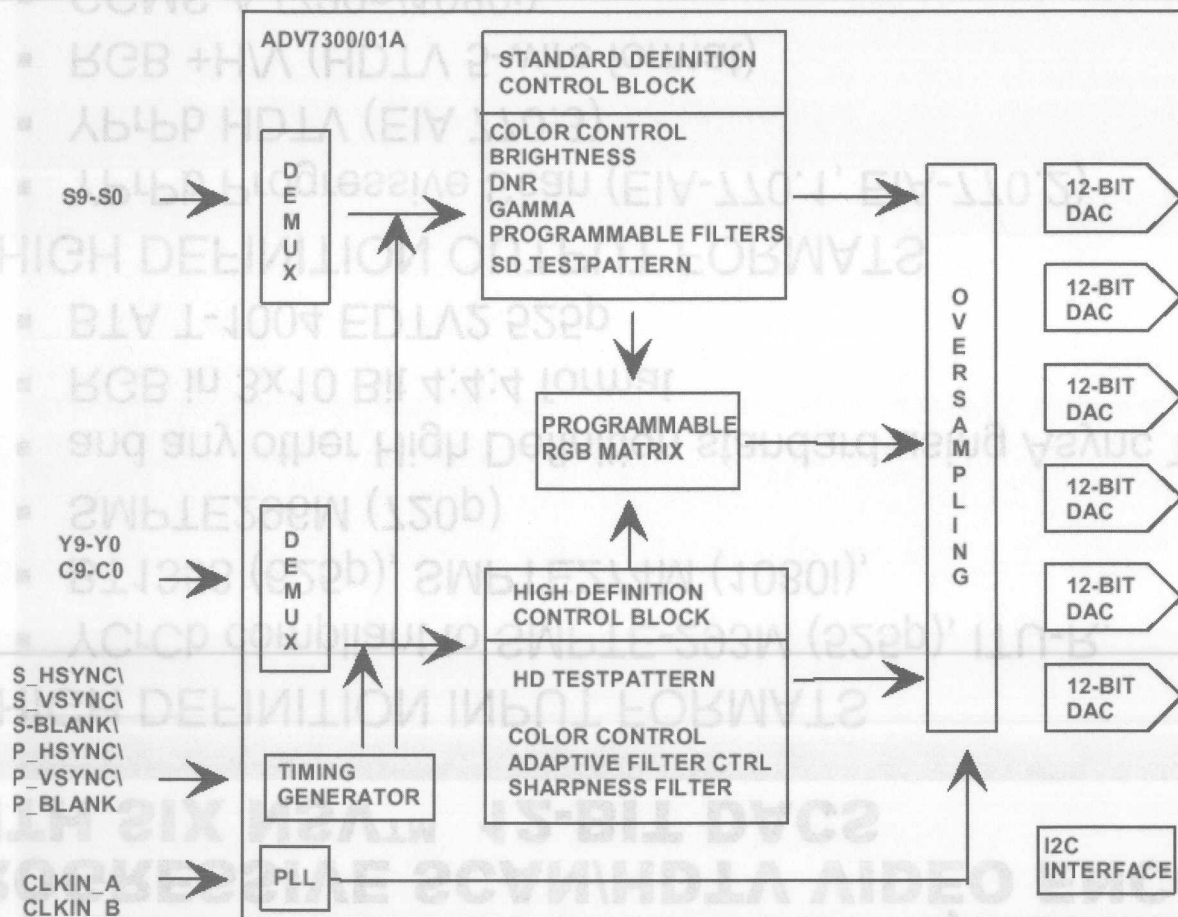
ADV7196A Multiformat Video Encoder (Progressive Scan/HDTV)

- Data Input Format
 - YCrCb in 1 x 10-bit (4:2:2) or 3 x 10-bit (4:4:4)
 - Compliant to SMPTE-293M (525p), ITU-R, BT1358 (625p), SMPTE274M (1080p), SMPTE296M (720p)
 - Any other HD standard using Async timing mode
 - RGB in 3 x 10-bit 4:4:4 format
- Output Formats
 - YPrPb progressive scan (EIA-770.1, EIA-770.2)
 - YPrPb HDTV (EIA-770.3)
 - RGB-compliant to RS-170 and RS-343A
- 2 x 11-Bit DACs for Color Components and [1 x 11-Bit + Sync] DAC for Y Component

ADV7196A Multiformat Video Encoder (Progressive Scan/HDTV)

- Internal Test Pattern Generator with Color Control
- Y/C Delay (\pm)
- Gamma Correction
- Sharpness Filter with Programmable Gain/Attenuation
- Programmable Adaptive Filter Control
- Undershoot Limiter
- Macrovision Rev.1.0 (525p)
- CGMS-A (525p)

ADV7300A/01A MULTI-FORMAT, STANDARD/PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 12-BIT DACS



ADV7300A/01A MULTI-FORMAT, STANDARD/PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 12-BIT DACS

- HIGH DEFINITION INPUT FORMATS
 - YCrCb compliant to SMPTE-293M (525p), ITU-R.
 - BT1358 (625p), SMPTE274M (1080i),
 - SMPTE296M (720p)
 - and any other High Definition standard using Async Timing Mode
 - RGB in 3x10 Bit 4:4:4 format
 - BTA T-1004 EDTV2 525p
- HIGH DEFINITION OUTPUT FORMATS
 - YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
 - YPrPb HDTV (EIA 770.3)
 - RGB +H/V (HDTV 5-wire format)
 - CGMS-A (720p/1080i)
 - Macrovision Rev1.0 (525p/625p) (ADV7300A only)
 - CGMS-A (525p)

ADV7300A/01A MULTI-FORMAT, STANDARD/ PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 12-BIT DACS

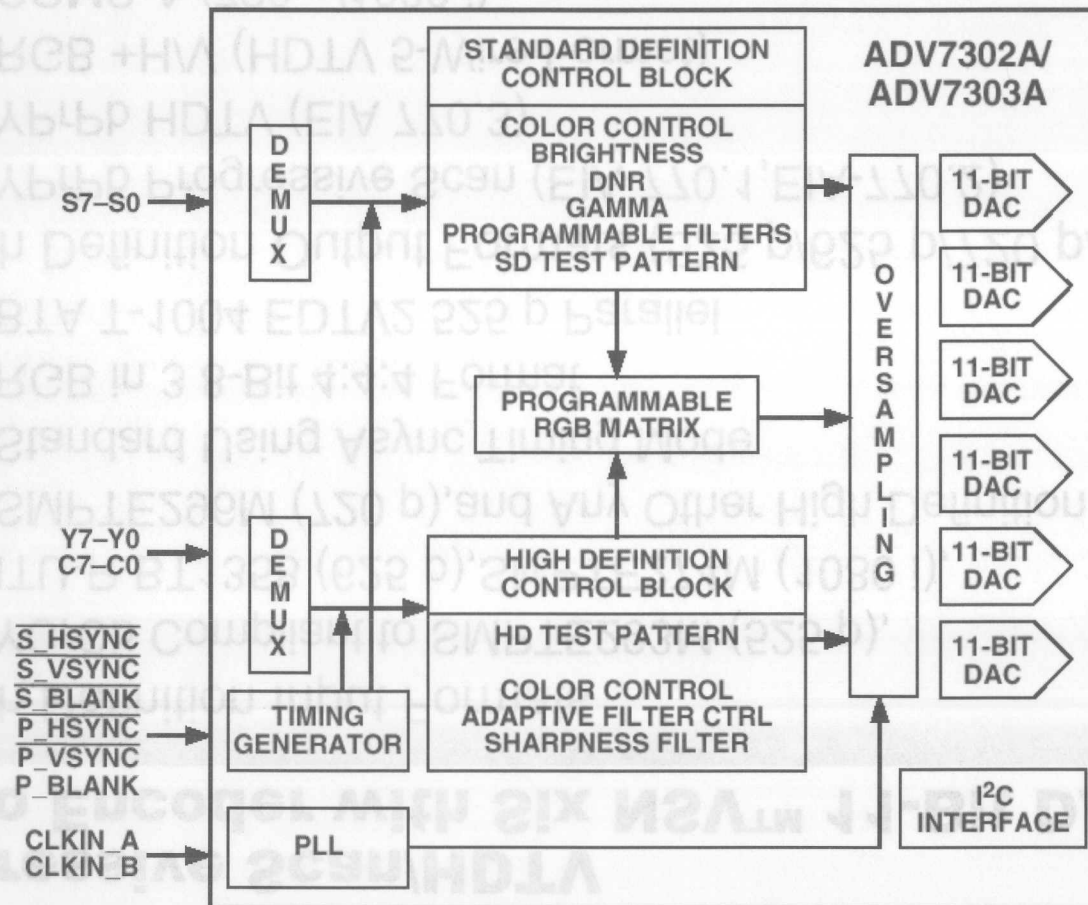
- STANDARD DEFINITION INPUT FORMATS
 - CCIR-656 4:2:2 8/10-bit Parallel Input
 - CCIR-601 4:2:2 16/20-bit Parallel Input
- STANDARD DEFINITION OUTPUT FORMATS
 - Composite NTSC M, N ;
 - Composite PAL M, N, B, D, G, H, I, PAL-60
 - SMPTE 170M NTSC compatible composite video
 - ITU-R BT.470 PAL compatible composite video
 - S-Video (Y/C)
 - EuroScart RGB
 - Component YUV (Betacam, MII, SMPTE/EBU N10)
 - Macrovision Rev 7.1 (ADV7300A only)
 - CGMS/WSS
 - Closed Captioning

ADV7300A/01A MULTI-FORMAT, STANDARD/ PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 12-BIT DACS

▪ GENERAL FEATURES

- Simultaneous SD & HD i/ps and o/ps
- Oversampling [108MHz/148.5MHz]
- On-board Voltage Reference
- Six 12-Bit Sigma-Delta DACs
- 2 Wire Serial MPU Interface
- Dual I/O Supply +2.5V/ +3.3 V Operation
- Analog & Digital Supply +2.5V
- On-board PLL
- 64-LQFP package
- Pb free product

ADV7302A/03A Multiformat Standard/ Progressive Scan/HDTV Video Encoder with Six NSV™ 11-Bit DACs



ADV7302A/03A Multiformat Standard/ Progressive Scan/HDTV Video Encoder with Six NSV™ 11-Bit DACs

- High Definition Input Formats
 - YCrCb Compliant to SMPTE293M (525 p),
 - ITU-R.BT1358 (625 p), SMPTE274M (1080 i),
 - SMPTE296M (720 p), and Any Other High Definition
 - Standard Using Async Timing Mode
 - RGB in 3 8-Bit 4:4:4 Format
 - BTA T-1004 EDTV2 525 p Parallel
- High Definition Output Formats (525 p/625 p/720 p/1080 i)
 - YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
 - YPrPb HDTV (EIA 770.3)
 - RGB +H/V (HDTV 5-Wire Format)
 - CGMS-A (720 p/1080 i)
 - Macrovision Rev 1.0 (525 p/625 p)1
 - CGMS-A (525 p)

ADV7302A/03A Multiformat Standard/ Progressive Scan/HDTV Video Encoder with Six NSV™ 11-Bit DACs

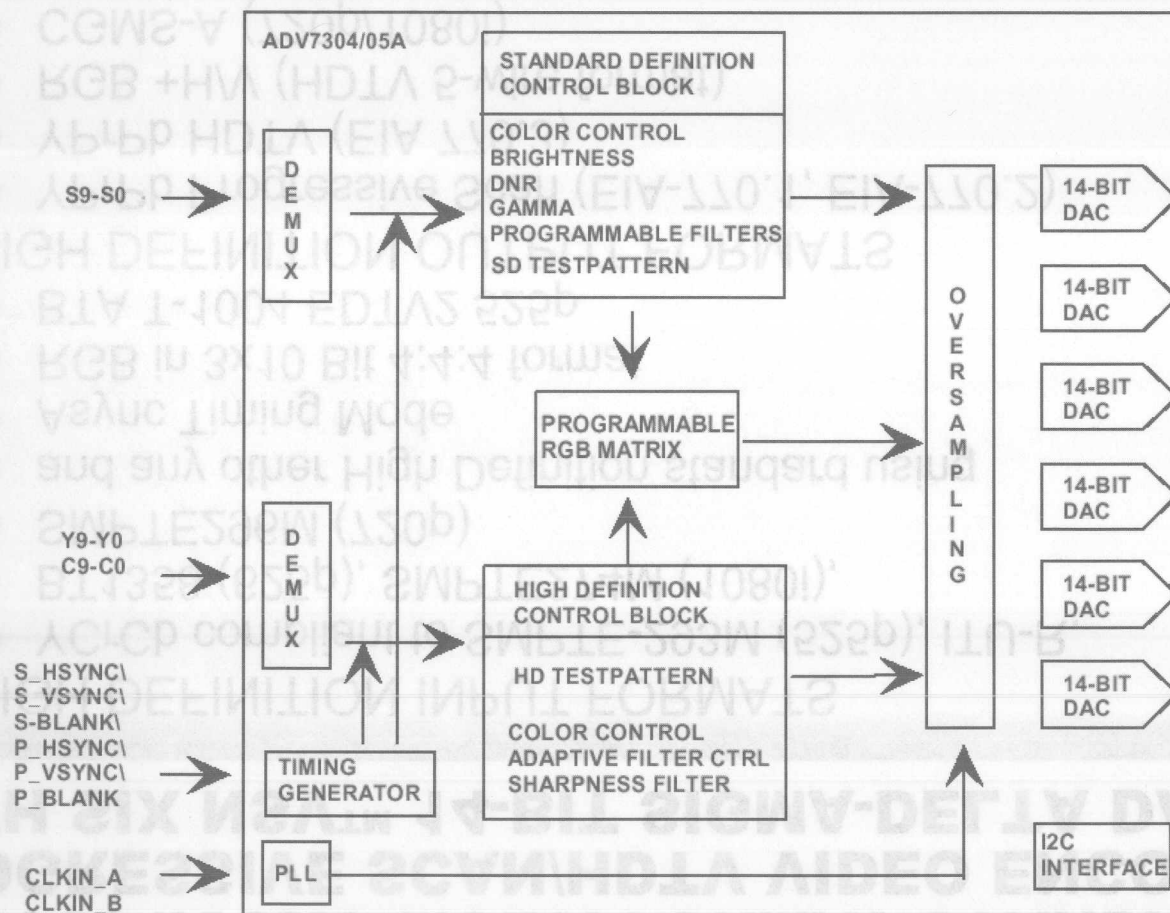
- Standard Definition Input Formats
 - CCIR-656 4:2:2 8-Bit Parallel Input
 - CCIR-601 4:2:2 16-Bit Parallel Input
- Standard Definition Output Formats
 - Composite NTSC M,N;
 - PAL M,N,B,D,G,H,I,PAL-60
 - SMPTE170M NTSC-Compatible Composite Video
 - ITU-R.BT470 PAL-Compatible Composite Video
 - S-Video (Y/C)
 - EuroScart RGB
 - Component YUV (Betacam,MII,SMPTE/EBU N10)
 - Macrovision Rev 7.1 1
 - CGMS/WSS
 - Closed Captioning

ADV7302A/03A Multiformat Standard/ Progressive Scan/HDTV Video Encoder with Six NSV™ 11-Bit DACs

■ GENERAL FEATURES

- Simultaneous SD and HD Inputs and Outputs
- Oversampling (108 MHz/148.5 MHz)
- On-Board Voltage Reference
- Six NSV Precision Video 11-Bit DACs
- 2-Wire Serial MPU Interface
- Dual I/O Supply 2.5 V/3.3 V Operation
- Analog and Digital Supply 2.5 V
- On-Board PLL
- 64-LQFP Package
- Lead-Free Product

ADV7304A/05A MULTI-FORMAT STANDARD/PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 14-BIT SIGMA-DELTA DACS



ADV7304A/05A MULTI-FORMAT STANDARD/ PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 14-BIT SIGMA-DELTA DACS

- HIGH DEFINITION INPUT FORMATS
 - YCrCb compliant to SMPTE-293M (525p), ITU-R.
 - BT1358 (625p), SMPTE274M (1080i),
 - SMPTE296M (720p)
 - and any other High Definition standard using
 - Async Timing Mode
 - RGB in 3x10 Bit 4:4:4 format
 - BTA T-1004 EDTV2 525p
- HIGH DEFINITION OUTPUT FORMATS
 - YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
 - YPrPb HDTV (EIA 770.3)
 - RGB +H/V (HDTV 5-wire format)
 - CGMS-A (720p/1080i)
 - Macrovision Rev1.0 (525p/625p) (ADV7304A only)
 - CGMS-A (525p)

ADV7304A/05A MULTI-FORMAT STANDARD/ PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 14-BIT SIGMA-DELTA DACS

▪ STANDARD DEFINITION INPUT FORMATS

- CCIR-656 4:2:2 8/10-bit Parallel Input
- CCIR-601 4:2:2 16/20-bit Parallel Input

▪ STANDARD DEFINITION OUTPUT FORMATS

- Composite NTSC M, N ;
- Composite PAL M, N, B, D, G, H, I, PAL-60
- SMPTE 170M NTSC compatible composite video
- ITU-R BT.470 PAL compatible composite video
- S-Video (Y/C)
- EuroScart RGB
- Component YUV (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1 (ADV7304A only)
- CGMS/WSS
- Closed Captioning

ADV7304A/05A MULTI-FORMAT STANDARD/ PROGRESSIVE SCAN/HDTV VIDEO ENCODER WITH SIX NSV™ 14-BIT SIGMA-DELTA DACS

■ GENERAL FEATURES

- Simultaneous SD & HD i/ps and o/ps
- Oversampling [108MHz/148.5MHz]
- On-board Voltage Reference
- Six 14-Bit Sigma-Delta DACs
- 2 Wire Serial MPU Interface
- Dual I/O Supply +2.5V/ +3.3 V Operation
- Analog & Digital Supply +2.5V
- On-board PLL
- 64-LQFP package
- Pb free product

Digital Video Codecs

and from the Analog and Digital video signal domains.
(SD-A/D, 24 MHz) plus Video DACs for conversion to
A Digital Video Codec comprises a video rate digitizer

What Are Digital Video Codecs?

What Are Digital Video Codecs?

A Digital Video Codec comprises a video rate digitizer (12-bit ADC, 54 MHz) plus Video DACs for conversion to and from the Analog and Digital video signal domains.

Digital Video Codecs

Where are Video Codecs Used?

- Highly Integrated Front and Back End Analog Solutions
 - Digital Personal Video Recorders (PVRs)
 - Digital TVs
 - Picture-in-Picture video systems
 - Cable and satellite Set-Top Boxes (STBs)
 - I and Q demodulation
 - QAM/QPSK
 - Professional video
 - Direct IF conversion

ADV7202 Video Codec

The ADV7202 supports up to six CVBS, four S-Video(YC), and two YUV inputs, digitized at up to 54 MHz with 12-bit resolution (2-bits used for gain and offset adjustment).

Four high-performance 10-bit video DACs provide support for CVBS, S-Video, YUV, and RGB output formats.

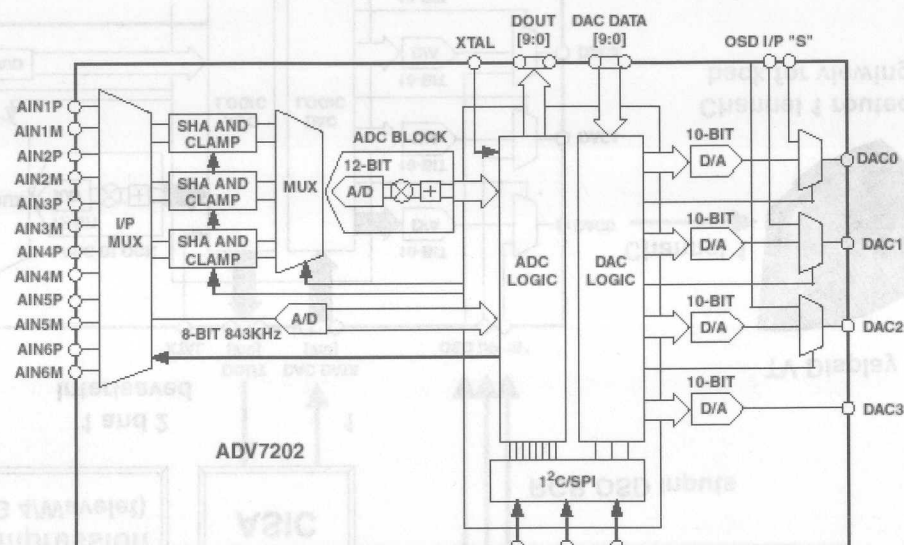
An additional 8-bit 843 kHz A/D converter allows sampling of up to eight additional auxiliary inputs for system monitoring, etc.

Picture-in-Picture functionality is also supported through the internal three-input mux which also muxes to the output DACs.

ADV7202 Functional Block Diagram

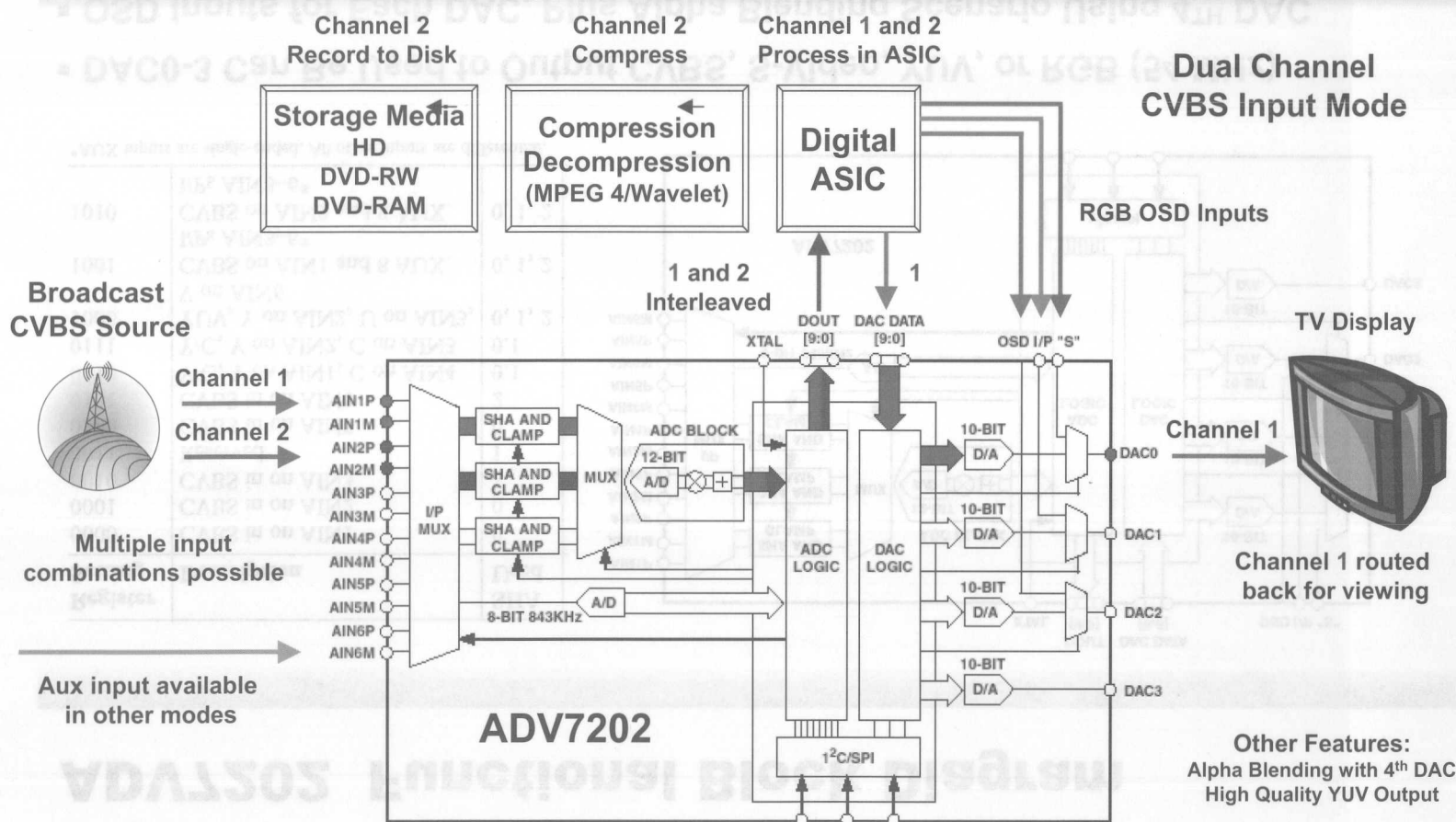
Register Setting	Description	SHA Used
0000	CVBS in on AIN1	0
0001	CVBS in on AIN2	0
0010	CVBS in on AIN3	1
0011	Reserved	1
0100	CVBS in on AIN5	0
0101	CVBS in on AIN6	2
0110	Y/C, Y on AIN1, C on AIN4	0.1
0111	Y/C, Y on AIN2, C on AIN3	0.1
1000	YUV, Y on AIN2, U on AIN3, V on AIN6	0, 1, 2
1001	CVBS on AIN1 and 8 AUX. I/Ps AIN3-6*	0, 1, 2
1010	CVBS on AIN2 and 8 AUX. I/Ps AIN3-6*	0, 1, 2

*AUX inputs are single-ended. All other inputs are differential.



- DAC0-3 Can Be Used to Output CVBS, S-Video, YUV, or RGB (54 MHz)
- OSD Inputs for Each DAC, Plus Alpha Blending Scenario Using 4TH DAC
- Dual CVBS Input and Output Possible
- 8-Bit 843 kHz ADC for System Monitoring Purposes (e.g., Temperature Sensing)

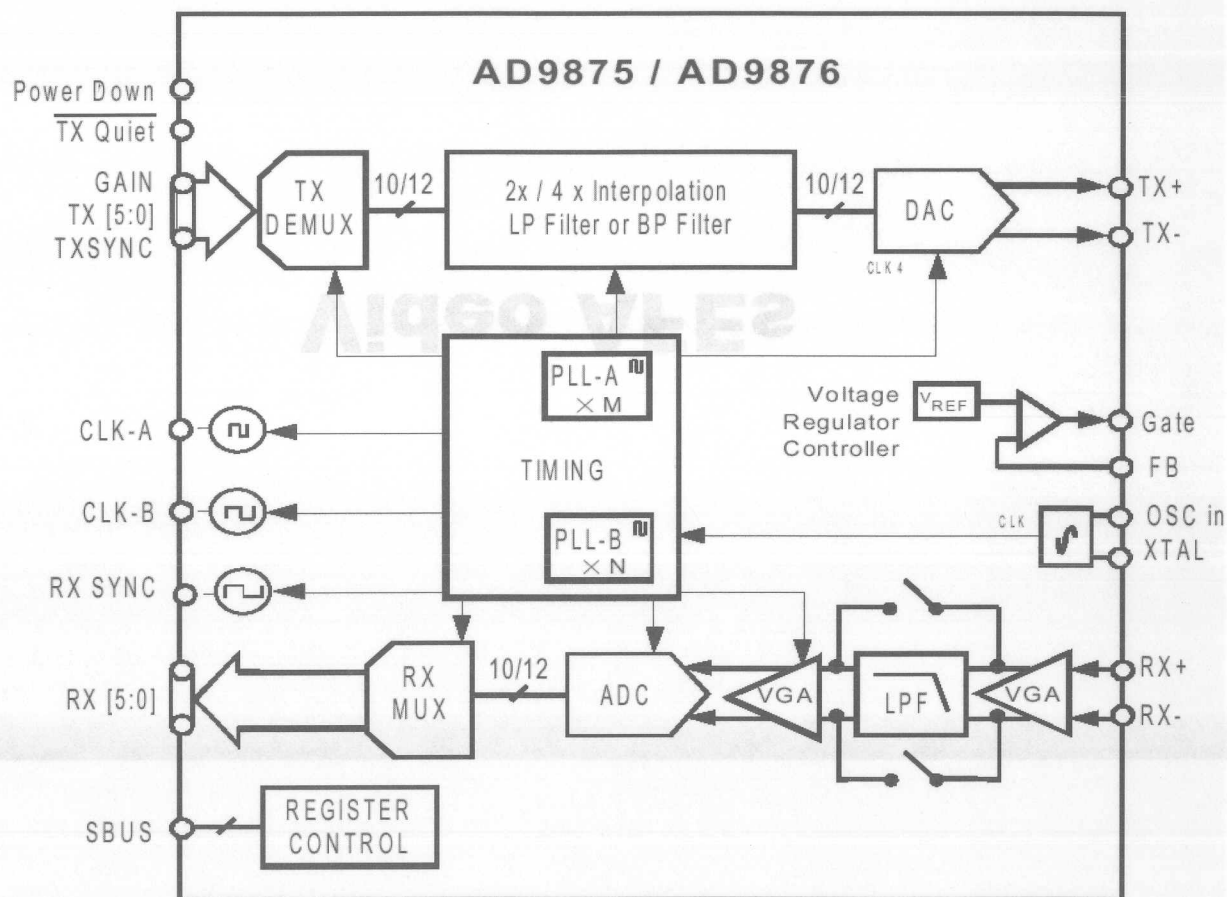
ADV7202 Suggested Application: Highly Integrated PVR





7-41

AD9875/76 Mixed-Signal Front Ends (MxFE™)



AD9875/76 Mixed-Signal Front End (MxFE™)

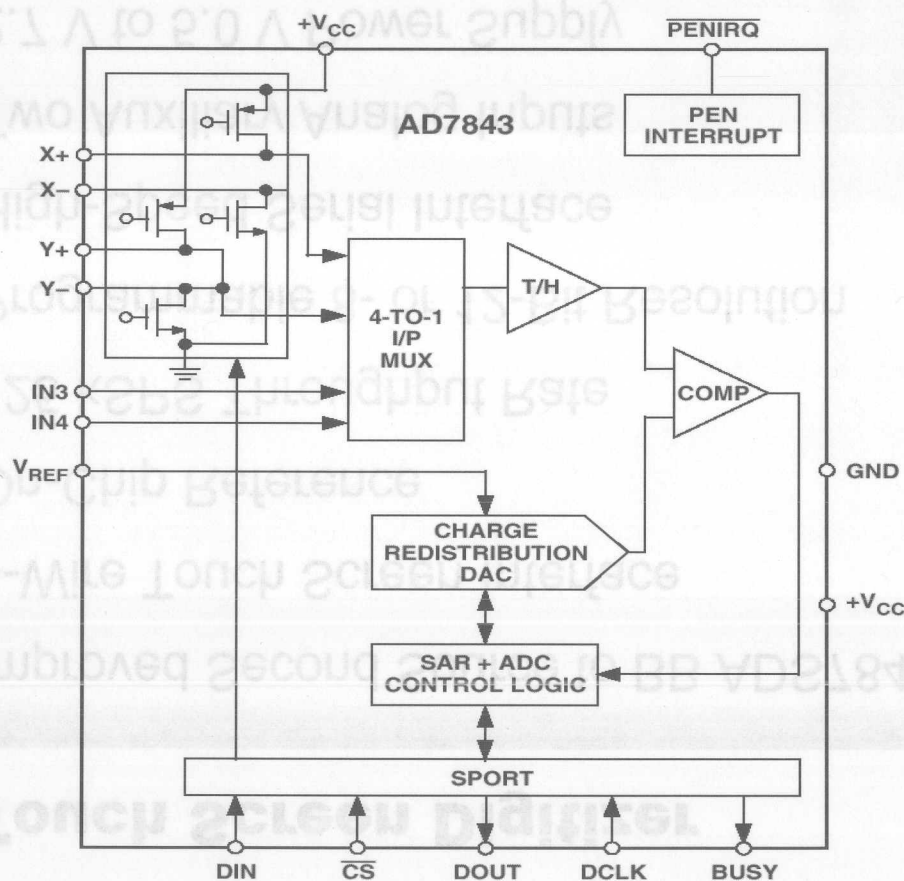
- AD9875: 10-Bit 50 MSPS ADC and 128 MSPS DAC
- AD9876: 12-Bit 50 MSPS ADC and 128 MSPS DAC
- 64 MSPS/32 MSPS Input Word Rate
- 2x/4x Interpolation LP or BP Transmit Filter
- 26 MHz Transmit Bandwidth
- 4TH Order 12 MHz or 29 MHz Low-Pass Filter (with Bypass)
- -6 dB to +36 dB PGA on Receive Channel
- Internal 4x Clock Multiplier PLL
- Power-Down Mode

- Power-Down Mode
- Internal 4x Clock Multiplier PLL
- -6 dB to +36 dB PGA on Receive Channel (with Bypass)
- 4th Order 15 MHz or 58 MHz Low-Pass Filter
- 58 MHz 15-Bit 1/2-Bandwidth
- 5x/4x Interpolation LP or BP Transmit Filter
- 64 MSPS/35 MSPS Input Word Rate
- AD9878: 15-Bit 50 MSPS ADC and 158 MSPS DAC
- AD9875: 10-Bit 50 MSPS ADC and 158 MSPS DAC

Touch Screen Digitizers

AD9875/78 Mixed-Signal Front End (MXFE™)

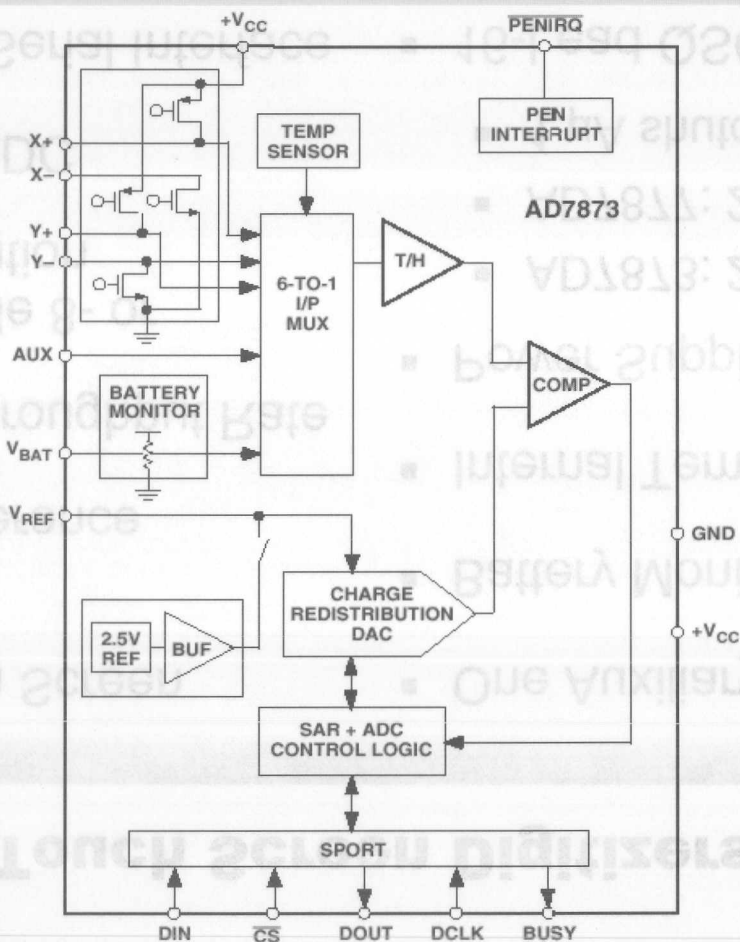
AD7843 Touch Screen Digitizer



AD7843 Touch Screen Digitizer

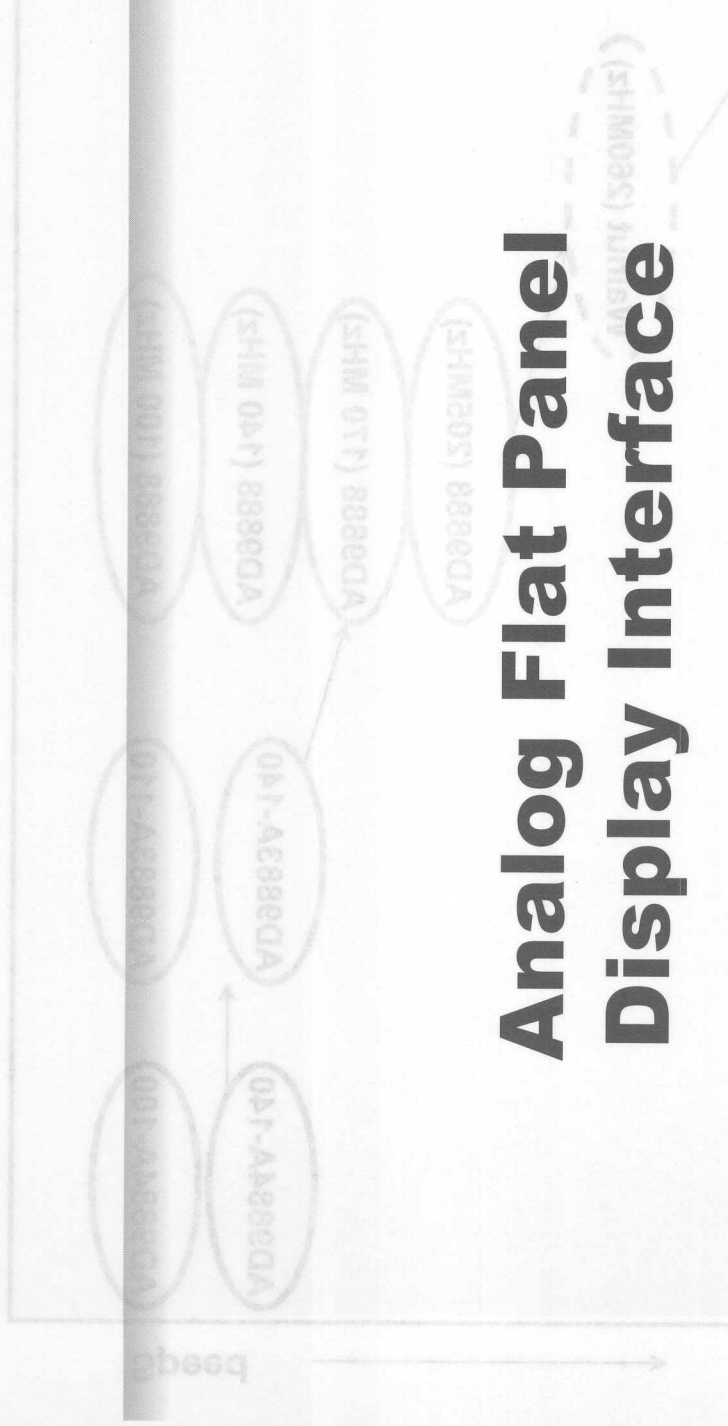
- Improved Second Source to BB ADS7843
- 4-Wire Touch Screen Interface
- On-Chip Reference
- 125 kSPS Throughput Rate
- Programmable 8- or 12-Bit Resolution
- High-Speed Serial Interface
- Two Auxiliary Analog Inputs
- 2.7 V to 5.0 V Power Supply
- 1 μ A Shutdown Current
- 16-Lead QSOP Package

AD7873/77 Touch Screen Digitizers



AD7873/77 Touch Screen Digitizers

- 4-Wire Touch Screen Interface
- On-Chip Reference
- 125 kSPS Throughput Rate
- Programmable 8- or 12-Bit Resolution
- 12-Bit SAR ADC
- High-Speed Serial Interface
- One Auxiliary Analog Input
- Battery Monitor Input
- Internal Temperature Sensor
- Power Supplies:
 - AD7873: 2.70 V to 5.25 V
 - AD7877: 2.35 V to 2.65 V
 - 1 μ A shutdown current
- 16-Lead QSOP Package

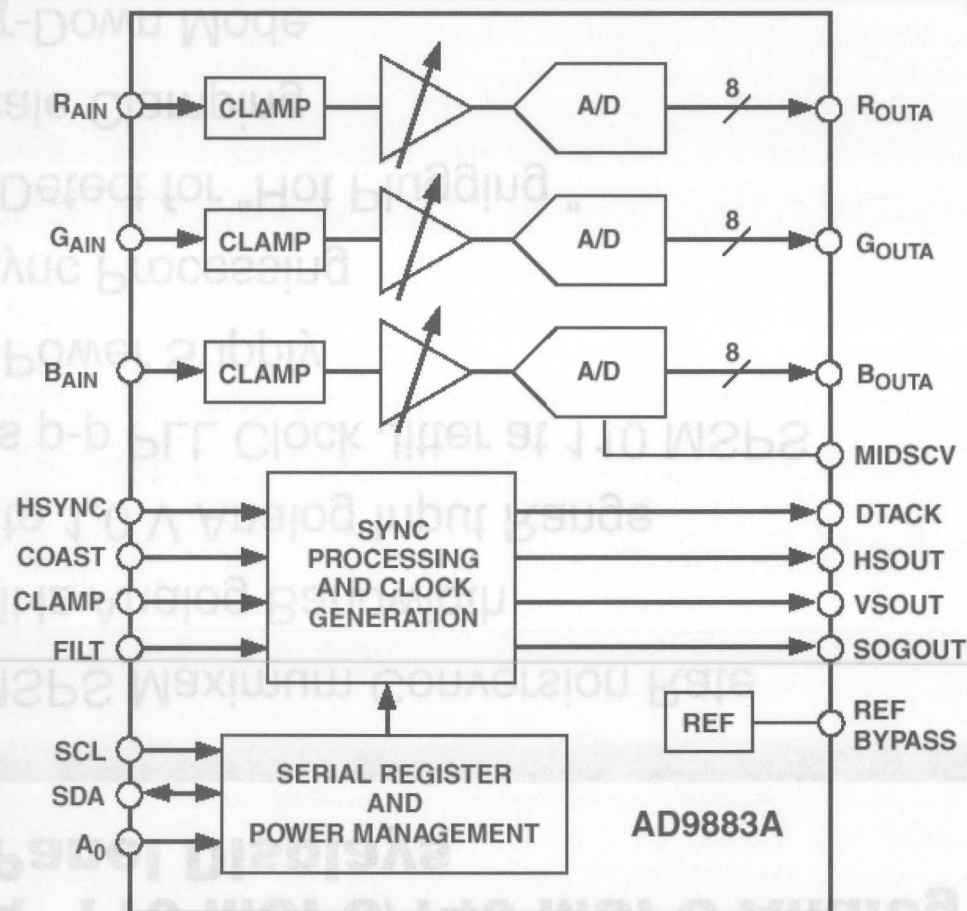


Analog Flat Panel Display Interface

Display Electronics Analog Interface Product Roadmap



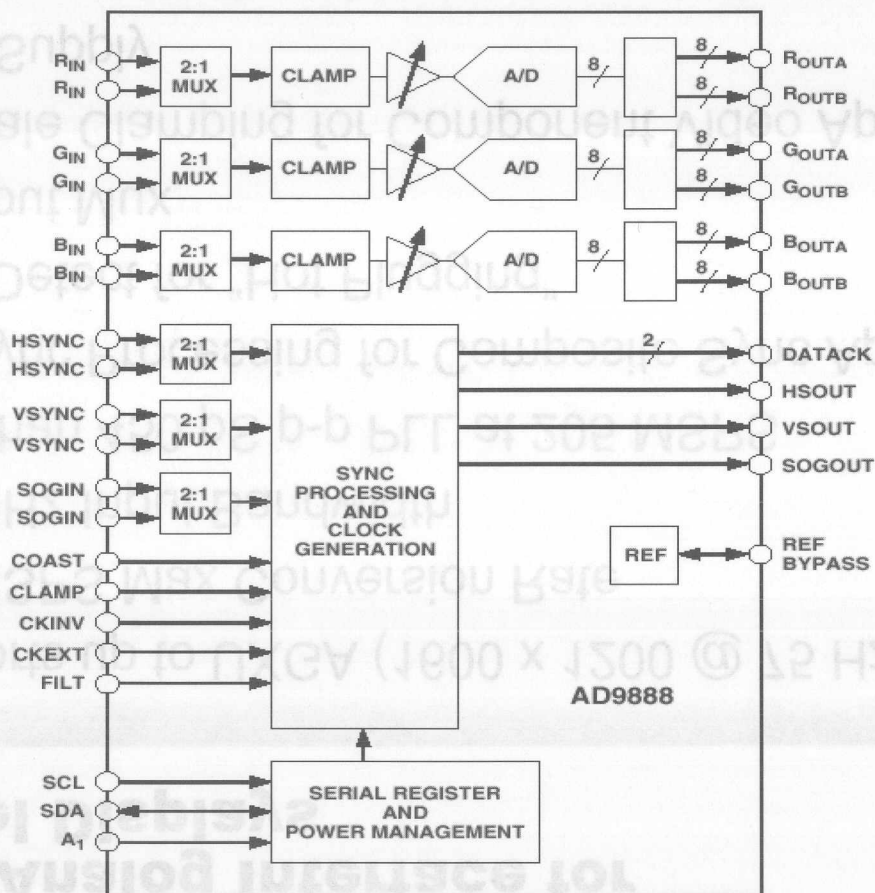
AD9883A 110 MSPS/140 MSPS Analog Interface for Flat Panel Displays



AD9883A 110 MSPS/140 MSPS Analog Interface for Flat Panel Displays

- 140 MSPS Maximum Conversion Rate
- 300 MHz Analog Bandwidth
- 0.5 V to 1.0 V Analog Input Range
- 500 ps p-p PLL Clock Jitter at 110 MSPS
- 3.3 V Power Supply
- Full Sync Processing
- Sync Detect for "Hot Plugging"
- Midscale Clamping
- Power-Down Mode
- Low Power: 500 mW Typical
- 4:2:2 Output Format Mode

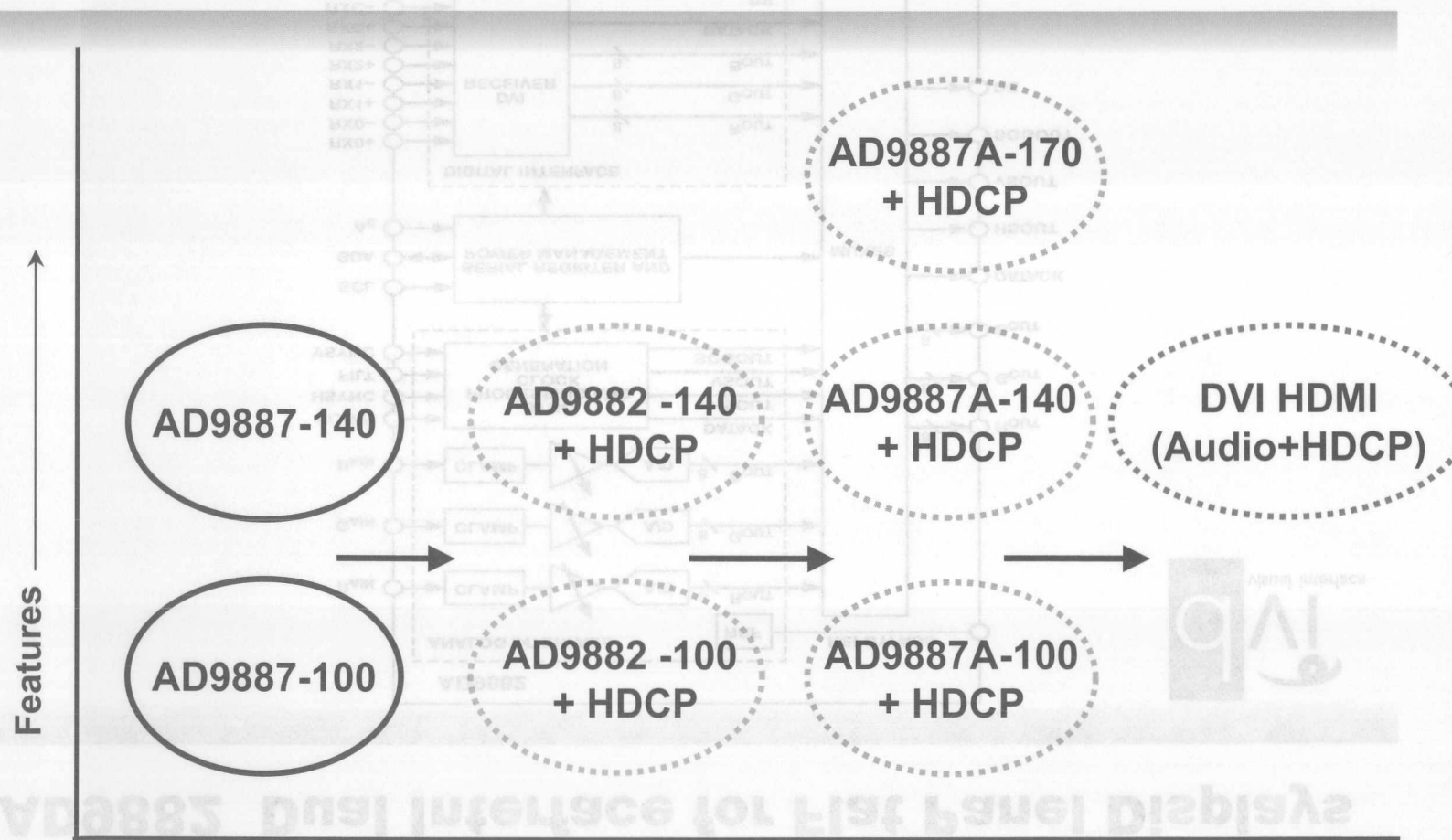
AD9888 Analog Interface for Flat Panel Displays



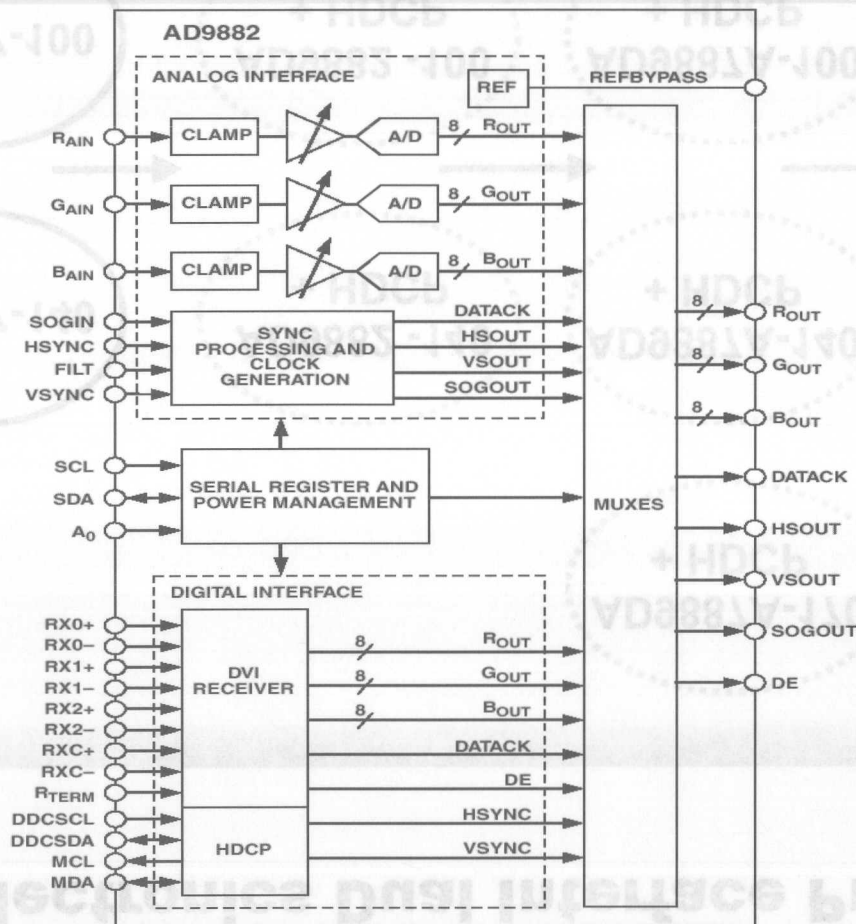
AD9888 Analog Interface for Flat Panel Displays

- Supports up to UXGA (1600 x 1200 @ 75 Hz)
- 205 MSPS Max Conversion Rate
- 500 MHz Input Bandwidth
- Less than 450 pS p-p PLL at 205 MSPS
- Full Sync Processing for Composite Sync Applications
- Sync Detect for “Hot Plugging”
- 2:1 Input Mux
- Midscale Clamping for Component Video Applications
- 3.3 V Supply
- Less than 1 W (Typ) Dissipation at 205 MSPS
- Power-Down Mode

Display Electronics Dual Interface Product Roadmap

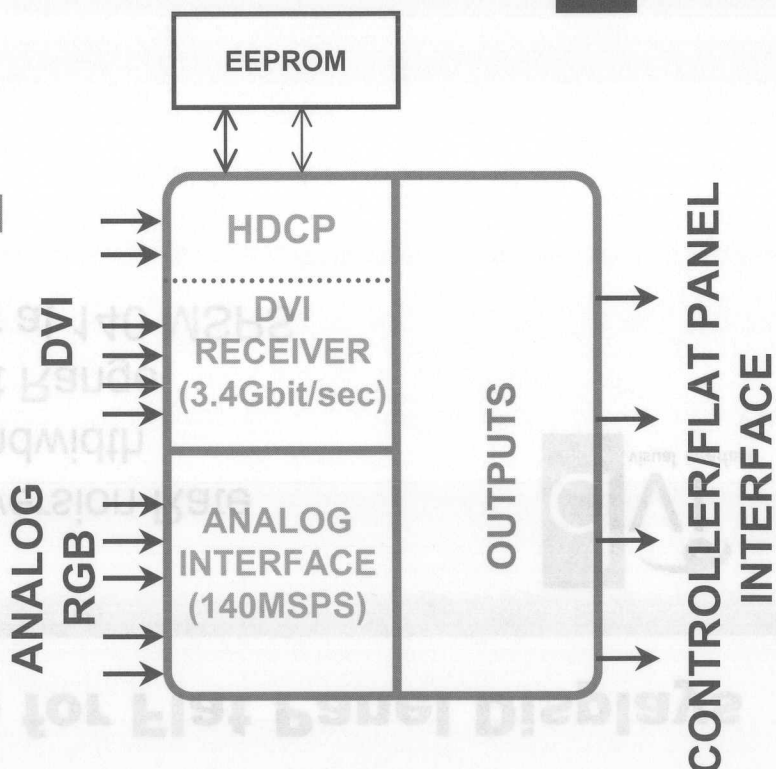


AD9882 Dual Interface for Flat Panel Displays



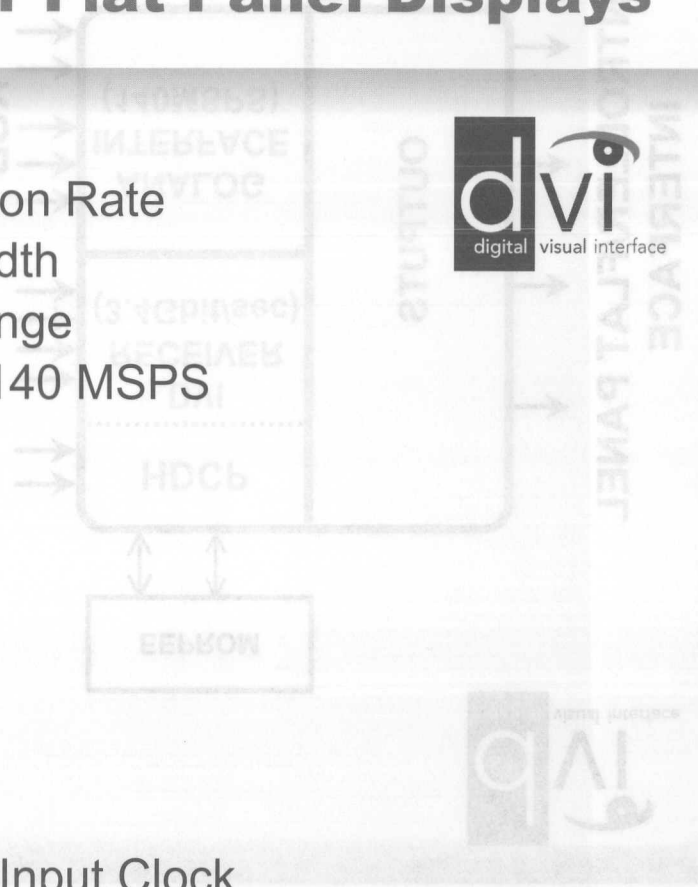
AD9882 Dual Interface for Flat Panel Displays

- 100/140 MSPS (XGA/SXGA)
- Targeted for low-cost XGA & SXGA displays
- Includes High-bandwidth Digital Content Protection (HDCP)
- Mid-scale clamp for YUV
- Full Sync processing
- 4:2:2 output formatting
- 100-pin LQFP (14x14mm)

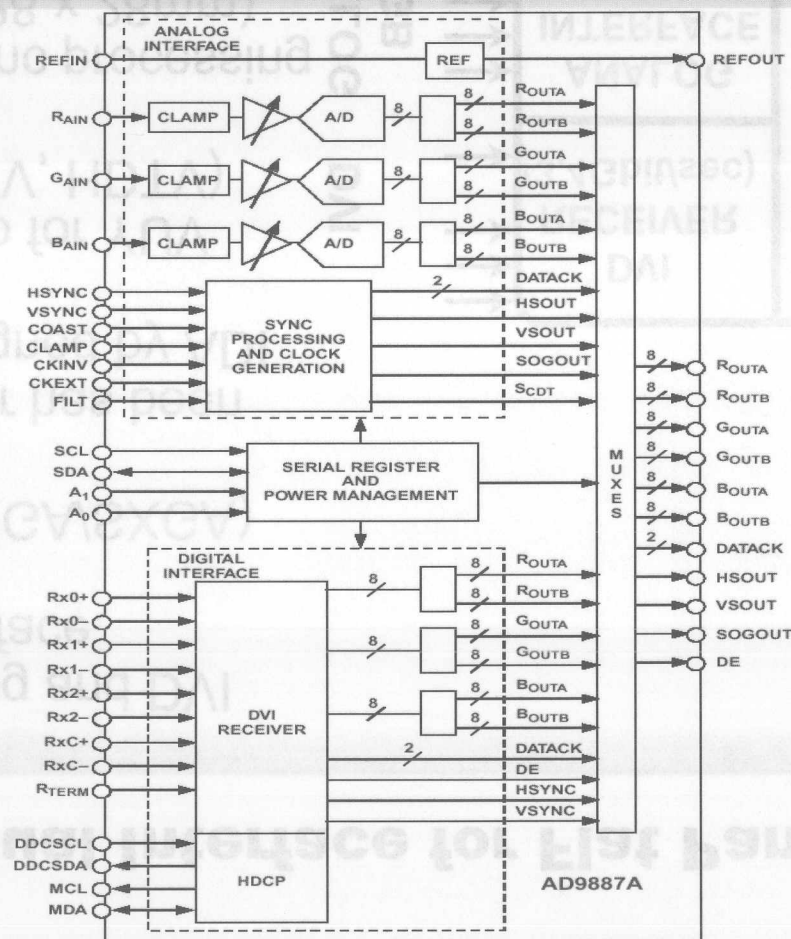


AD9882 Dual Interface for Flat Panel Displays

- Analog Interface
 - 140 MSPS Maximum Conversion Rate
 - Programmable Analog Bandwidth
 - 0.5 V to 1.0 V Analog Input Range
 - 500 pSp-p PLL Clock Jitter at 140 MSPS
 - 3.3 V Power Supply
 - Full Sync Processing
 - Midscale Clamping
 - 4:2:2 Output Format Mode
- Digital Interface
 - DVI 1.0 Compatible Interface
 - 112 MHz Operation
 - High Skew Tolerance of 1 Full Input Clock
 - Sync Detect for "Hot Plugging"
 - Supports High-Bandwidth Digital Content Protection



AD9887A Dual Interface for Flat Panel Displays



AD9887A Dual Interface for Flat Panel Displays

Integrated analog and DVI compatible interface.

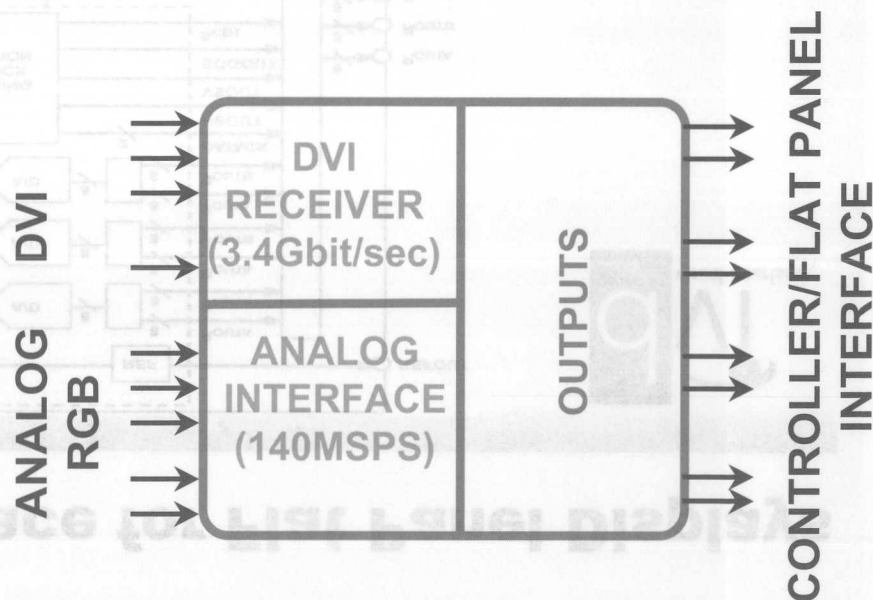
100/140 MHz (XGA/SXGA)

The DVI receiver has been completely designed by ADI

Mid-scale Clamp for YUV applications (DTV, HDTV)

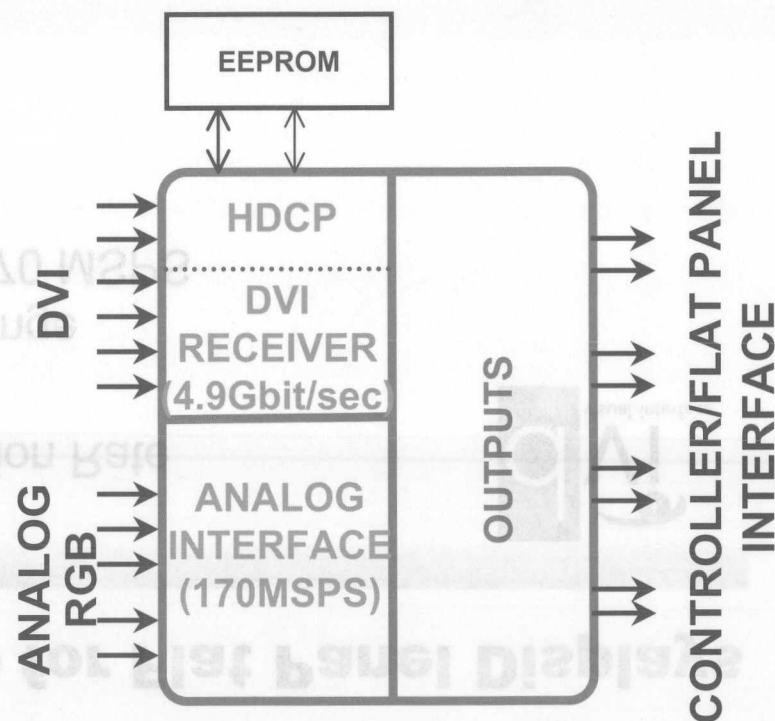
Includes Full Sync processing
160-pin LQFP (28 x 28mm)

AD9887 Currently in high volume production



AD9887A Dual Interface for Flat Panel Displays

- Pin-to-pin and software compatible with the AD9887
- 100/140/170 MHz (XGA/SXGA/UXGA) operation for both interfaces
- Includes High-bandwidth Digital Content Protection (HDCP)
- Mid-scale Clamp for YUV applications (DTV, HDTV)
- Includes Full Sync processing
- 160-pin LQFP (28 x 28mm)



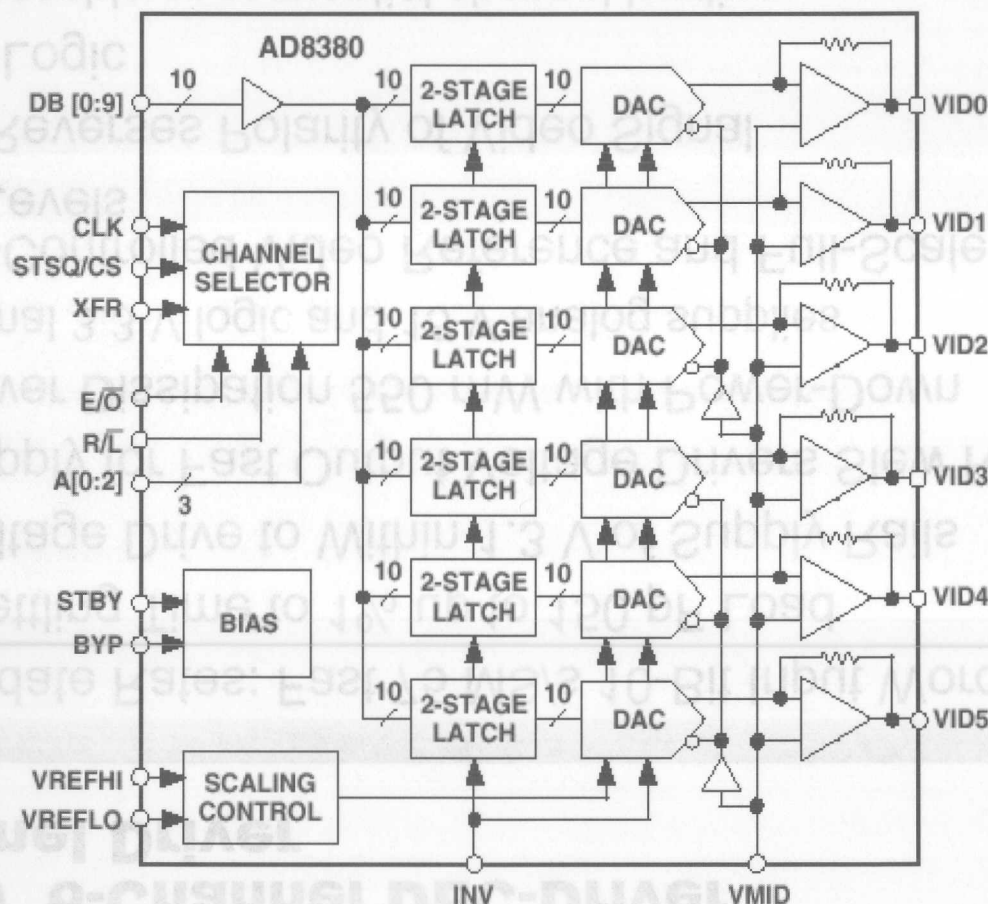
AD9887A Dual Interface for Flat Panel Displays



- Analog Interface
 - 170 MSPS Maximum Conversion Rate
 - 330 MHz Analog Bandwidth
 - 0.5 V to 1.0 V Analog Input Range
 - 500 pSp-p PLL clock jitter at 170 MSPS
 - 3.3 V power supply
 - Full sync processing
 - Midscale Clamping
 - 4:2:2 Output Format Mode
- Digital (DVI Compliant) Interface
 - 170 MHz operation (2 pixels/clock mode)
 - High skew tolerance of 1 full input clock
 - Sync Detect for “Hot plug in”
 - Supports High-Bandwidth Digital Protection



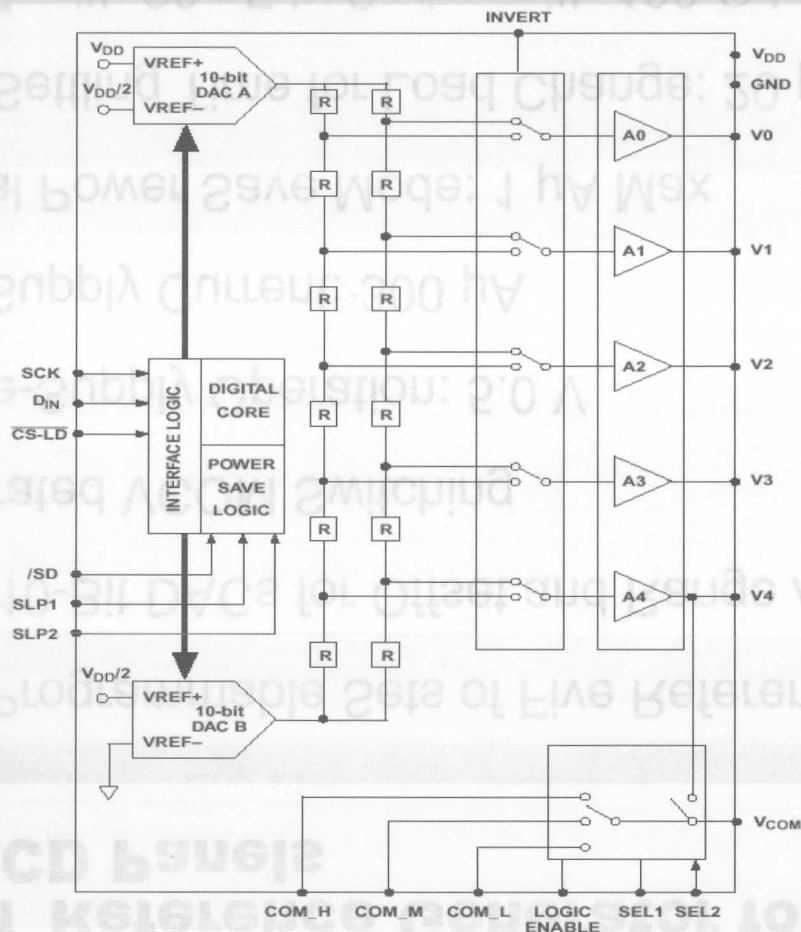
AD8380 6-Channel DEC-Driver LCD Panel Driver



AD8380 6-Channel DEC-Driver LCD Panel Driver

- High Update Rates: Fast 75 MS/s 10-Bit Input Word Rate
- 26 ns Settling Time to 1% up to 150 pF Load
- High-Voltage Drive to Within 1.3 V of Supply Rails
- 24 V Supply for Fast Output Voltage Drivers Slew Rate 270 V/ μ s
- Low Power Dissipation 550 mW with Power-Down
 - Nominal 3.3 V logic and 15 V analog supplies
- Voltage-Controlled Video Reference and Full-Scale (Contrast) Output Levels
- INV Bit Reverses Polarity of Video Signal
- Flexible Logic
 - Addressable or sequential channel loading
 - STSQ/CS allows parallel AD8380 operation for XGA and greater resolution

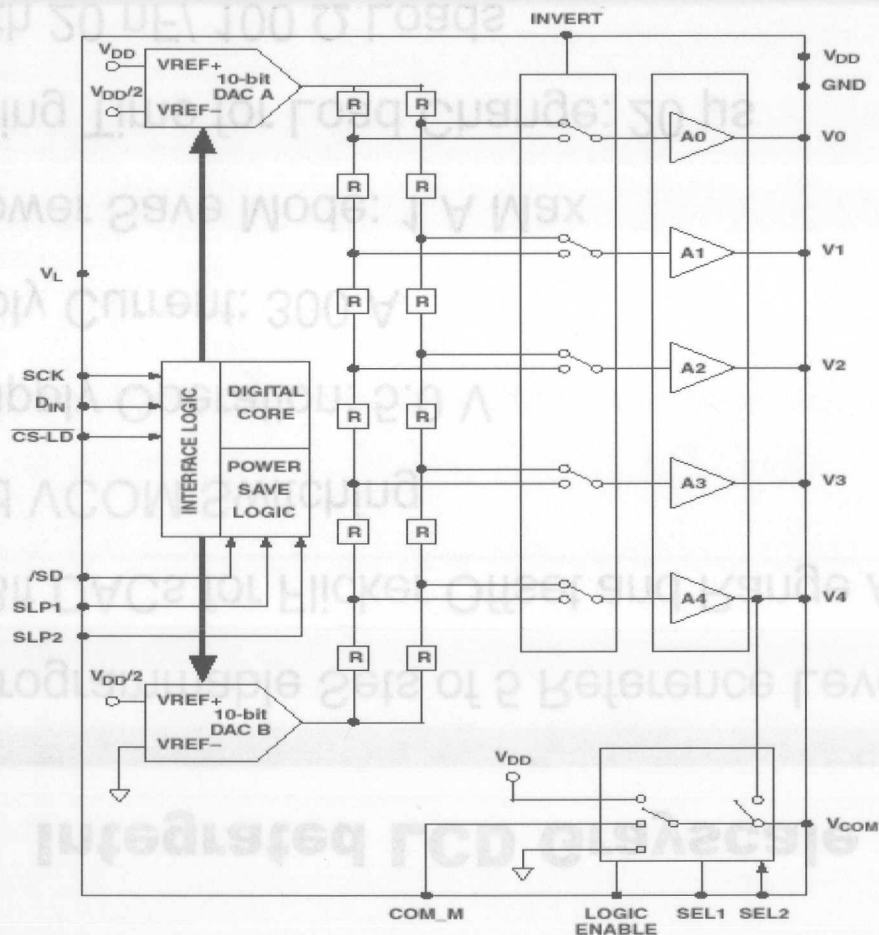
ADD8501 Reference Generator for Mobile LCD Panels



ADD8501 Reference Generator for Mobile LCD Panels

- Two Programmable Sets of Five Reference Levels
- Dual 10-Bit DACs for Offset and Range Adjustment
- Integrated VCOM Switching
- Single-Supply Operation: 5.0 V
- Low Supply Current: 300 μ A
- Global Power Save Mode: 1 μ A Max
- Fast Settling Time for Load Change: 20 μ s
- Stable with 20 nF in Series with 100 Ω Loads
- CMOS/TTL Input Levels

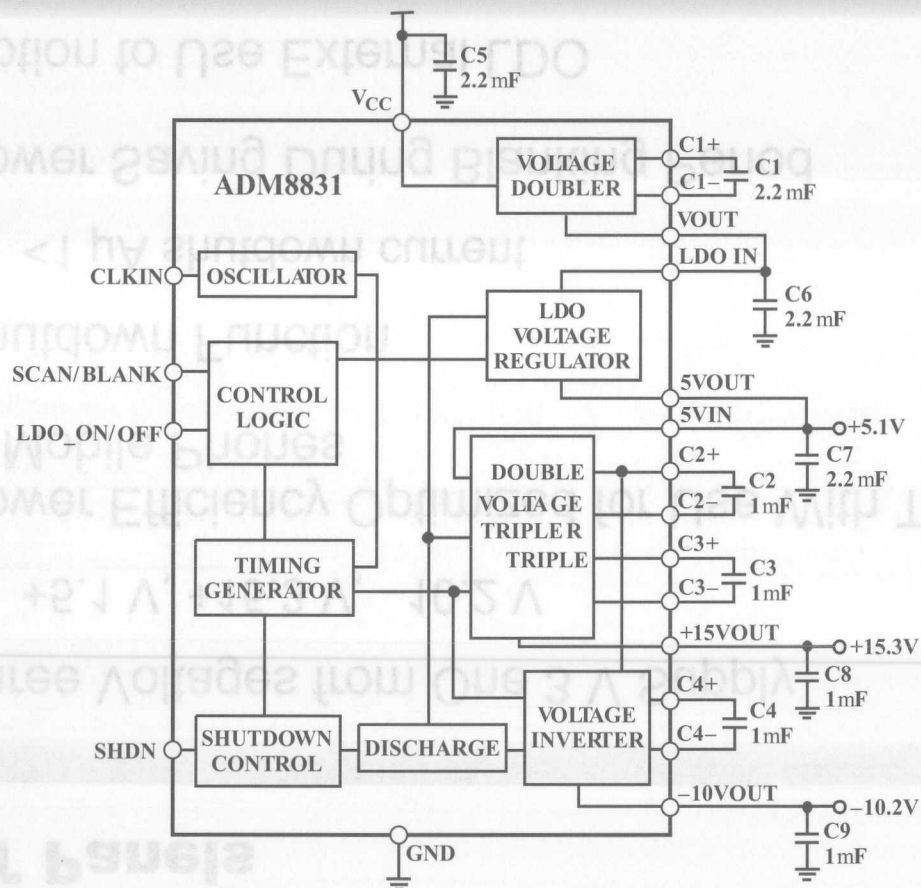
ADD8502 Integrated LCD Grayscale Generator



ADD8502 Integrated LCD Grayscale Generator

- 2 Mask Programmable Sets of 5 Reference Levels
- Dual 10-Bit DACs for Flicker Offset and Range Adjustment
- Integrated VCOM Switching
- Single-Supply Operation: 5.0 V
- Low Supply Current: 300 A
- Global Power Save Mode: 1 A Max
- Fast Settling Time for Load Change: 20 μ s
- Stable with 20 nF/ 100 Ω Loads
- CMOS/TTL Input Levels

ADM8831 Charge Pump Regulator for Color TFT Panels



ADM8831 Charge Pump Regulator for Color TFT Panels

- Three Voltages from One 3 V Supply
 - +5.1 V, +15.3 V, −10.2 V
- Power Efficiency Optimized for Use With TFT in Mobile Phones
- Shutdown Function
 - <1 μ A shutdown current
- Power Saving During Blanking Period
- Option to Use External LDO

SECTION 8

COMMUNICATIONS

RF/IF

SIGNAL PROCESSORS

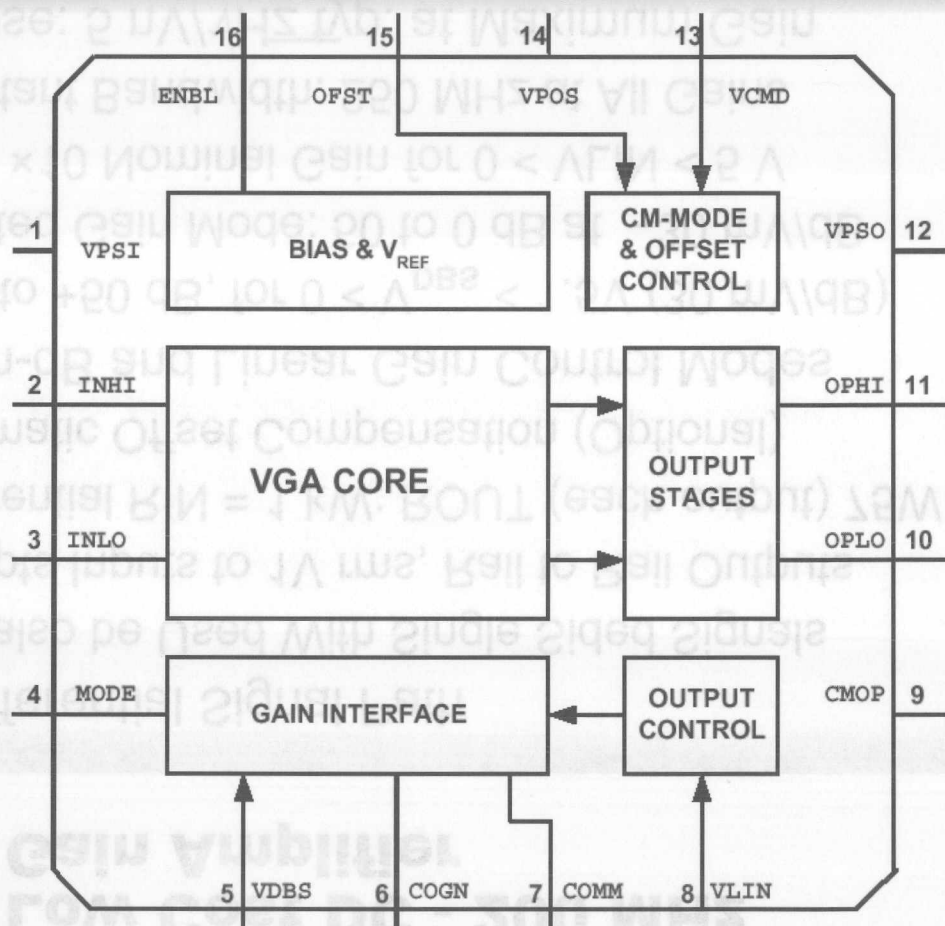
SIGNAL PROCESSORS

RF/IF

COMMUNICATIONS

SECTION 8

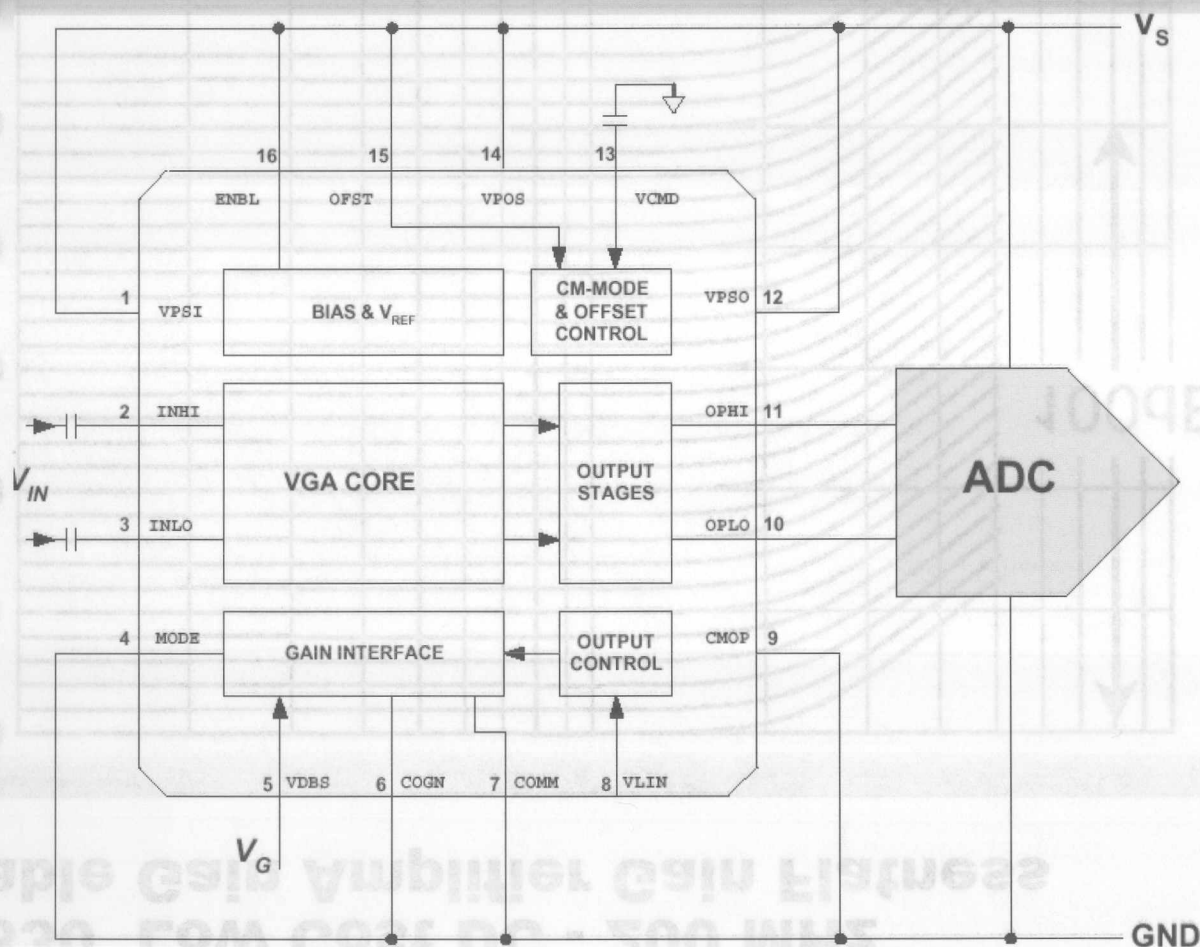
AD8330 Low Cost DC - 200 MHz Variable Gain Amplifier



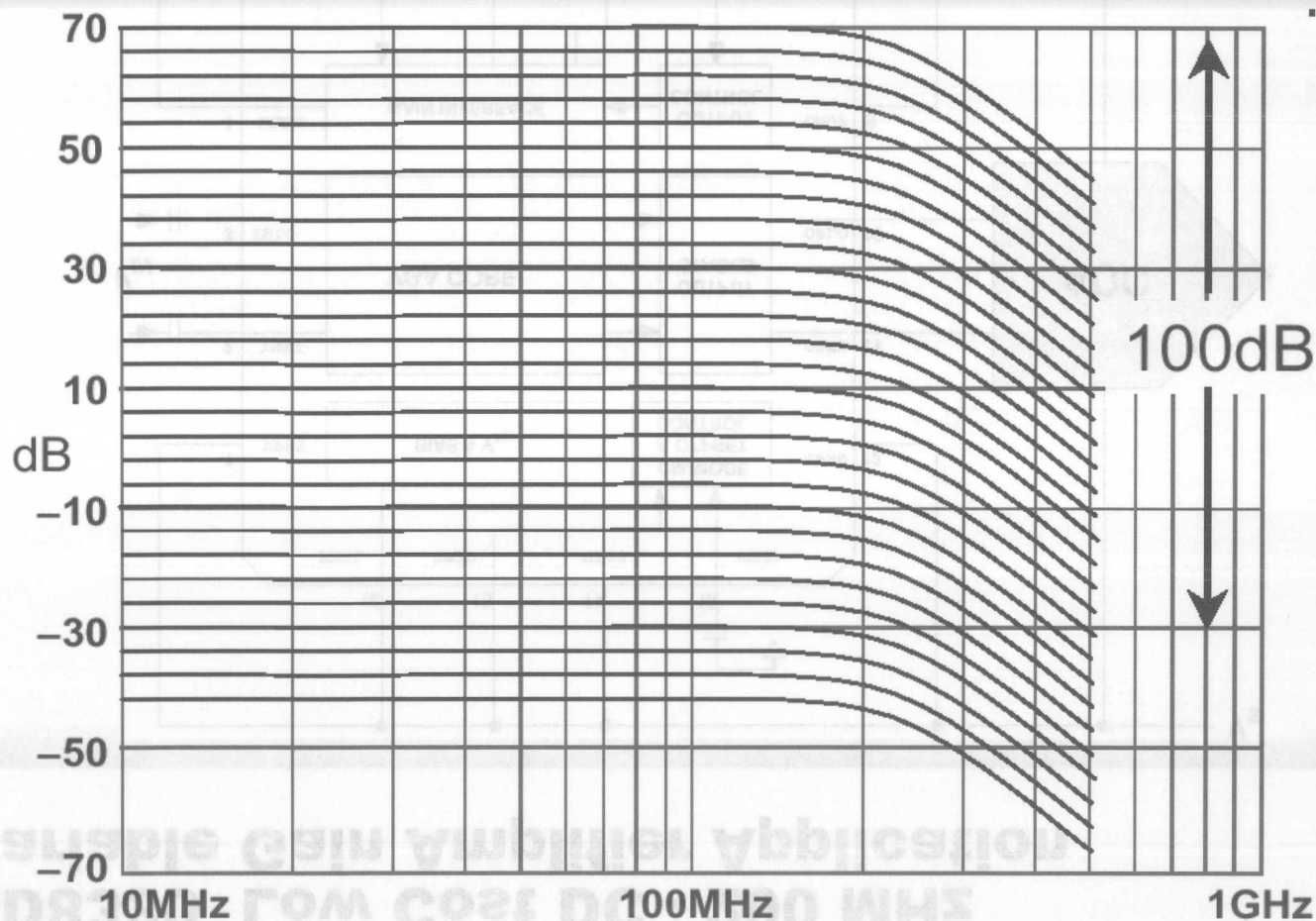
AD8330 Low Cost DC - 200 MHz Variable Gain Amplifier

- Fully Differential Signal Path
 - May also be Used With Single Sided Signals
 - Accepts Inputs to 1V rms, Rail to Rail Outputs
 - Differential RIN = 1 kW; ROUT (each output) 75W
 - Automatic Offset Compensation (Optional)
- Linear-in-dB and Linear Gain Control Modes
 - 0 dB to +50 dB, for $0 < V_{DBS} < 1.5V$ (30 mV/dB)
 - Inverted Gain Mode: 50 to 0 dB at -30 mV/dB
 - $\times 0$ to $\times 10$ Nominal Gain for $0 < V_{LIN} < 5 V$
 - Constant Bandwidth: 250 MHz at All Gains
- Low Noise: 5 nV/ \sqrt{Hz} typ. at Maximum Gain
- Low Distortion: < -60 dBc typ. at all Gains
- Low Power: 18 mA typ. at V_S of 2.7 V to 6 V

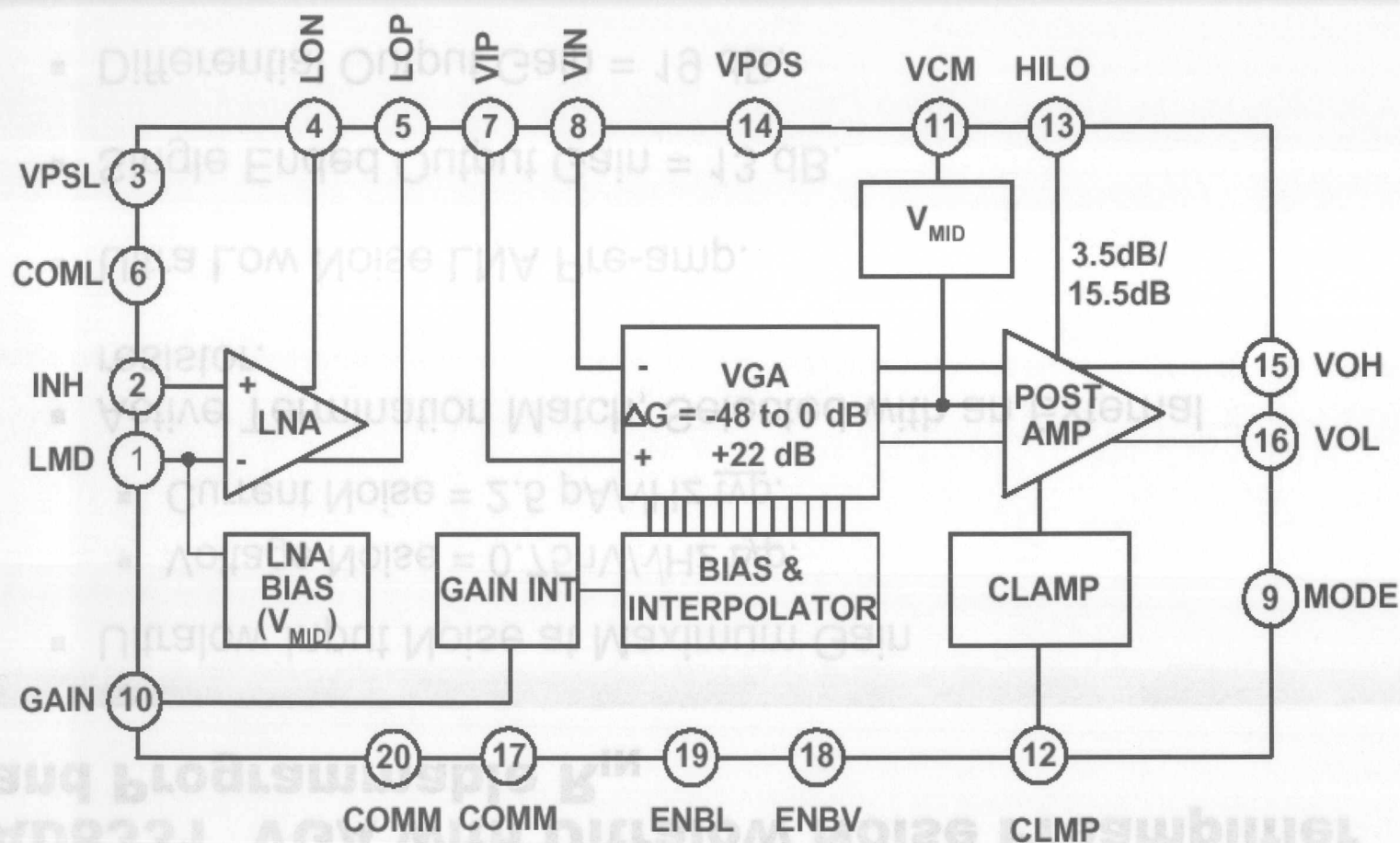
AD8330 Low Cost DC - 200 MHz Variable Gain Amplifier Application



AD8330 Low Cost DC - 200 MHz Variable Gain Amplifier Gain Flatness



AD8331 VGA with Ultralow Noise Preamplifier and Programmable R_{IN}



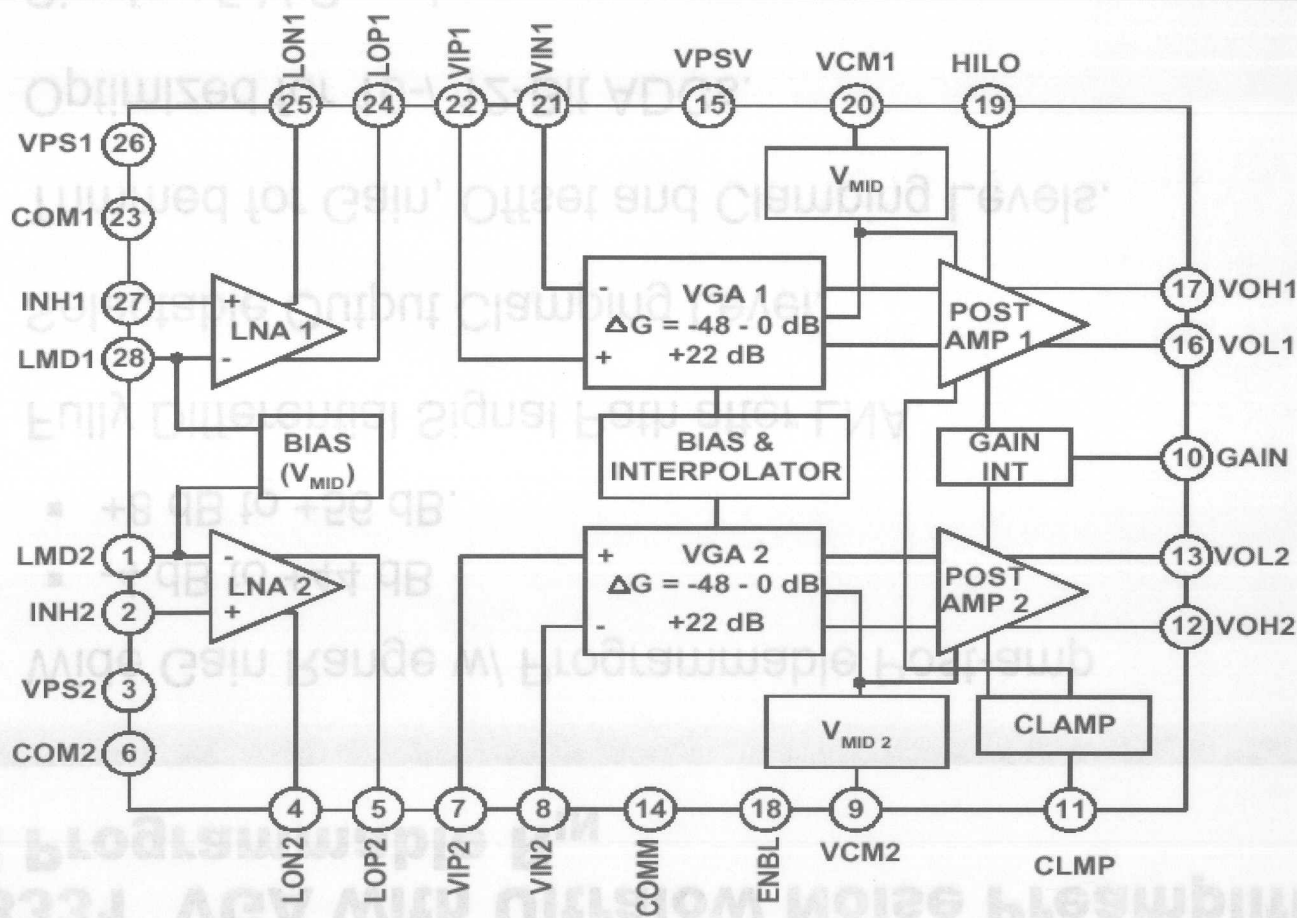
AD8331 VGA with Ultralow Noise Preamplifier and Programmable R_{IN}

- Ultralow Input Noise at Maximum Gain
 - Voltage Noise = $0.75\text{nV}/\sqrt{\text{Hz}}$ typ.
 - Current Noise = $2.5\text{ pA}/\sqrt{\text{Hz}}$ typ.
- Active Termination Match, Selected with an External resistor.
- Ultra Low Noise LNA Pre-amp.
- Single Ended Output Gain = 13 dB.
- Differential Output Gain = 19 dB.
- Bandwidth: 200 MHz (-3 dB)

AD8331 VGA with Ultralow Noise Preamplifier and Programmable R_{IN}

- Wide Gain Range w/ Programmable Post-amp
 - -4 dB to +44 dB
 - +8 dB to +56 dB.
- Fully Differential Signal Path after LNA.
- Selectable Output Clamping Level.
- Trimmed for Gain, Offset and Clamping Levels.
- Optimized for 10-/ 12-Bit ADCs.
- Single +5 V Supply

AD8332 Dual VGA with Ultralow Noise Preamplifier and Programmable R_{IN}



AD8332 Dual VGA with Ultralow Noise Preamplifier and Programmable R_{IN}

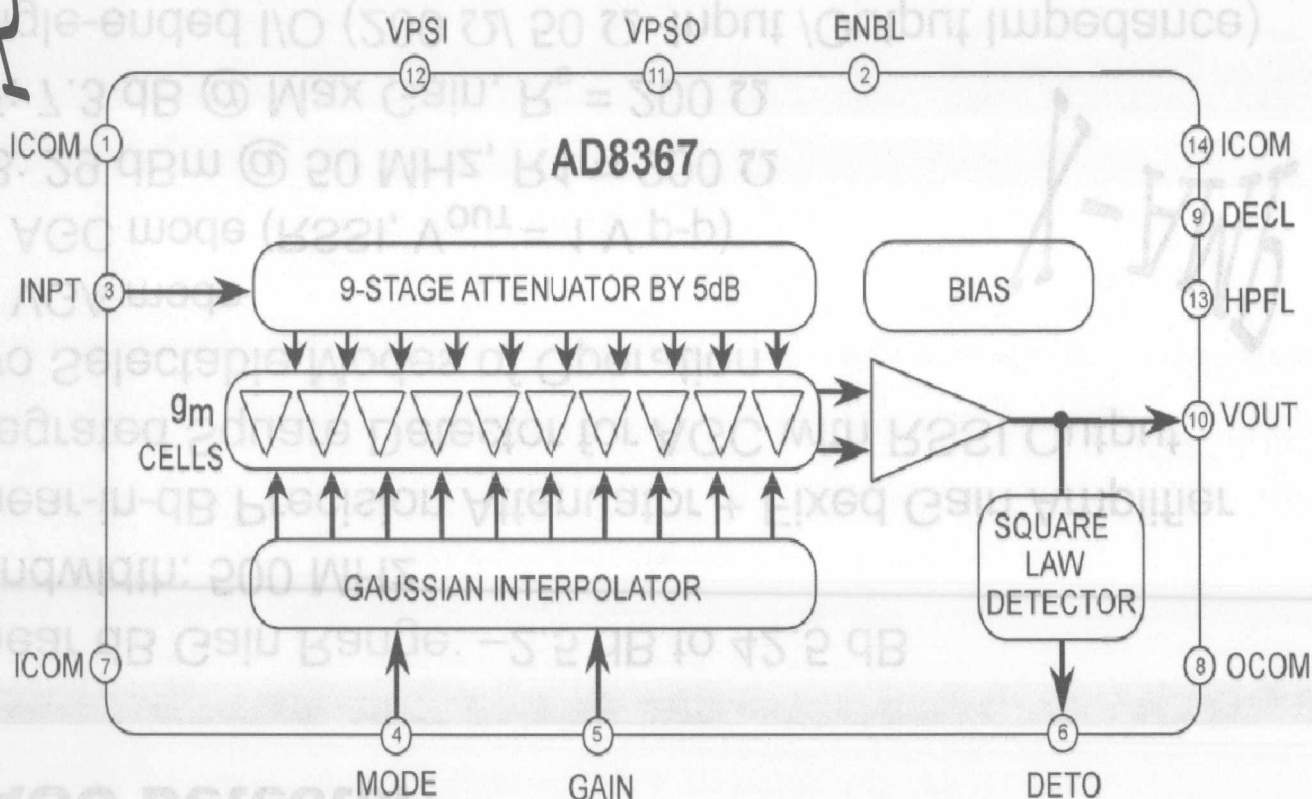
- Ultralow Input Noise at Maximum Gain
 - Voltage Noise = $0.75\text{nV}/\sqrt{\text{Hz}}$ typ.
 - Current Noise = $2.5\text{ pA}/\sqrt{\text{Hz}}$ typ.
- Active Termination Match, Selected with an External resistor.
- Ultra Low Noise LNA Pre-amp.
- Single Ended Output Gain = 14 dB.
- Differential Output Gain = 19 dB.
- Bandwidth: 200 MHz (-3 dB)

AD8332 Dual VGA with Ultralow Noise Preamplifier and Programmable R_{IN}

- Wide Gain Range w/ Programmable Post-amp
 - -4 dB to +44 dB
 - +8 dB to +56 dB.
- Fully Differential Signal Path after LNA.
- Selectable Output Clamping Level.
- Trimmed for Gain, Offset and Clamping Levels.
- Optimized for 10-/12-Bit ADCs.
- Single +5 V Supply

AD8367 LF – 500 MHz 45 dB VGA with AGC Detector

X-AMP



AD8367 LF – 500 MHz 45 dB VGA with AGC Detector

- Linear dB Gain Range: –2.5 dB to 42.5 dB
- Bandwidth: 500 MHz
- Linear-in-dB Precision Attenuator + Fixed Gain Amplifier
- Integrated Square Detector for AGC with RSSI Output
- Two Selectable Modes of Operation
 - VGA mode
 - AGC mode (RSSI, $V_{OUT} = 1\text{ V p-p}$)
- IP3: 29 dBm @ 50 MHz, $R_1 = 200\ \Omega$
- NF: 7.3 dB @ Max Gain, $R_s = 200\ \Omega$
- Single-ended I/O (200 Ω / 50 Ω Input /Output Impedance)
- Single Supply Operation 2.7 V – 5.5 V
- Power-Down Capability
- 14 Lead TSSOP Package

~~X-AMP~~

AD8367 LF to 500 MHz VGA

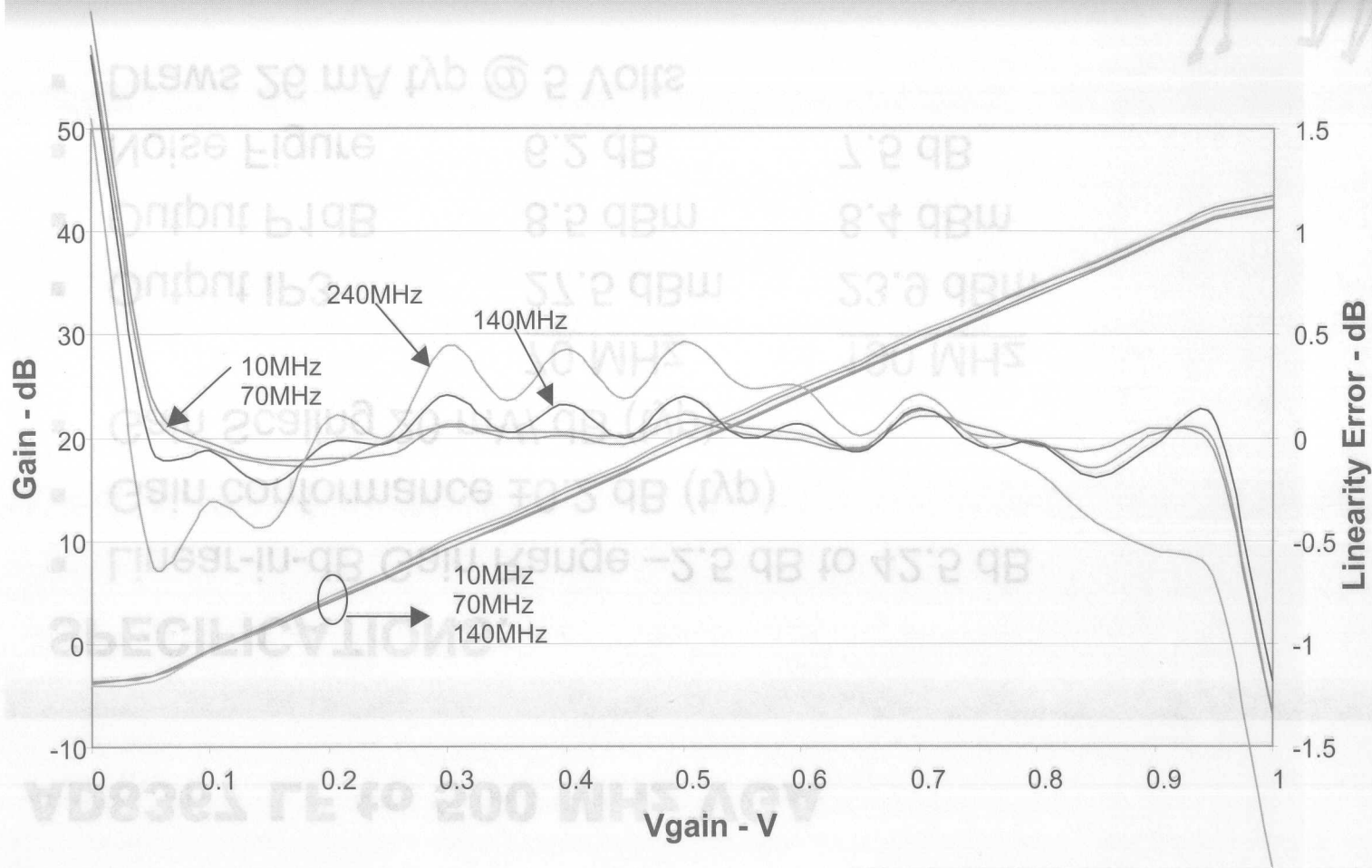
SPECIFICATIONS:

- Linear-in-dB Gain Range -2.5 dB to 42.5 dB
- Gain conformance ± 0.2 dB (typ)
- Gain Scaling 20 mV/ dB (typ)

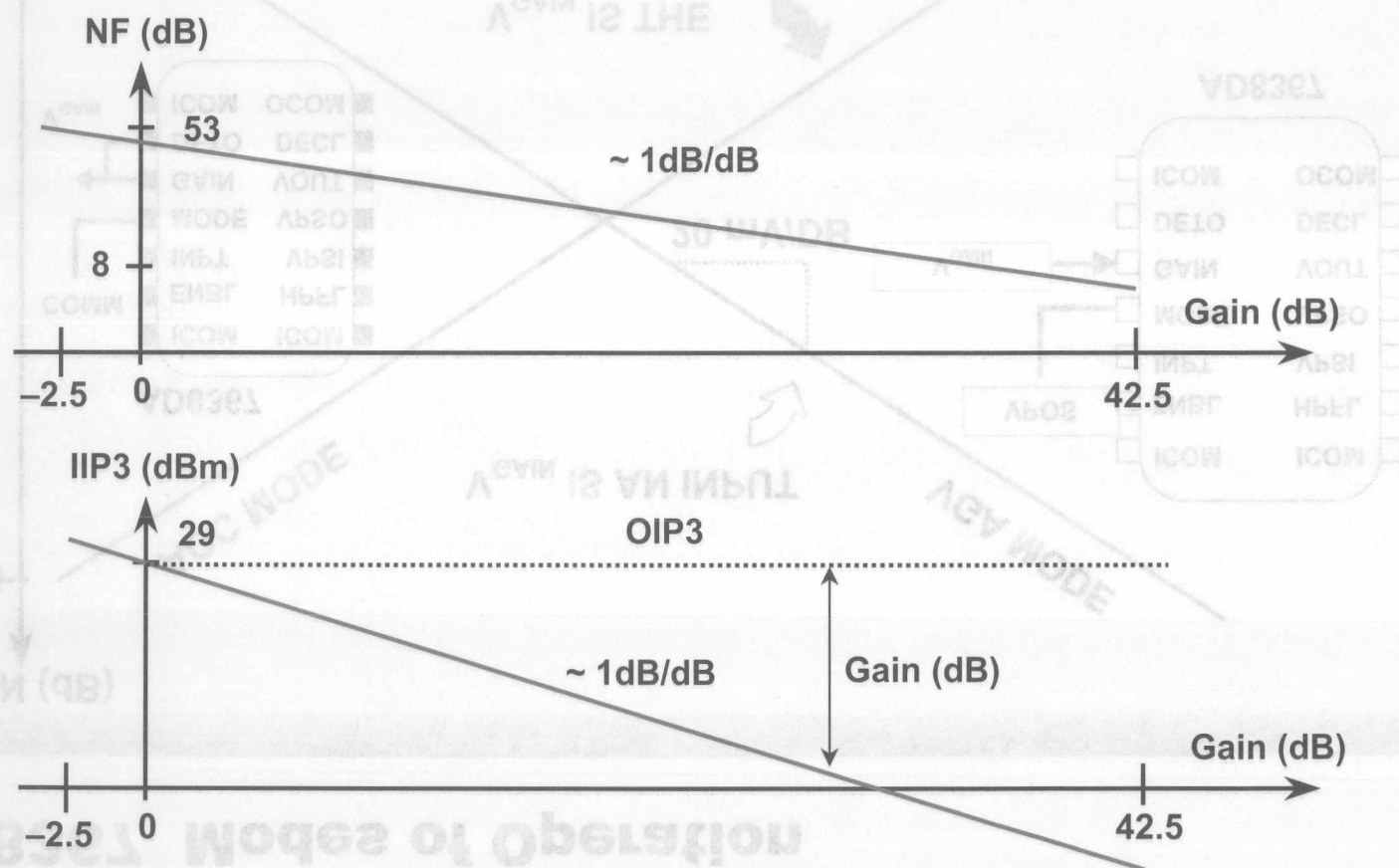
	<u>70 MHz</u>	<u>190 MHz</u>
▪ Output IP3	27.5 dBm	23.9 dBm
▪ Output P1dB	8.5 dBm	8.4 dBm
▪ Noise Figure	6.2 dB	7.5 dB
▪ Draws 26 mA typ @ 5 Volts		

X-AMP

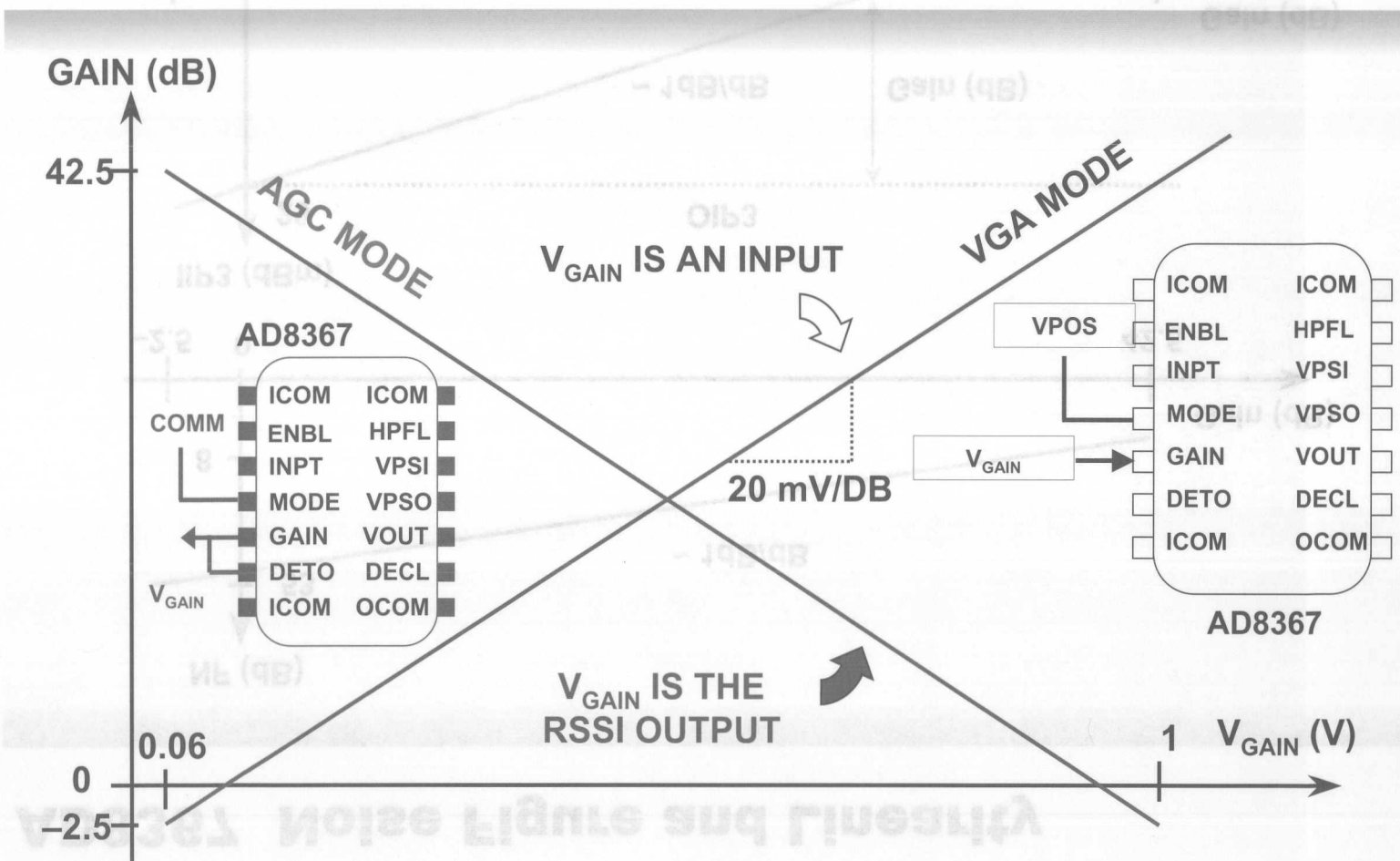
AD8367 IF Accuracy



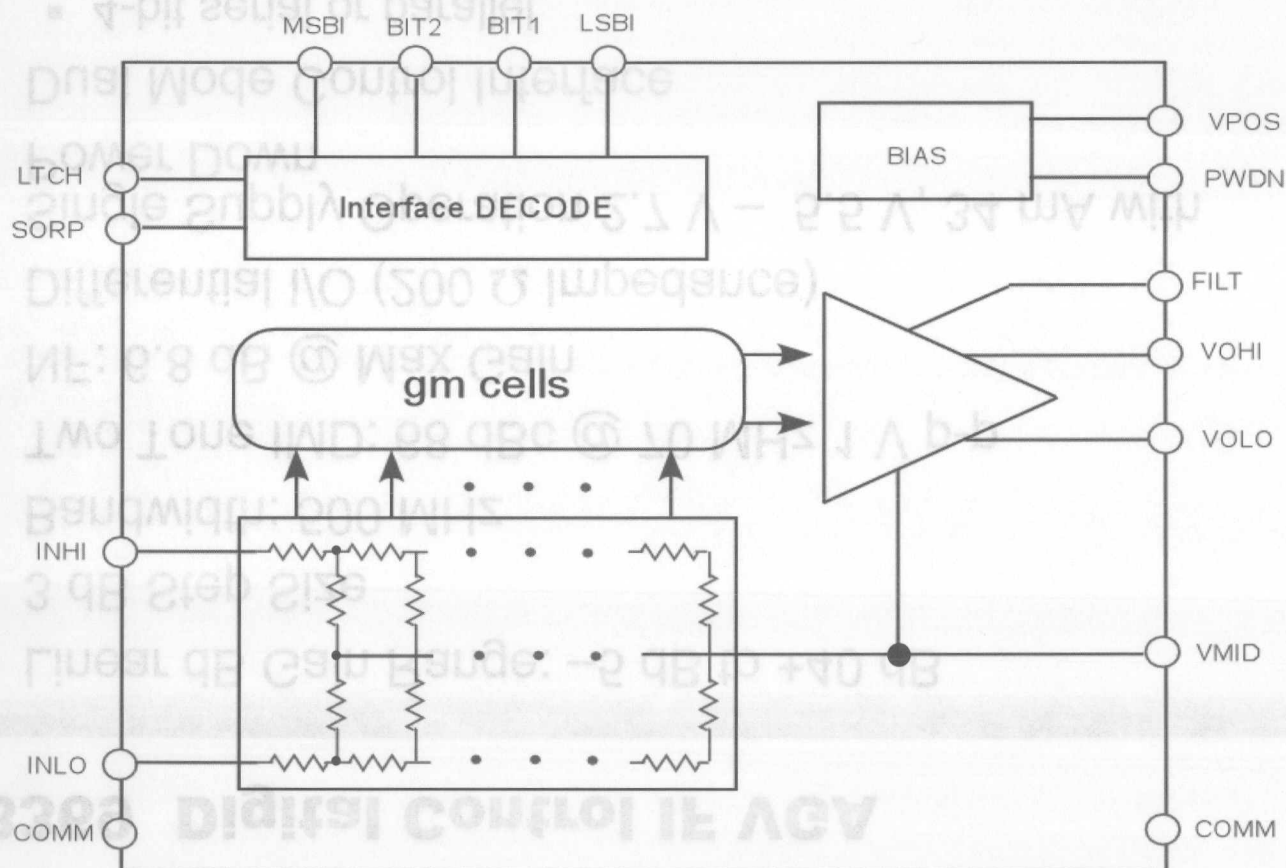
AD8367 Noise Figure and Linearity



AD8367 Modes of Operation



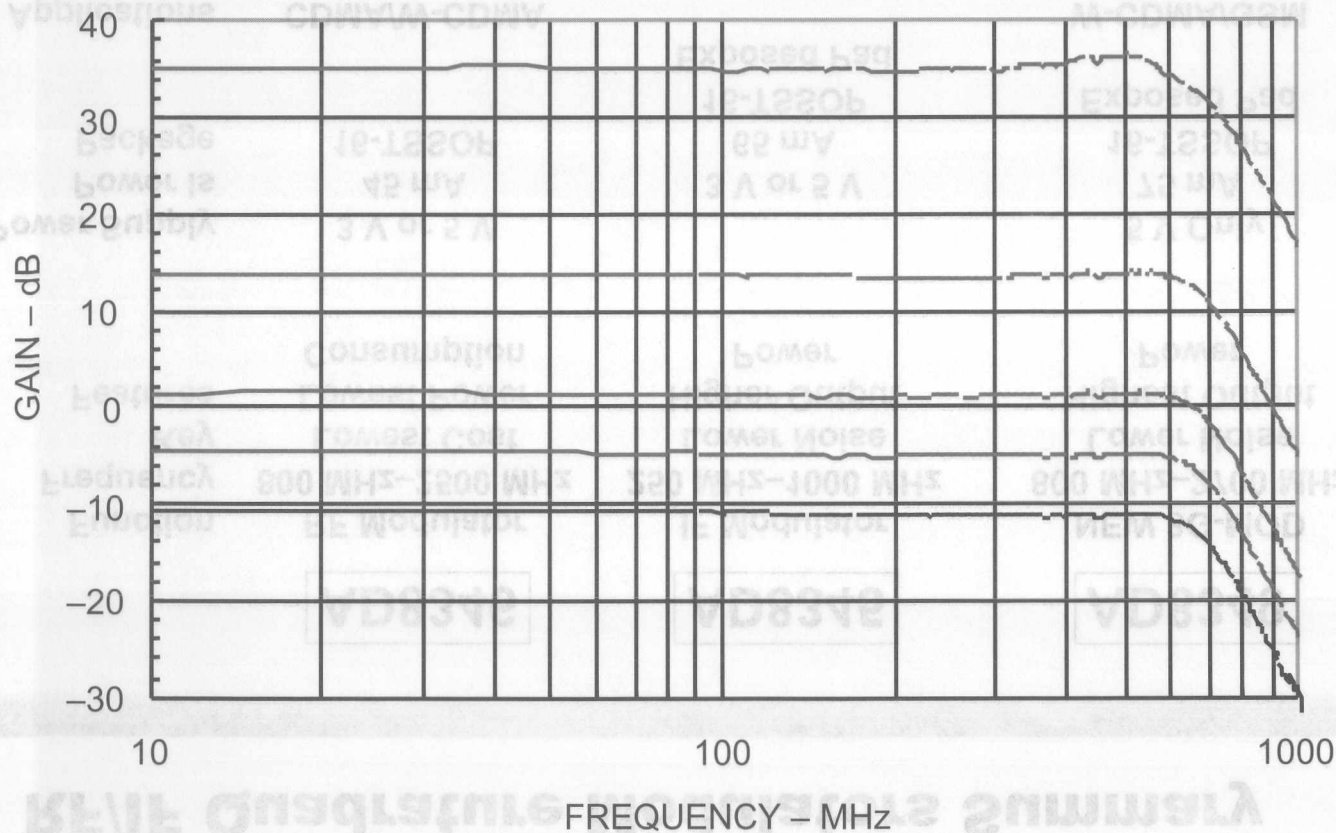
AD8369 Digital Control IF VGA



AD8369 Digital Control IF VGA

- Linear dB Gain Range: -5 dB to +40 dB
- 3 dB Step Size
- Bandwidth: 500 MHz
- Two Tone IMD: 68 dBc @ 70 MHz 1 V p-p
- NF: 6.8 dB @ Max Gain
- Differential I/O (200 Ω Impedance)
- Single Supply Operation 2.7 V – 5.5 V, 34 mA with Power Down
- Dual Mode Control Interface
 - 4-bit serial or parallel
 - Latch enable feature

AD8369 Digital Gain Control



RF/IF Quadrature Modulators Summary

	AD8346	AD8345	AD8349
Function	RF Modulator	IF Modulator	NEW 3G-MOD
Frequency	800 MHz–2500 MHz	250 MHz–1000 MHz	800 MHz–2700 MHz
Key Features	Lowest Cost Lowest Power Consumption	Lower Noise Higher Output Power	Lower Noise Highest Output Power
Power Supply	3 V or 5 V	3 V or 5 V	5 V Only
Power Is	45 mA	65 mA	75 mA
Package	16-TSSOP	16-TSSOP Exposed Pad	16-TSSOP Exposed Pad
Applications	CDMA/W-CDMA WLL, QPSK 3 V Applications	IF—All STDs Direct 800/900 GSM QAM Modulators SSB Mixer	W-CDMA/GSM QAM Modulators SSB Mixer

The AD8345/6/9 are pin compatible

AD8349 800 MHz – 2.7 GHz Quadrature Modulator

• BiCMOS Compatible With AD8348 / AD8342

• 20 mA Wiper Output Dissipation

• 25 mA Total Current

• Single Supply 4.5 – 5.5 V

• Amplitude Balance: 0.5 dB

• Phase Quadrature

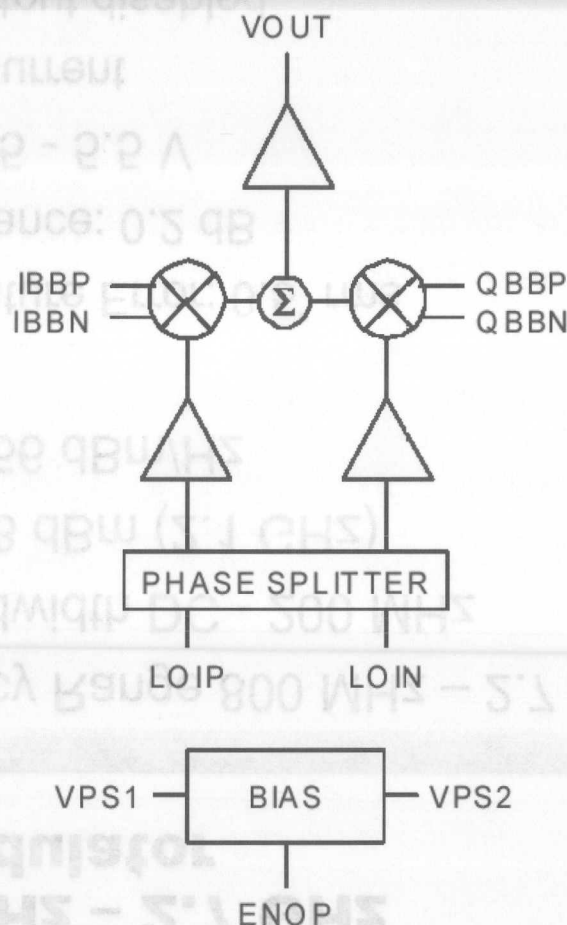
• High Accuracy

• Noise Floor: -128 dBm

• Output Level: +3 dBm (1 GHz)

• Modulation Bandwidth: DC – 500 MHz

• Output Frequency Range: 800 MHz – 2.7 GHz

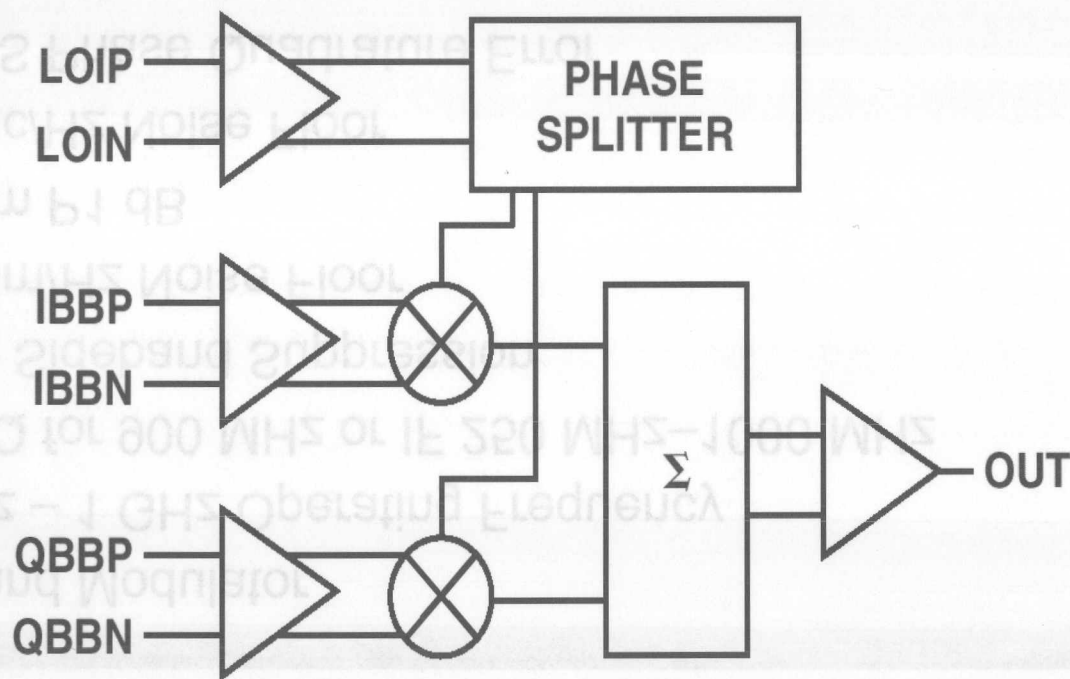


MATCHED 50 Ω
OUTPUTS

AD8349 800 MHz – 2.7 GHz Quadrature Modulator

- Output Frequency Range 800 MHz – 2.7 GHz
- Modulation Bandwidth DC - 200 MHz
- Output Level: +3 dBm (2.1 GHz)
- Noise Floor: –156 dBm/Hz
- High Accuracy
 - Phase Quadrature Error: 0.5° rms
 - Amplitude Balance: 0.2 dB
- Single Supply 4.5 - 5.5 V
 - 95 mA Total Current
 - 50 mA with output disabled
- Pin Compatible With AD8346 / AD8345
- 16-lead exposed paddle TSSOP package

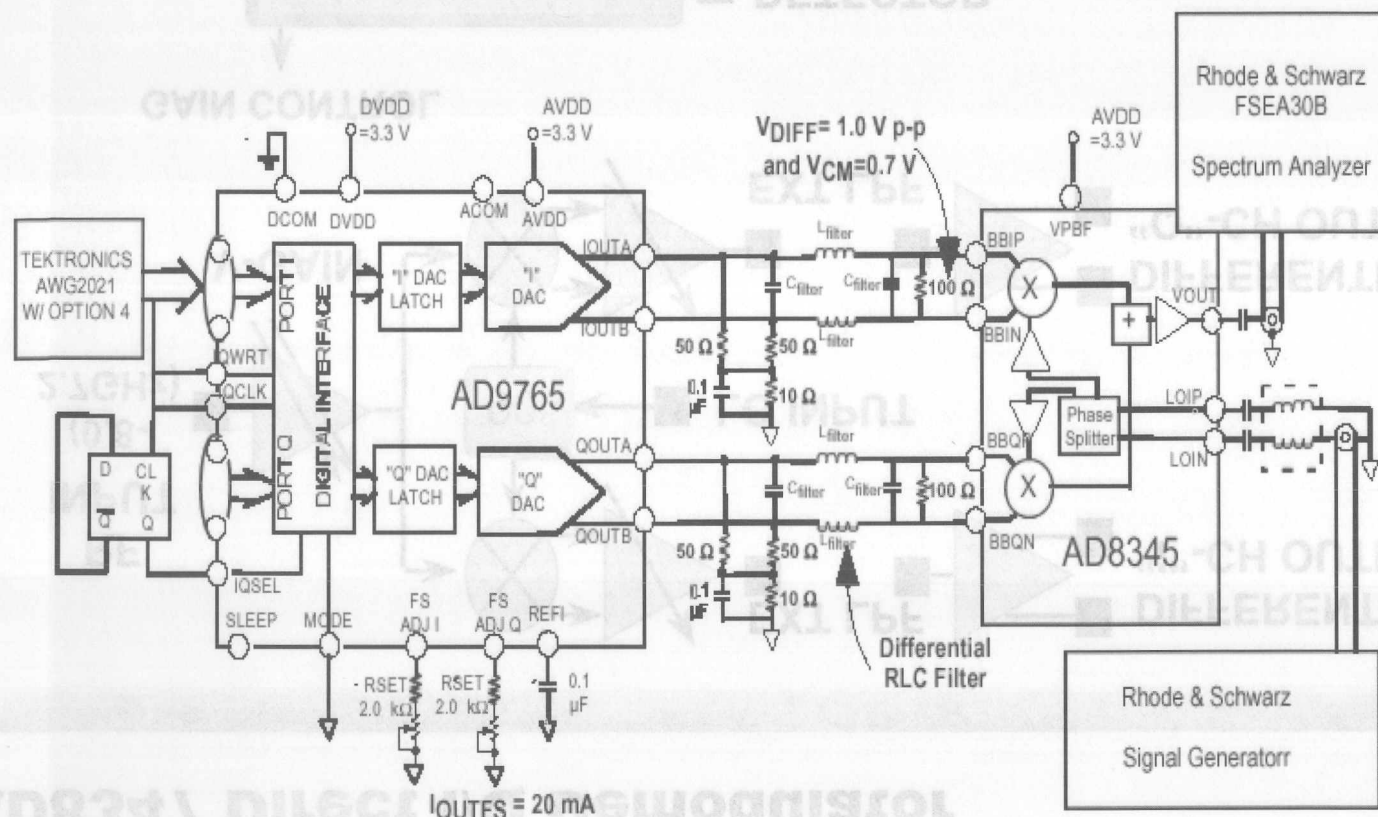
AD8345 250 MHz – 1 GHz Quadrature Modulator



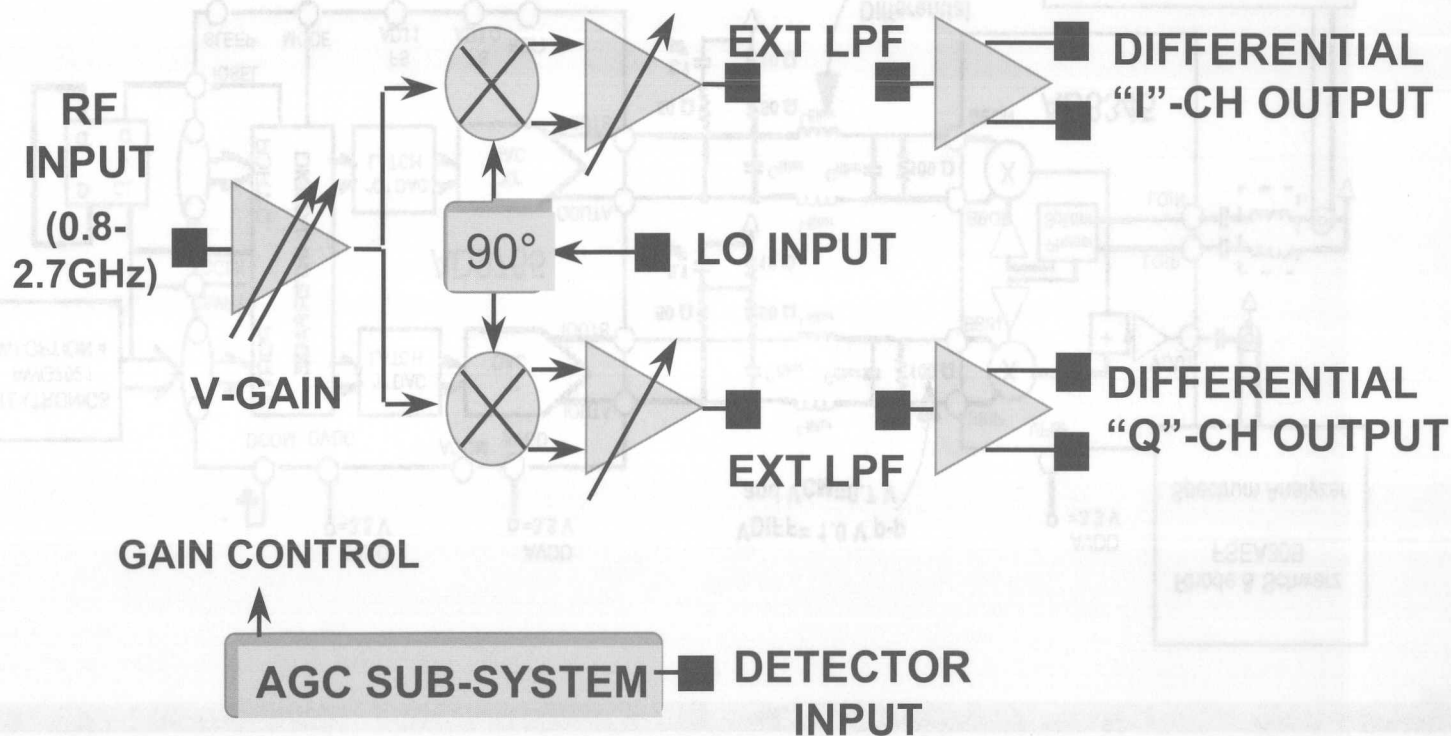
AD8345 250 MHz – 1 GHz Quadrature Modulator

- Broadband Modulator
- 250 MHz – 1 GHz Operating Frequency
- Direct I/Q for 900 MHz or IF 250 MHz–1000 MHz
- –42 dBc Sideband Suppression
- –155 dBm/Hz Noise Floor
- +2.5 dBm P1 dB
- –150 dBc/Hz Noise Floor
- 0.5° RMS Phase Quadrature Error
- 0.2 dB Amplitude Balance
- 3.7 V – 5.5 V Supply Range
- 16-Lead TSSOP Exposed Pad
(Pin Compatible with AD8346)

AD8345 Interface with TxDAC



AD8347 Direct I/Q Demodulator



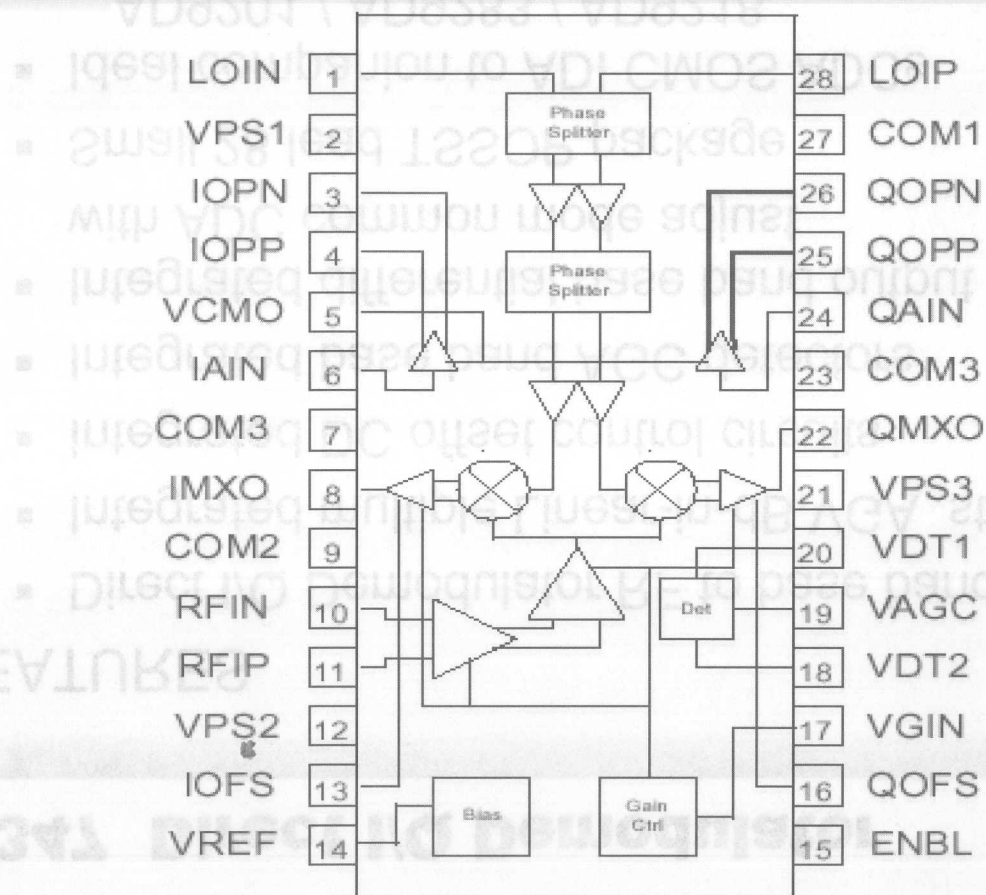
RF / IF demodulator linear gain control with base band output amplifiers

AD8347 Direct I/Q Demodulator

FEATURES

- Direct I/Q Demodulator RF to base band
- Integrated multiple Linear-in-dB VGA stages
- Integrated DC offset control circuits
- Integrated base band AGC detectors
- Integrated differential base band output amplifiers with ADC common mode adjust
- Small 28 lead TSSOP package
- Ideal companion to ADI CMOS ADCs
AD9201 / AD9283 / AD9218

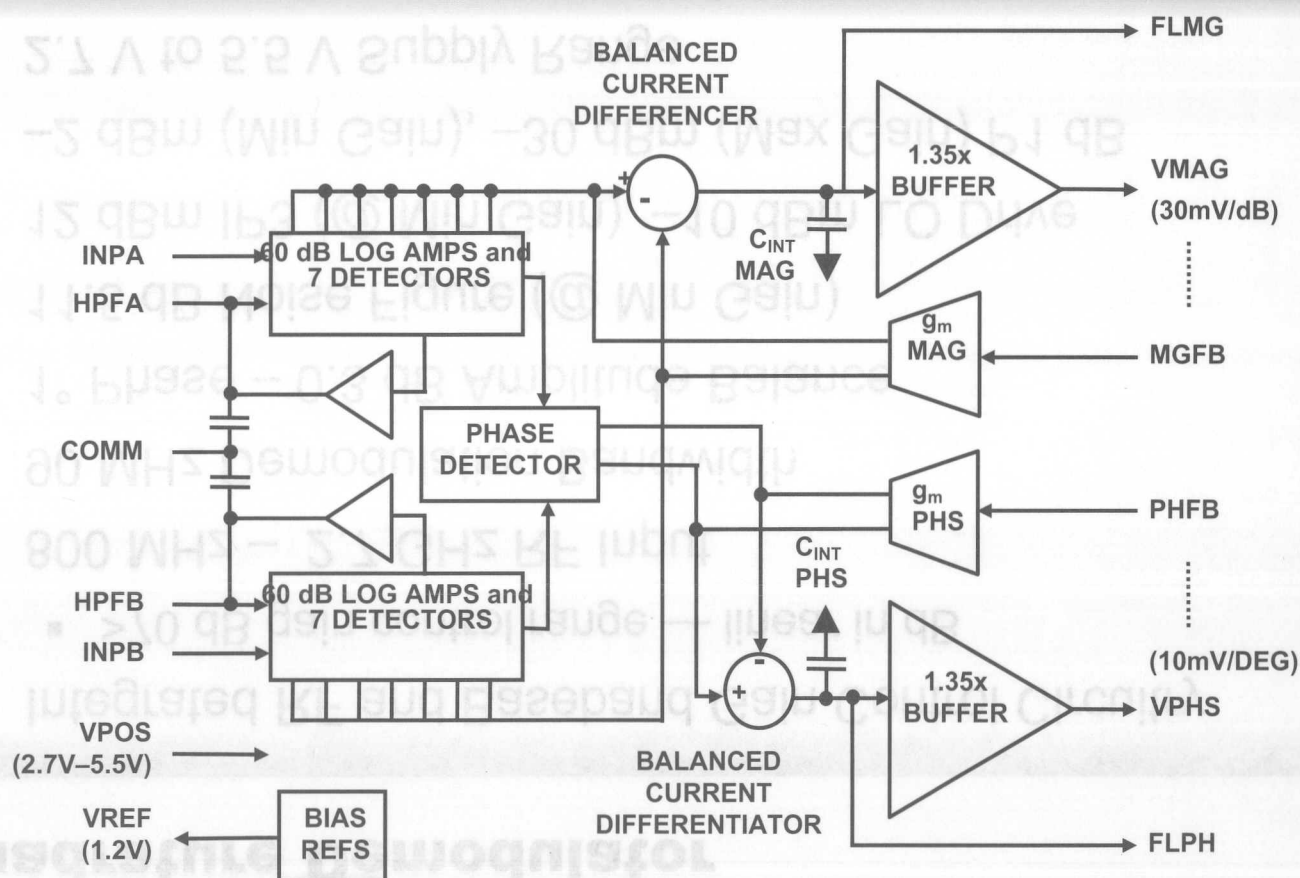
AD8347 2.3 GHz Direct Conversion Quadrature Demodulator



AD8347 2.3 GHz Direct Conversion Quadrature Demodulator

- Integrated RF and Baseband Gain Control Circuitry
 - >70 dB gain control range — linear in dB
- 800 MHz – 2.7 GHz RF Input
- 90 MHz Demodulation Bandwidth
- 1° Phase – 0.3 dB Amplitude Balance
- 11.5 dB Noise Figure (@ Min Gain)
- 12 dBm IP3 (@ Min Gain), –10 dBm LO Drive
- –2 dBm (Min Gain), –30 dBm (Max Gain) P1 dB
- 2.7 V to 5.5 V Supply Range
 - 64 mA supply current (@ 5 V)
 - Power-down to 30 μ A

AD8302 Gain Phase Detector



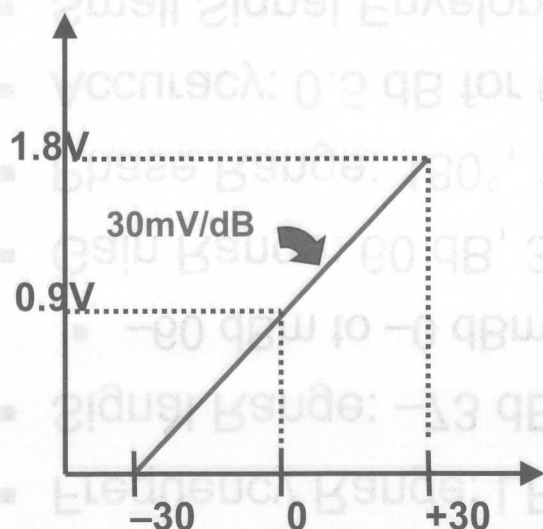
AD8302 Gain Phase Detector

- Frequency Range: LF – 2.7 GHz
- Signal Range: –73 dBV to –13 dBV
 - –60 dBm to –0 dBm referenced to 50 Ω
- Gain Range: 60 dB, 30 mV/dB, 0 V to 1.8 V
- Phase Range: 180°, 10 mV/°, 0 V to 1.8 V
- Accuracy: 0.5 dB for Gain, 1° for Phase
- Small Signal Envelop Bandwidth: 30 MHz
- Response Time: 60 ns for 30% Change
- Current Consumption: 19 mA Room Temperature
- Supply Voltage: 2.7 V to 5.5 V

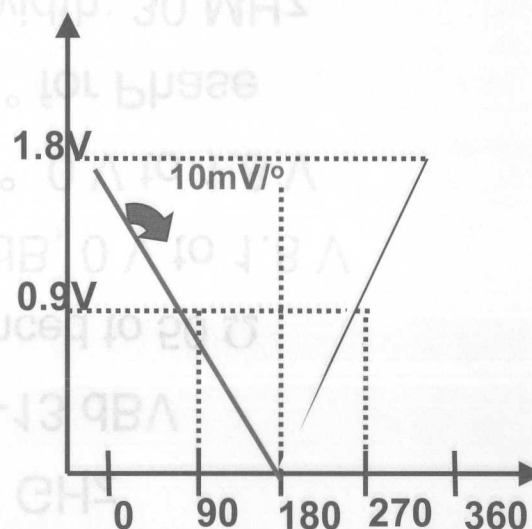
AD8302 Gain Phase Detector Output Characteristics

$$V_{MAG} = 600 \text{ mV} \log(V_a/V_b) + 900 \text{ mV}$$

$$V_{PHS} = 10 \text{ mV} (f_a - f_b - 90^\circ) + 900 \text{ mV}$$



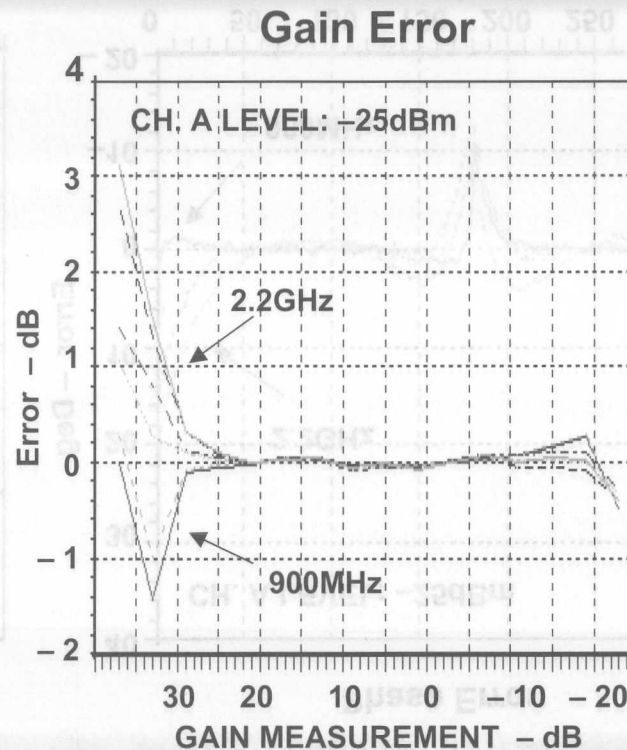
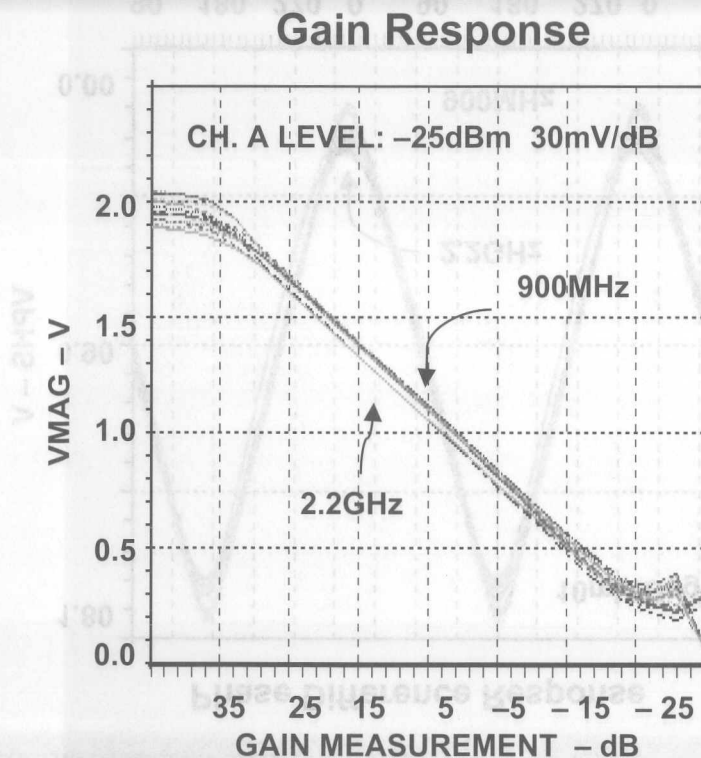
Gain (dB)



Phase (°)

AD8302 Gain Phase Detector

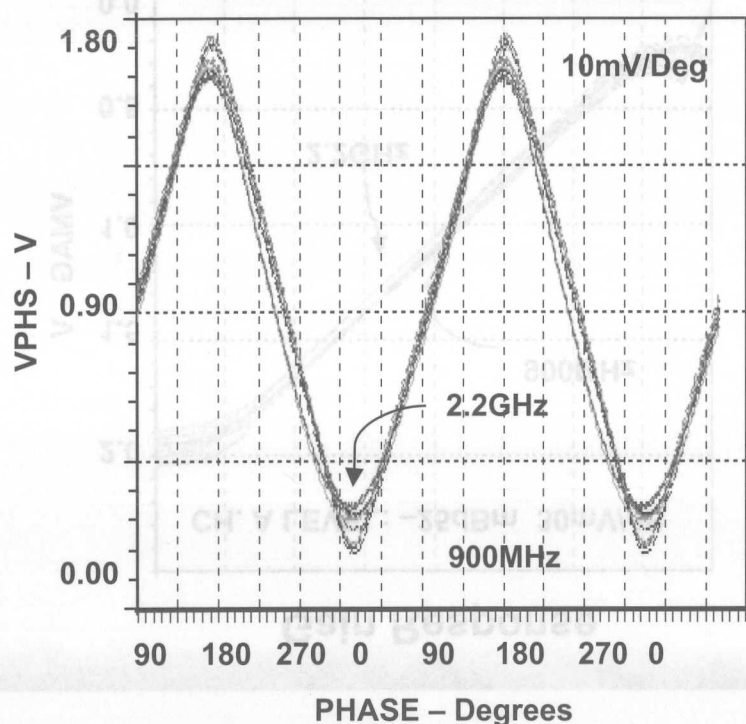
Gain Measurement Performance



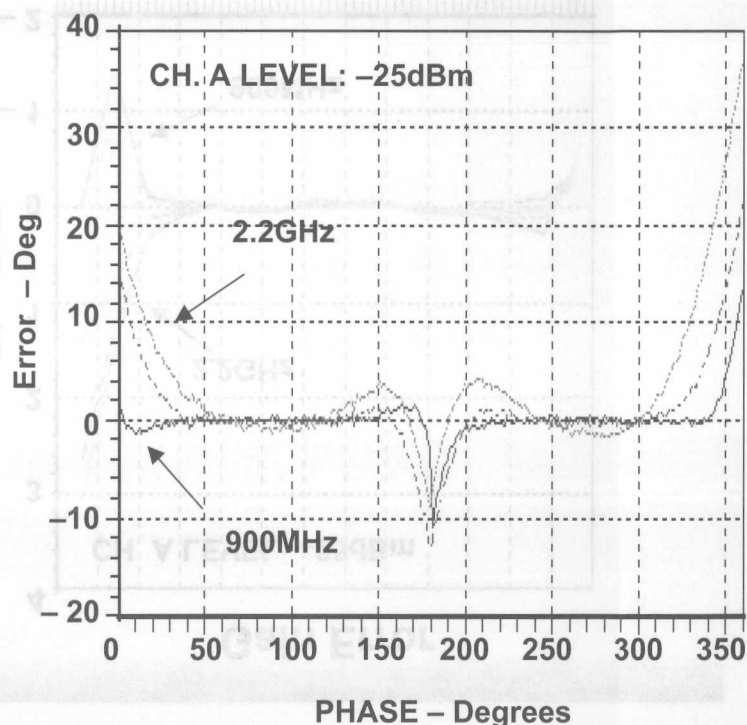
Gain measurement response maintains integrity beyond 2.2 GHz with a precise slope of 30 mV/dB while maintaining <0.2 dB error over >40 dB of gain range.

AD8302 Gain Phase Detector Phase Measurement Performance

Phase Difference Response

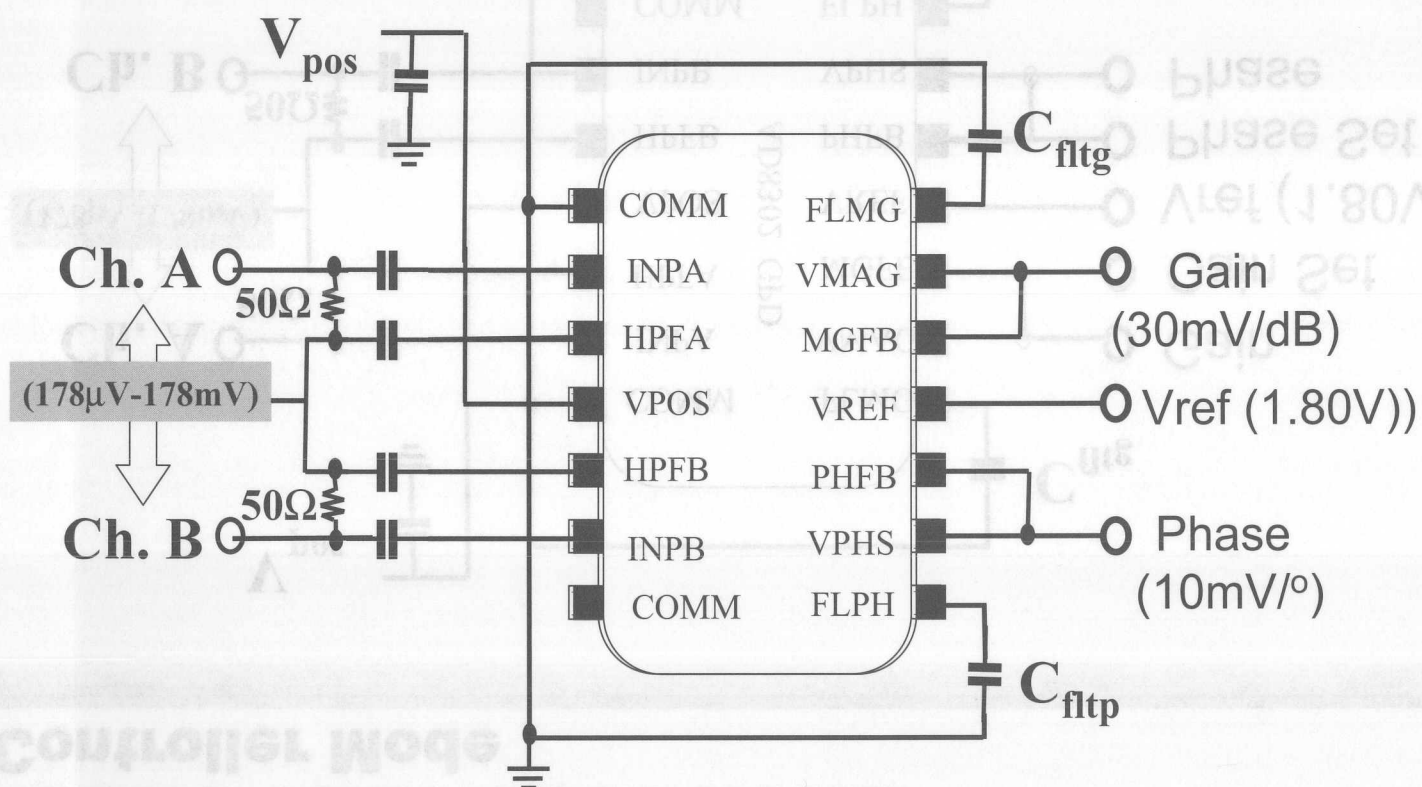


Phase Error

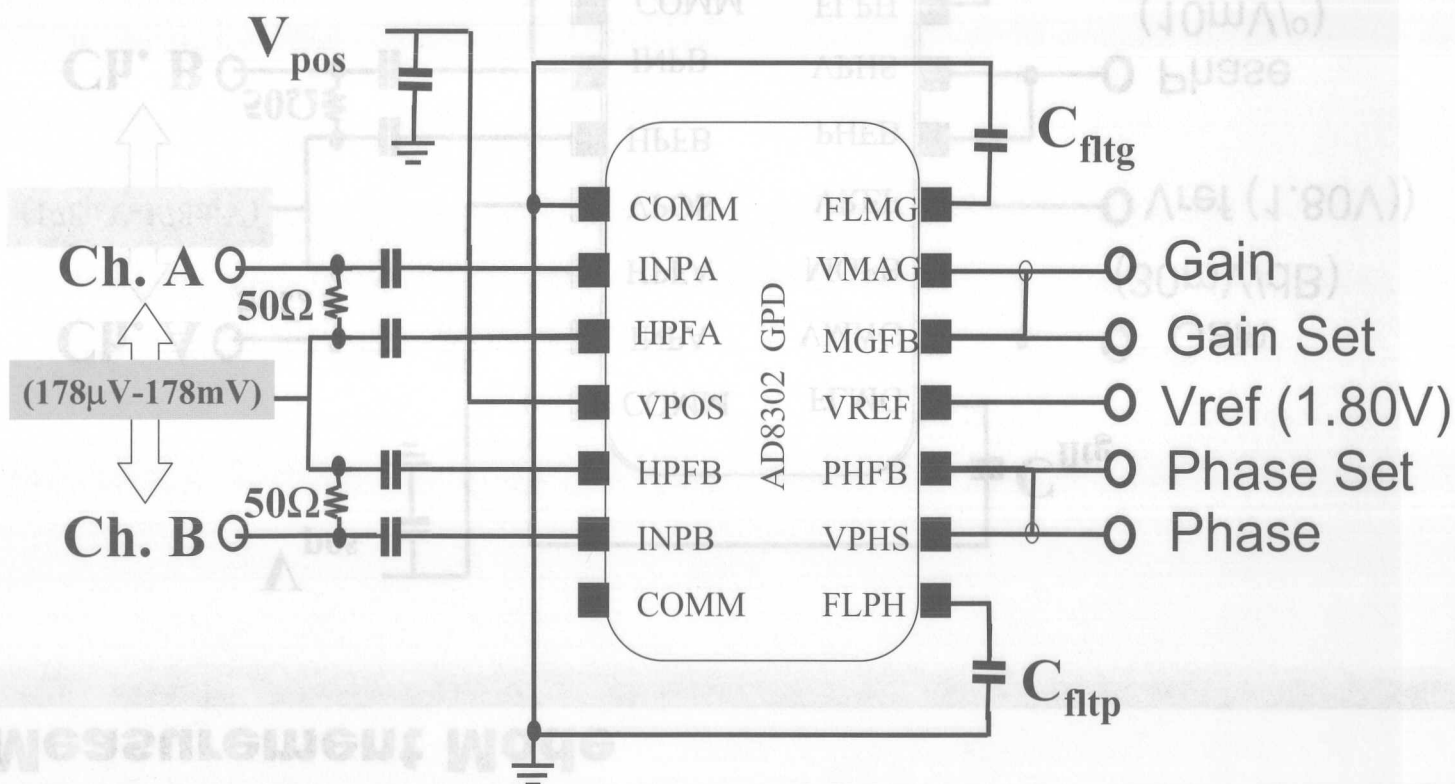


Phase measurement response shows a precise slope of 10 mV/deg with a phase error $<1^\circ$ over the entire phase range

AD8302 Gain Phase Detector Measurement Mode



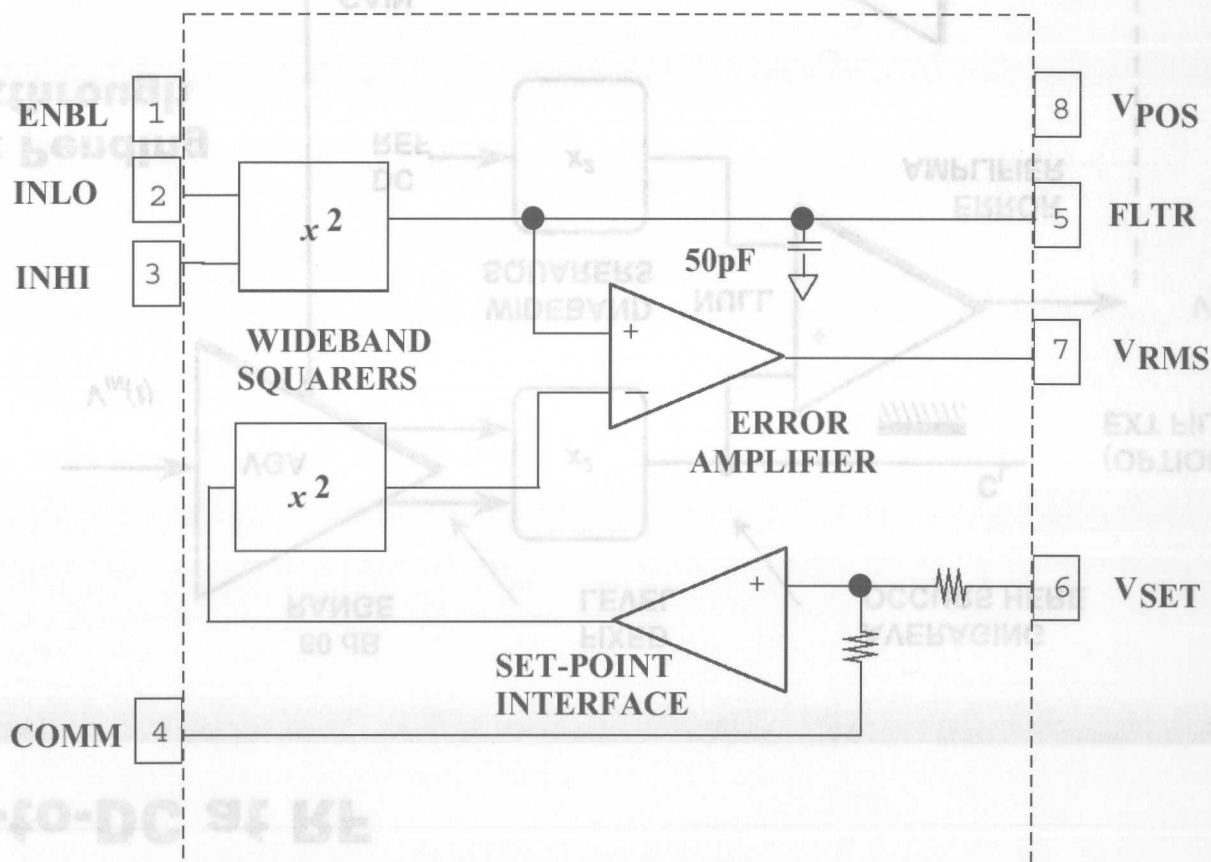
AD8302 Gain Phase Detector Controller Mode



Patent Pending Breakthrough



AD8362 60 dB TruPwr Detector RMS-to-DC at RF

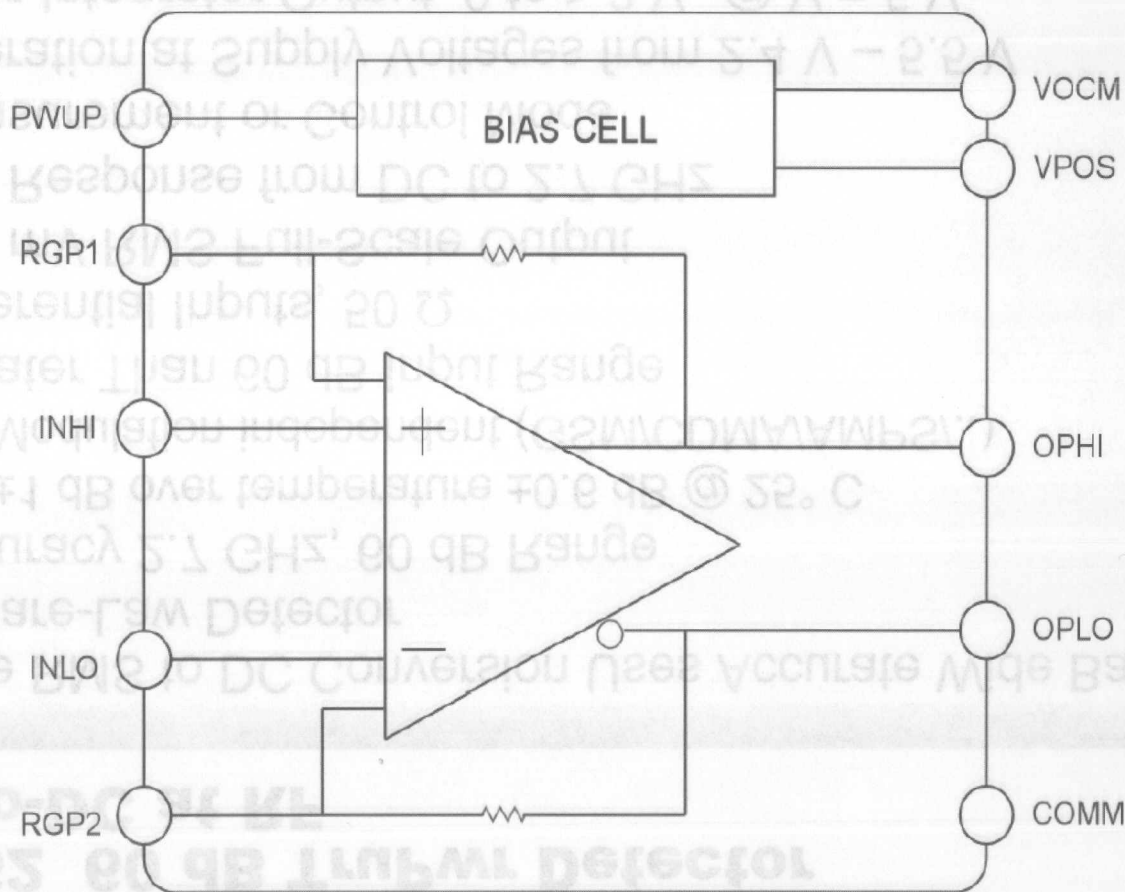


AD8362 60 dB TruPwr Detector RMS-to-DC at RF

- True RMS to DC Conversion Uses Accurate Wide Band Square-Law Detector
- Accuracy 2.7 GHz, 60 dB Range
 - ± 1 dB over temperature ± 0.6 dB @ 25° C
 - Modulation independent (GSM/CDMA/AMPS/..)
- Greater Than 60 dB Input Range
- Differential Inputs, 50 Ω
- 100 mV RMS Full-Scale Output
- Flat Response from DC to 2.7 GHz
- Measurement or Control Mode
- Operation at Supply Voltages from 2.4 V – 5.5 V
- Error-Integrator Output, 0 to $> 3 V_p$ @ $V = 5 V$
- External Capacitor Extends $T_{AVERAGE}$
- Rapid Power-Down to 1 μA Max

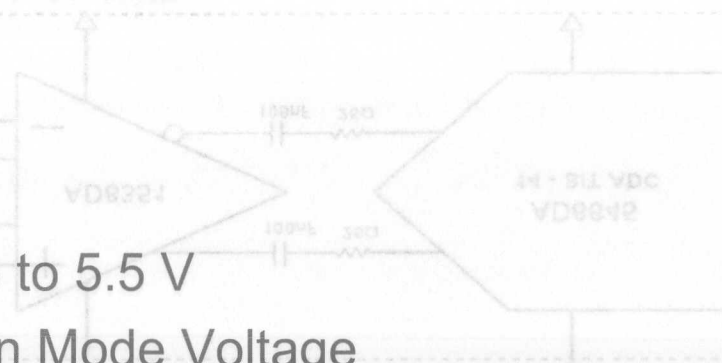
AD8351 Low Distortion Differential Amplifier

- Excellent Crossover Frequency
- Error Integral Output $0.10 > 3 \text{ V}^2 @ V = 2 \text{ V}$
- Operation at Supply Voltages from $5 \text{ V} - 2.2 \text{ V}$
- Measurement of Control Signals
- Fast Response from DC to 5 MHz
- 100 MHz Full-Scale Output
- Differential Inputs 20 V
- Greater Than 60 dB Input Range
- Multiplexed Input (25 MHz)
- $\pm 1 \text{ V}$ over temperature $\pm 0.5 \text{ V} @ 52^\circ \text{C}$
- Accuracy 5 V 5 MHz 50 V Range
- Square-Wave Detector
- True RMS to DC Conversion Uses Accurate Mode Band

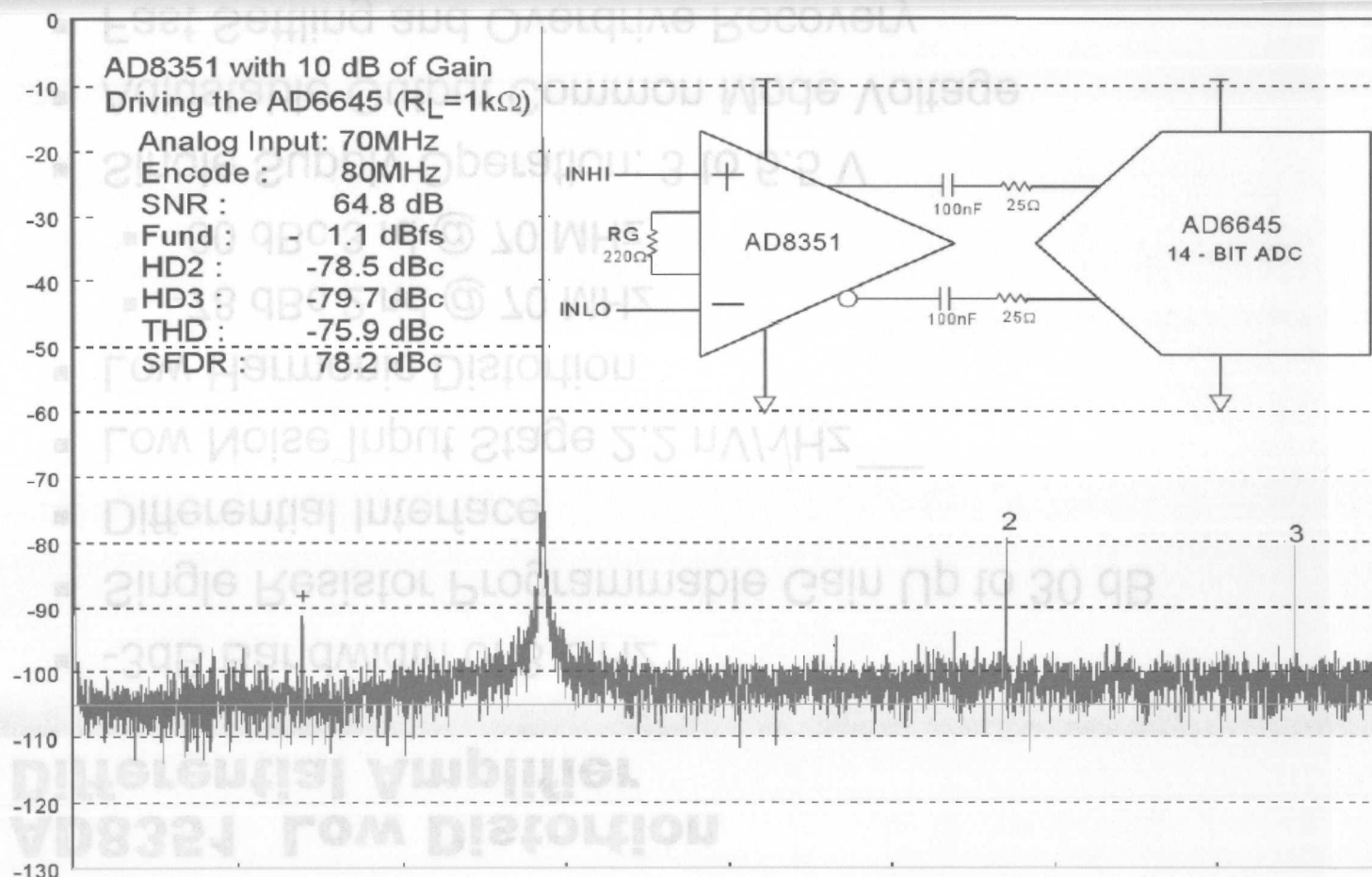


AD8351 Low Distortion Differential Amplifier

- -3dB Bandwidth of 3 GHz
- Single Resistor Programmable Gain Up to 30 dB
- Differential Interface
- Low Noise Input Stage $2.2 \text{ nV}/\sqrt{\text{Hz}}$
- Low Harmonic Distortion
 - -78 dBc 2nd @ 70 MHz
 - -80 dBc 3rd @ 70 MHz
- Single Supply Operation: 3 to 5.5 V
- Adjustable Output Common Mode Voltage
- Fast Settling and Overdrive Recovery
- Power Down Capability
- 10 Pin Micro SO Package

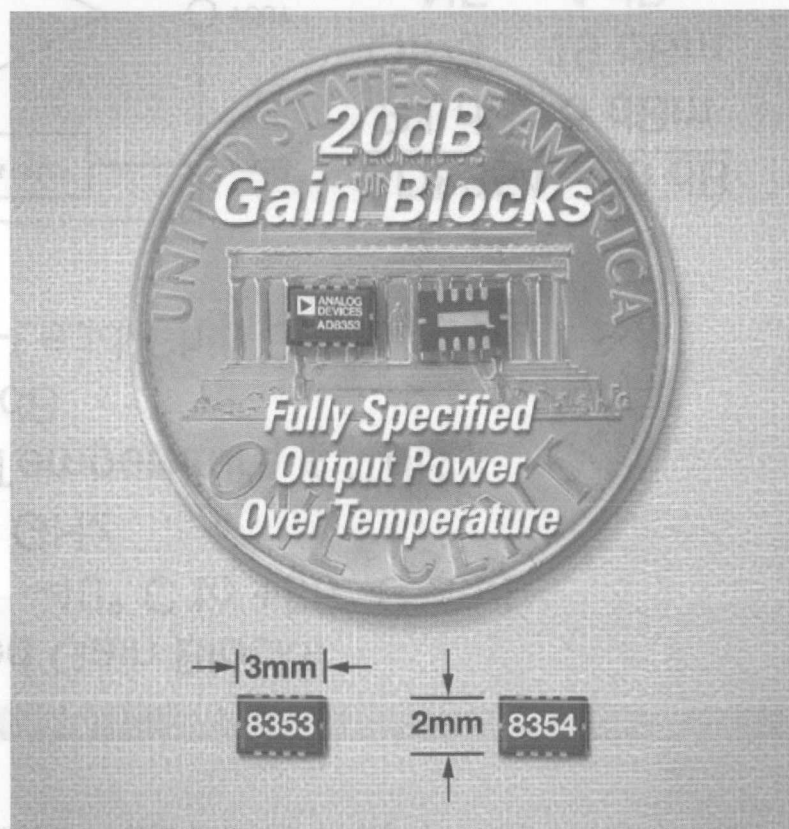


AD8351 Low Distortion Differential Amplifier



AD8353/54 Gain Blocks in CSP

- 3 x 2 mm Chip Scale Package with exposed paddle
- Excellent thermal impedance for low operating junction temperatures
- Excellent package parasitic impedances for good performance over frequency

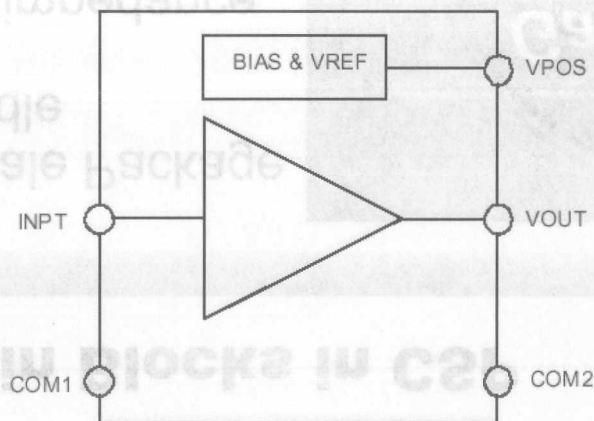


AD8353/54 100 MHz – 2.7 GHz RF Gain Block

- Silicon Bipolar 50 Ω Matched Gain Blocks
- Fully Specified Over Temp: -40°C to $+85^{\circ}\text{C}$ and Frequency 100 MHz – 2.7 GHz
- Output Power Stable Over Temperature $< 1\text{ dB}$
- Excellent Gain Stability $< 1\text{ dB}$
- Package in 3 mm x 2 mm 8-Lead Chip Scale

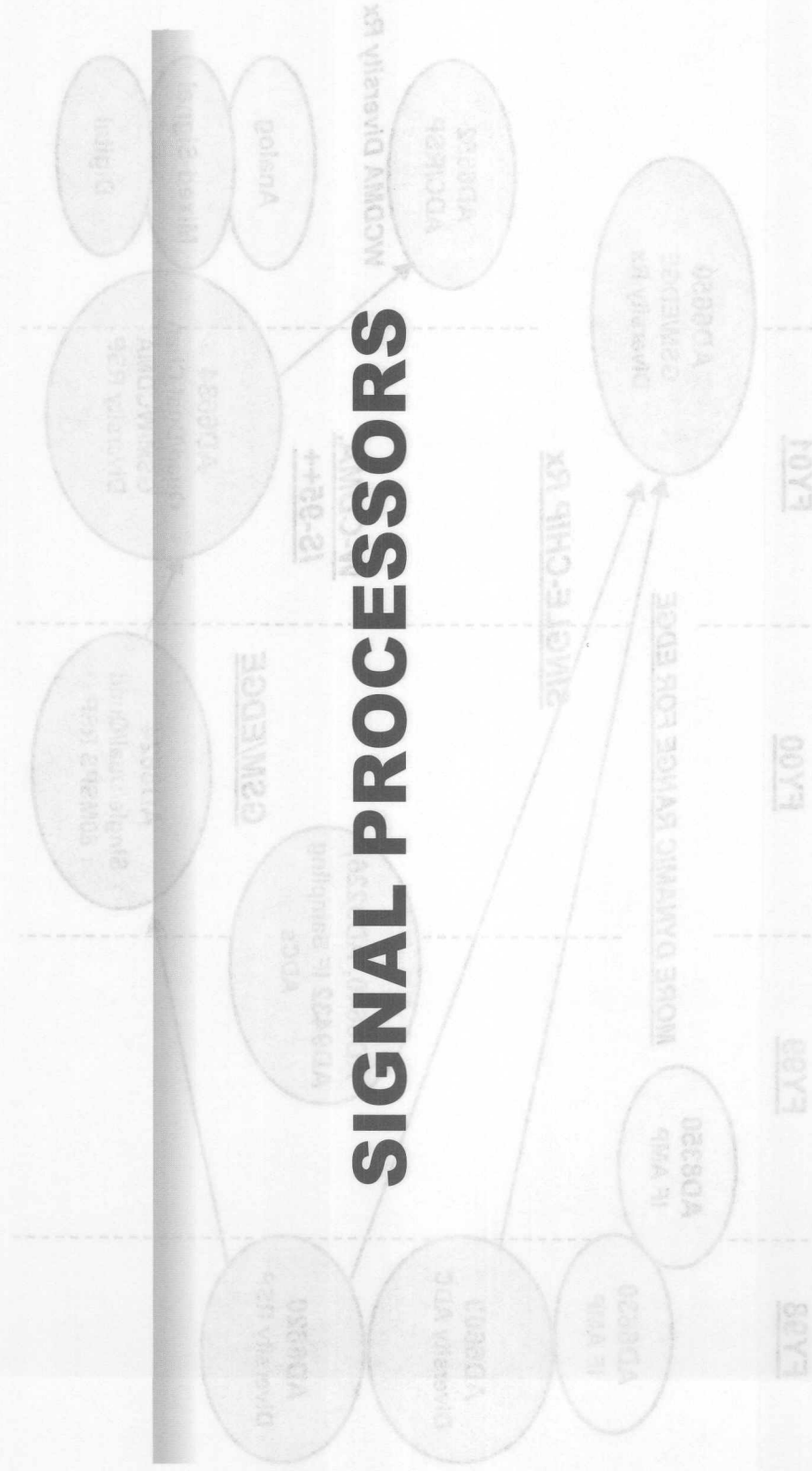
AD8353 - 20dB

P1 dB	9 dBm
OIP3	23 dBm
NF	5 dB
I _{SUPPLY}	41 mA



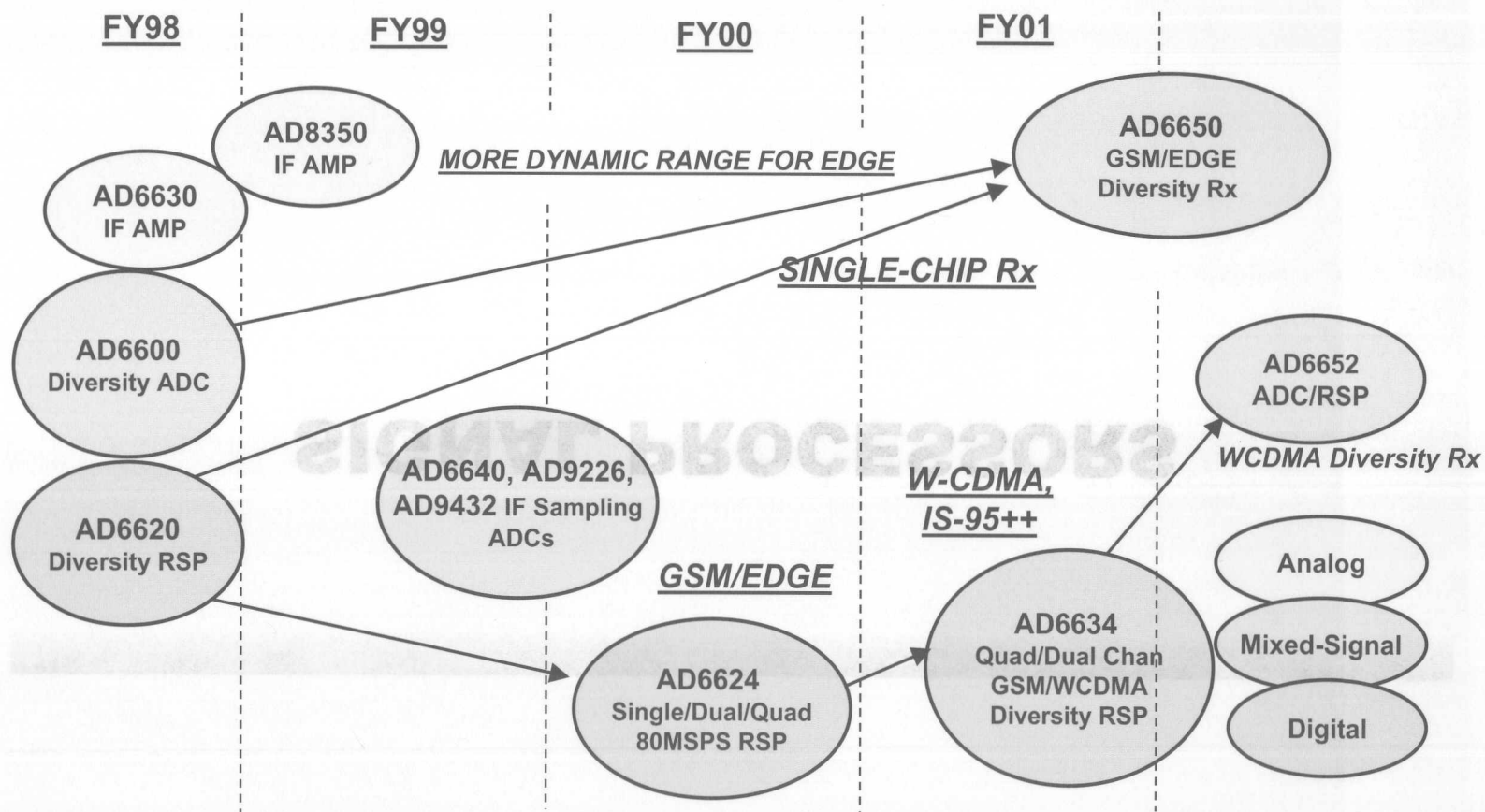
AD8354 - 20 dB

P1 dB	5 dBm
OIP3	19 dBm
NF	4 dB
I _{SUPPLY}	23 mA

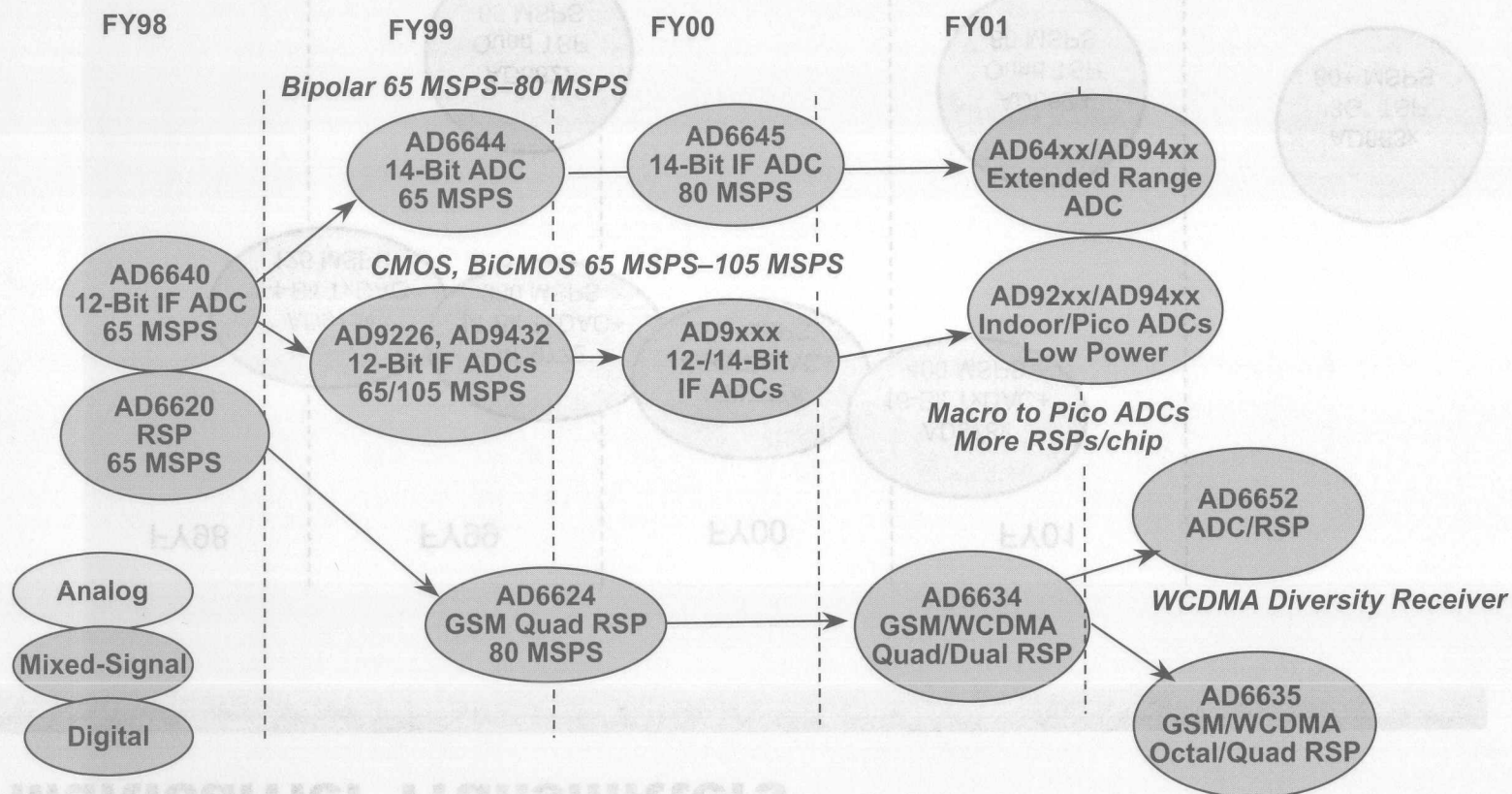


Single Carrier Receivers

Single Carrier Receivers



Multicarrier Receivers



Multicarrier Transmitters

FY98

AD9754
14-Bit TxDAC
125 MSPS

FY99

AD9772
14-Bit TxDAC+
300 MSPS

AD6622
Quad TSP
65 MSPS

FY00

AD9772A
14-Bit TxDAC+
300 MSPS

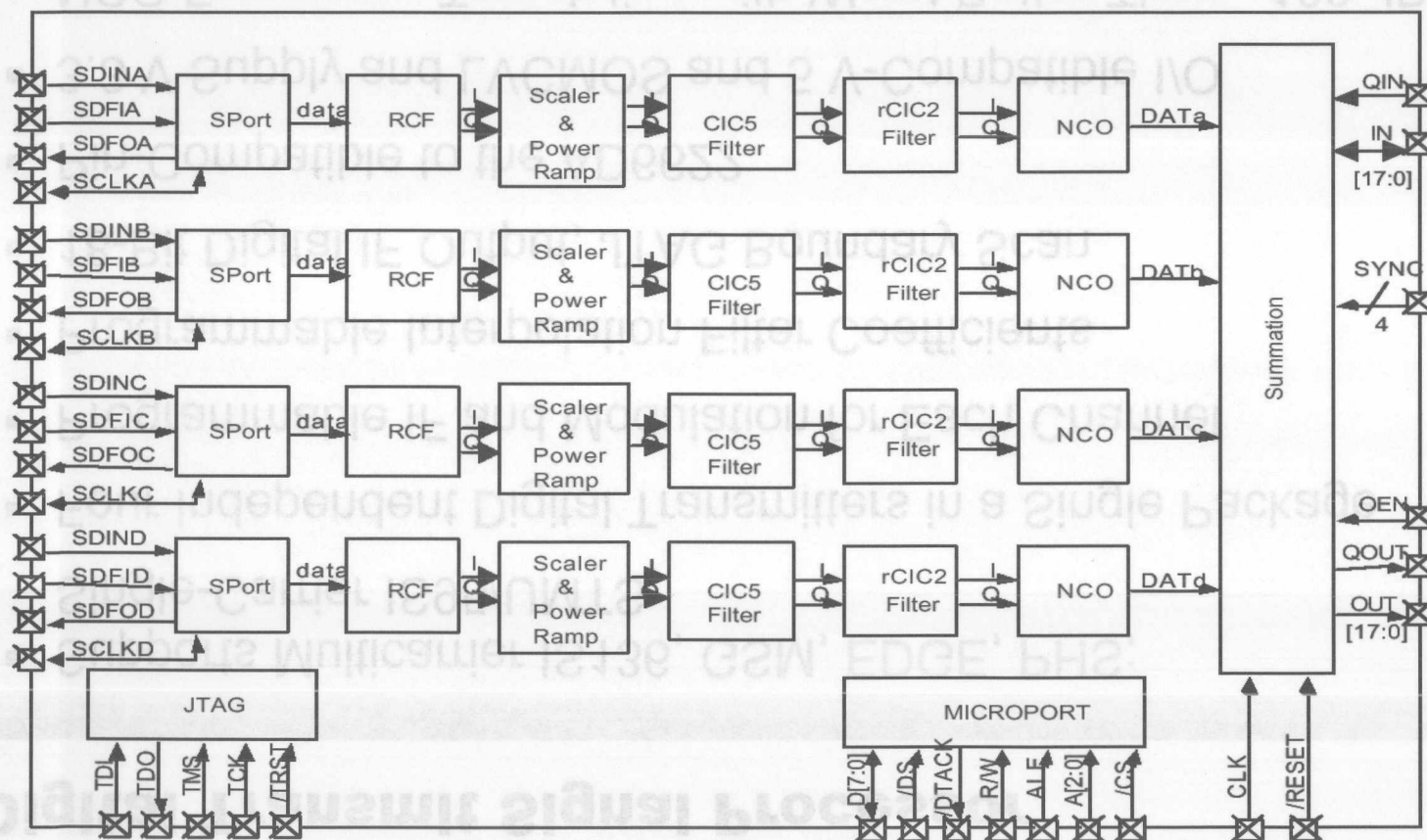
FY01

AD978x
16-Bit TxDAC+
400 MSPS

AD6623
Quad TSP
80 MSPS

AD663x
"3G" TSP
80+ MSPS

AD6623 4-Channel 104 MSPS Digital Transmit Signal Processor



AD6623 4-Channel 104 MSPS Digital Transmit Signal Processor

Supports Multicarrier IS136, GSM, EDGE, PHS;
Single-Carrier IS95/UMTS

Four Independent Digital Transmitters in a Single Package

Programmable IF and Modulation for Each Channel

Programmable Interpolation Filter Coefficients

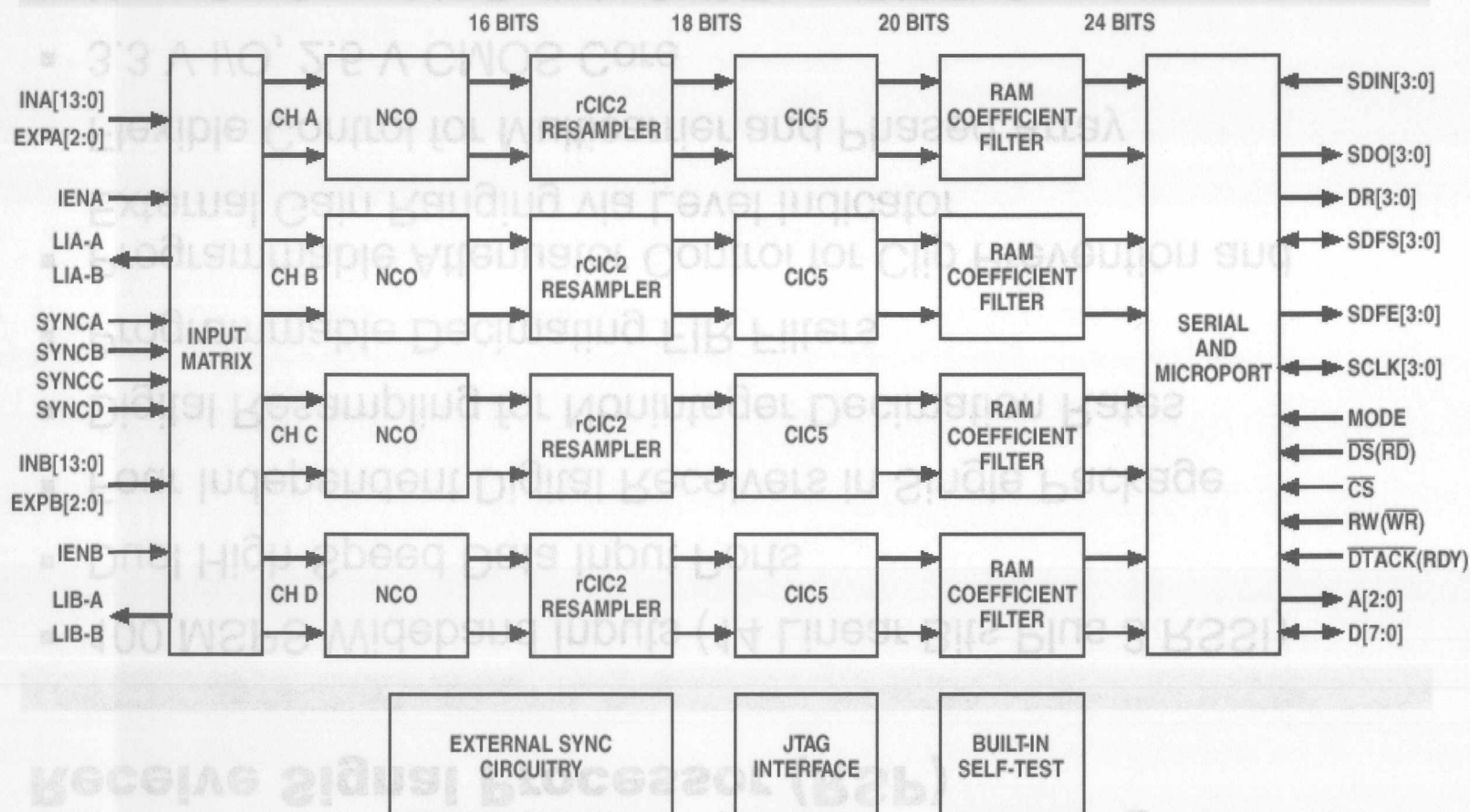
18-Bit Digital IF Output, JTAG Boundary Scan

Pin-Compatible to the AD6622

3.3 V Supply and LVCMOS and 5 V-Compatible I/O

VCO Frequency Translation with Worst Better Than -100 dBc

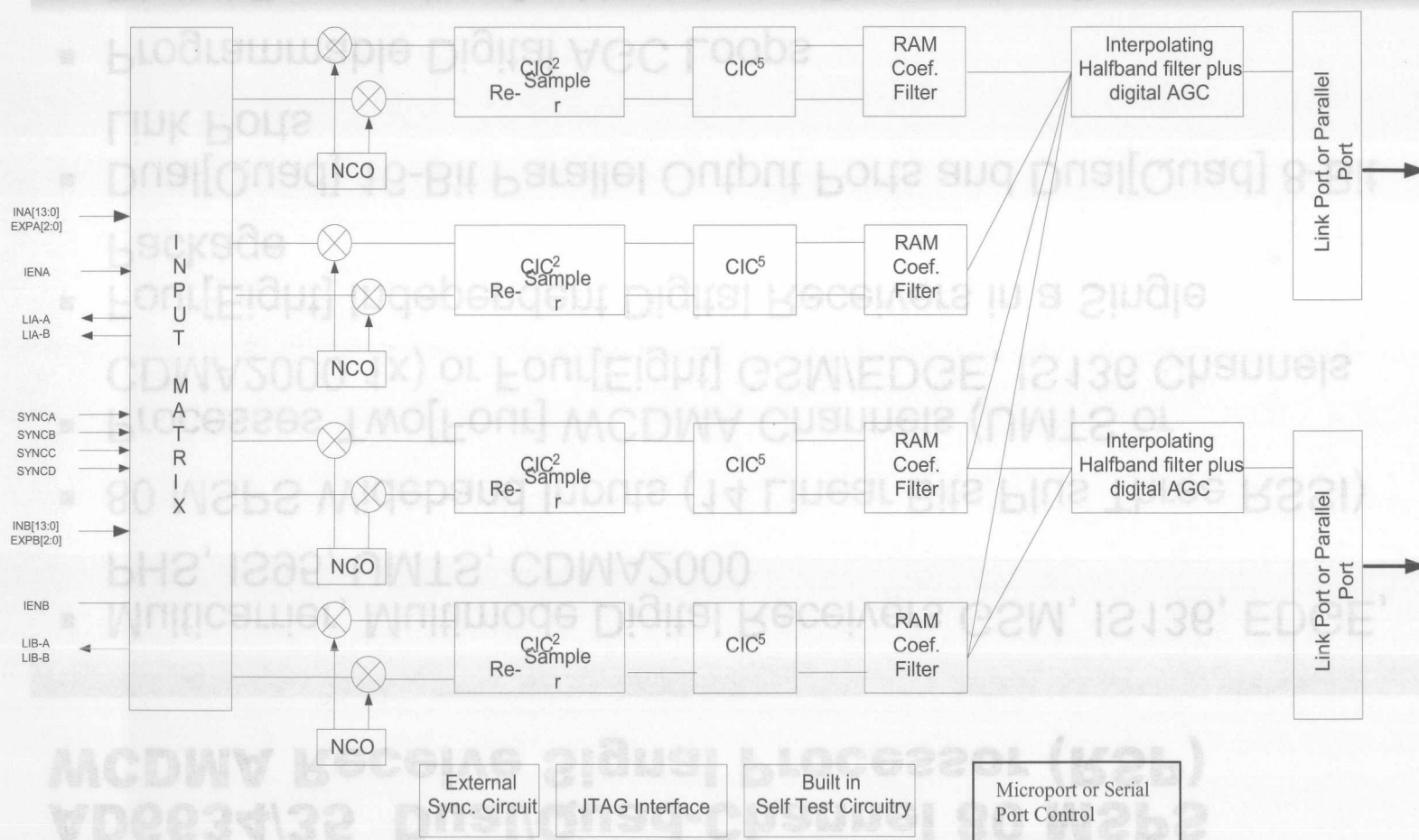
AD6624A Four-Channel, 100 MSPS Digital Receive Signal Processor (RSP)



AD6624A Four-Channel, 100 MSPS Digital Receive Signal Processor (RSP)

- 100 MSPS Wideband Inputs (14 Linear Bits Plus 3 RSSI)
- Dual High-Speed Data Input Ports
- Four Independent Digital Receivers in Single Package
- Digital Resampling for Noninteger Decimation Rates
- Programmable Decimating FIR Filters
- Programmable Attenuator Control for Clip Prevention and External Gain Ranging via Level Indicator
- Flexible Control for Multicarrier and Phased Array
- 3.3 V I/O, 2.5 V CMOS Core
- User-Configurable Built-In Self-Test (BIST) Capability
- JTAG Boundary Scan

AD6634/35 Dual/Quad-Channel 80 MSPS WCDMA Receive Signal Processor (RSP)



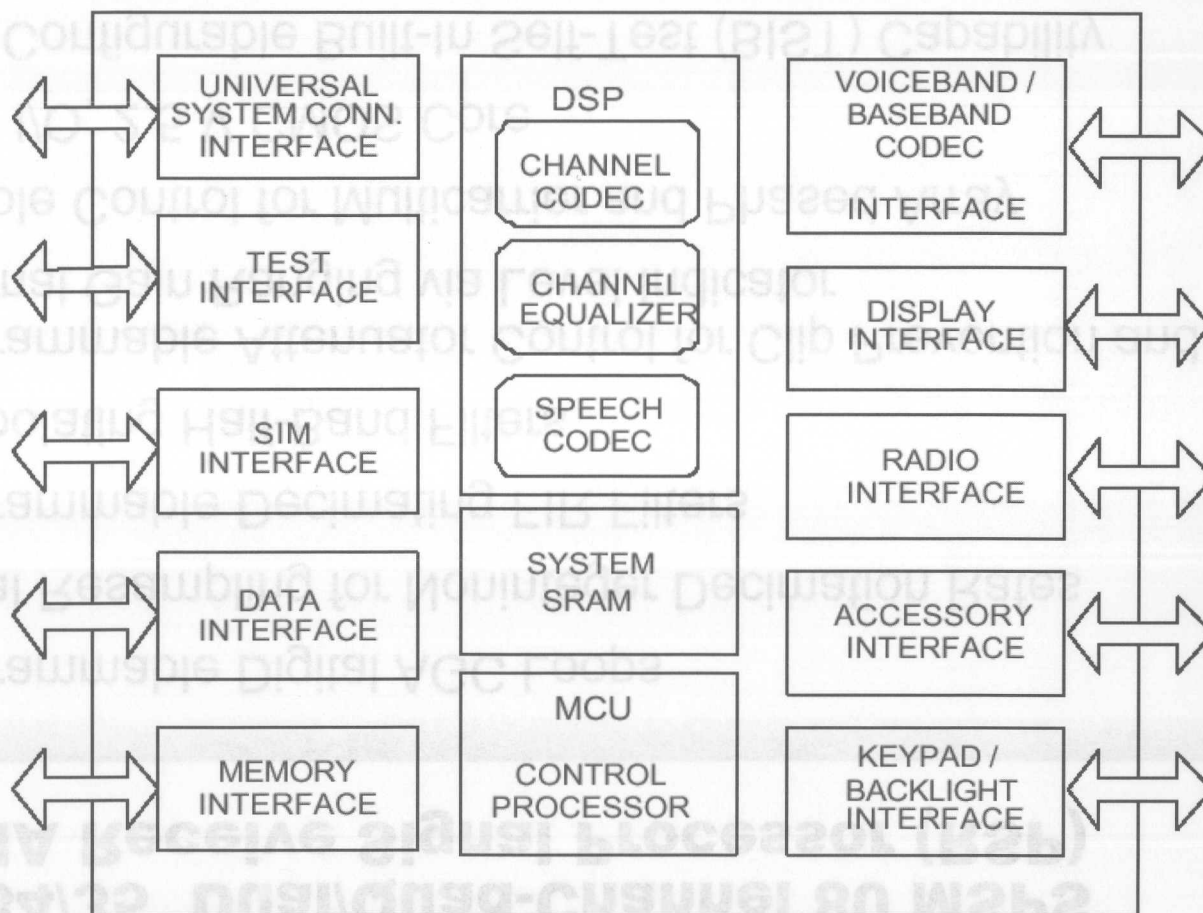
AD6634/35 Dual/Quad-Channel 80 MSPS WCDMA Receive Signal Processor (RSP)

- Multicarrier, Multimode Digital Receivers GSM, IS136, EDGE, PHS, IS95, UMTS, CDMA2000
- 80 MSPS Wideband Inputs (14 Linear Bits Plus Three RSSI)
- Processes Two[Four] WCDMA Channels (UMTS or CDMA2000 1x) or Four[Eight] GSM/EDGE, IS136 Channels
- Four[Eight] Independent Digital Receivers in a Single Package
- Dual[Quad] 16-Bit Parallel Output Ports and Dual[Quad] 8-Bit Link Ports
- Programmable Digital AGC Loops
- Digital Resampling for Noninteger Decimation Rates

AD6634/35 Dual/Quad-Channel 80 MSPS WCDMA Receive Signal Processor (RSP)

- Programmable Digital AGC Loops
- Digital Resampling for Noninteger Decimation Rates
- Programmable Decimating FIR Filters
- Interpolating Half-Band Filters
- Programmable Attenuator Control for Clip Prevention and External Gain Ranging via Level Indicator
- Flexible Control for Multicarrier and Phased Array
- 3.3 V I/O, 2.5 V CMOS Core
- User Configurable Built-In Self-Test (BIST) Capability
- JTAG Boundary Scan

AD6526 GSM/ GPRS Digital Baseband Processor



AD6526 GSM/ GPRS Digital Baseband Processor

- Complete Single Chip Programmable Digital Baseband Processor divided into three main subsystems:
 - Control Processor Subsystem including:
 - 32-bit MCU ARM7TDMI® Control Processor
 - On-chip Zero-wait-state System SRAM
 - DSP Subsystem including
 - 16-bit Fixed Point DSP Processor
 - Data and Program SRAM
 - Program Instruction Cache
 - Full Rate, Enhanced Full Rate and Half Rate
 - Speech Encoding/Decoding

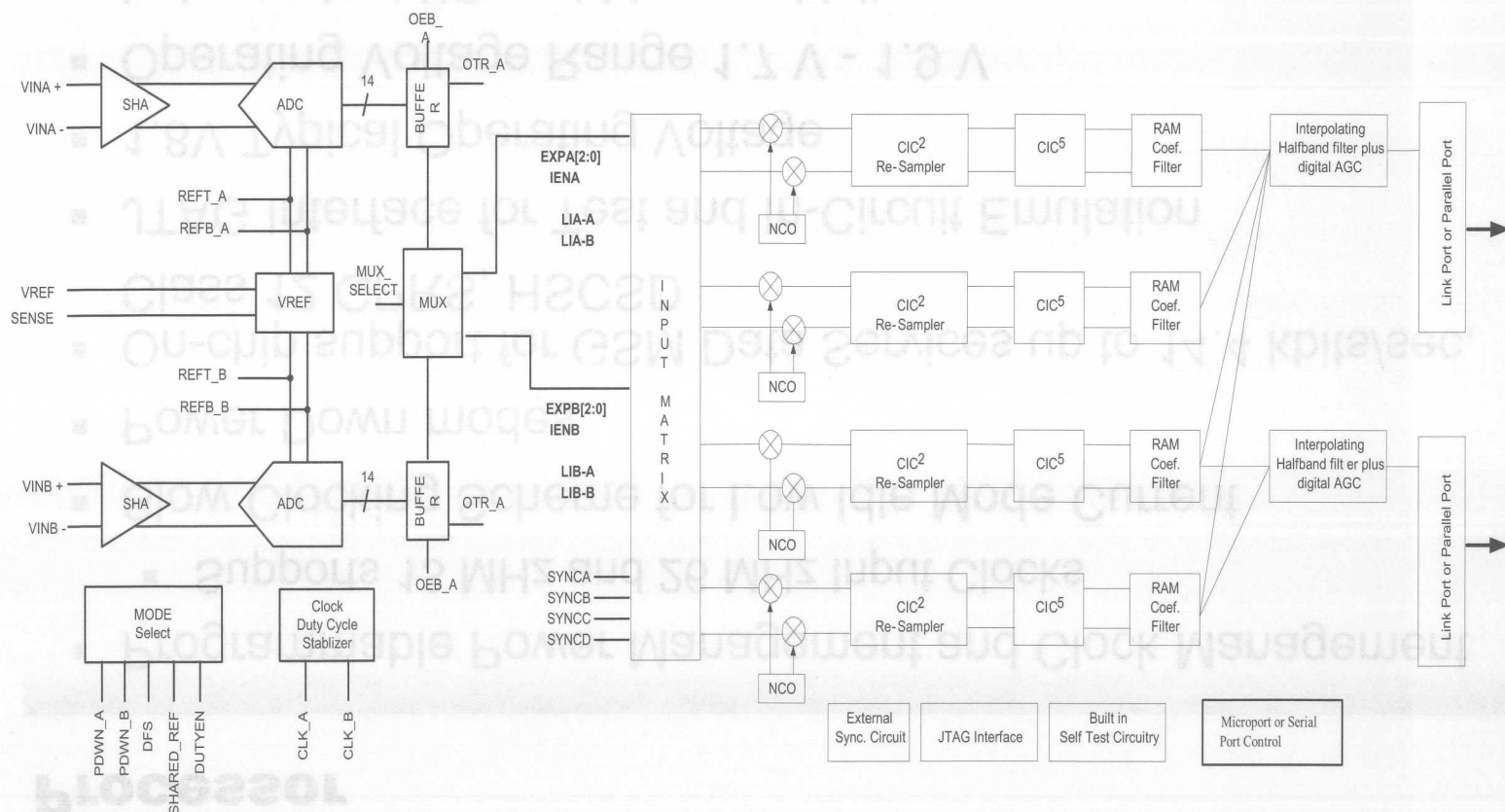
AD6526 GSM/ GPRS Digital Baseband Processor

- Peripheral Subsystem including
 - Shared Peripheral Bus and Interface Peripherals
 - Peripheral Functions
 - Parallel and Serial Display Interface
 - Keypad Interface
 - FLASH Memory Interface
 - 1.8 V and 3.0 V, 64 kbps SIM Interface
 - Universal System Connector Interface
 - Baseband Converter Interface
 - Data Services Interface
- Control of Radio Subsystem
- Three independent programmable backlight outputs
- Real Time Clock with Alarm

AD6526 GSM/ GPRS Digital Baseband Processor

- Programmable Power Management and Clock Management
 - Supports 13 MHz and 26 MHz Input Clocks
- Slow Clocking Scheme for Low Idle Mode Current
- Power Down modes
- On-chip support for GSM Data Services up to 14.4 kbits/sec, Class 12 GPRS, HSCSD
- JTAG Interface for Test and In-Circuit Emulation
- 1.8V Typical Operating Voltage
- Operating Voltage Range 1.7 V - 1.9 V
- Independent I/O and Memory Voltages
- 160-Ball LFBGA (mini-BGA) package

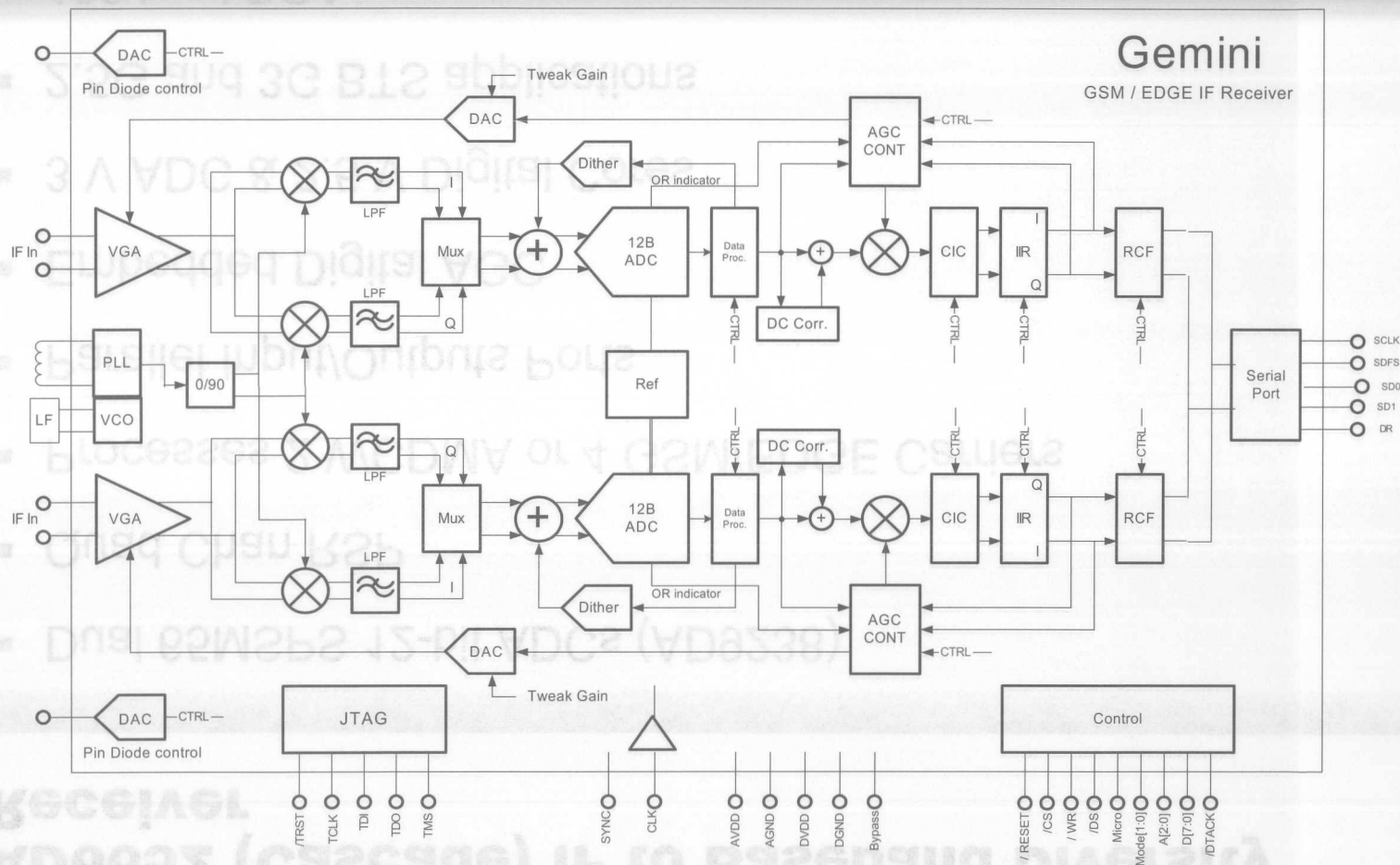
AD6652 (Cascade) IF to Baseband Diversity Receiver



AD6652 (Cascade) IF to Baseband Diversity Receiver

- Dual 65MSPS 12-bit ADCs (AD9238)
- Quad Chan RSP
- Processes 2 WCDMA or 4 GSM/EDGE Carriers
- Parallel Input/Outputs Ports
- Embedded Digital AGC
- 3 V ADC & 2.5 V Digital Cores
- 2.5G and 3G BTS applications
- 196 lead BGA

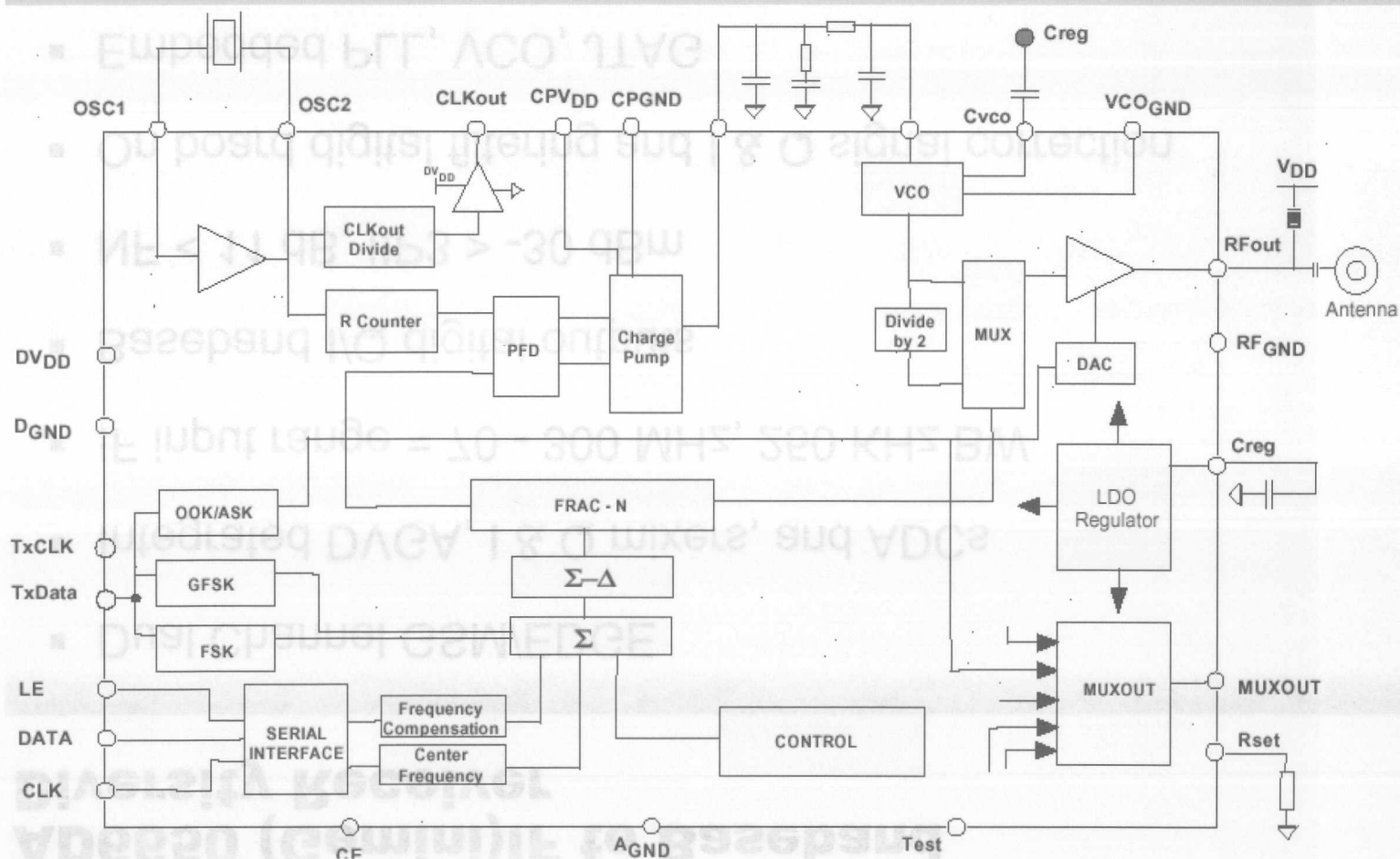
AD6650 (Gemini) IF to Baseband Diversity Receiver



AD6650 (Gemini) IF to Baseband Diversity Receiver

- Dual Channel GSM/EDGE
- Integrated DVGA, I & Q mixers, and ADCs
- IF input range = 70 - 300 MHz, 250 KHz BW
- Baseband I/Q digital outputs
- $NF < 11 \text{ dB}$, $IIP3 > -30 \text{ dBm}$
- On board digital filtering and I & Q signal correction
- Embedded PLL, VCO, JTAG

ADF7010 High Performance ISM Band ASK/ FSK/ GFSK Transmitter IC



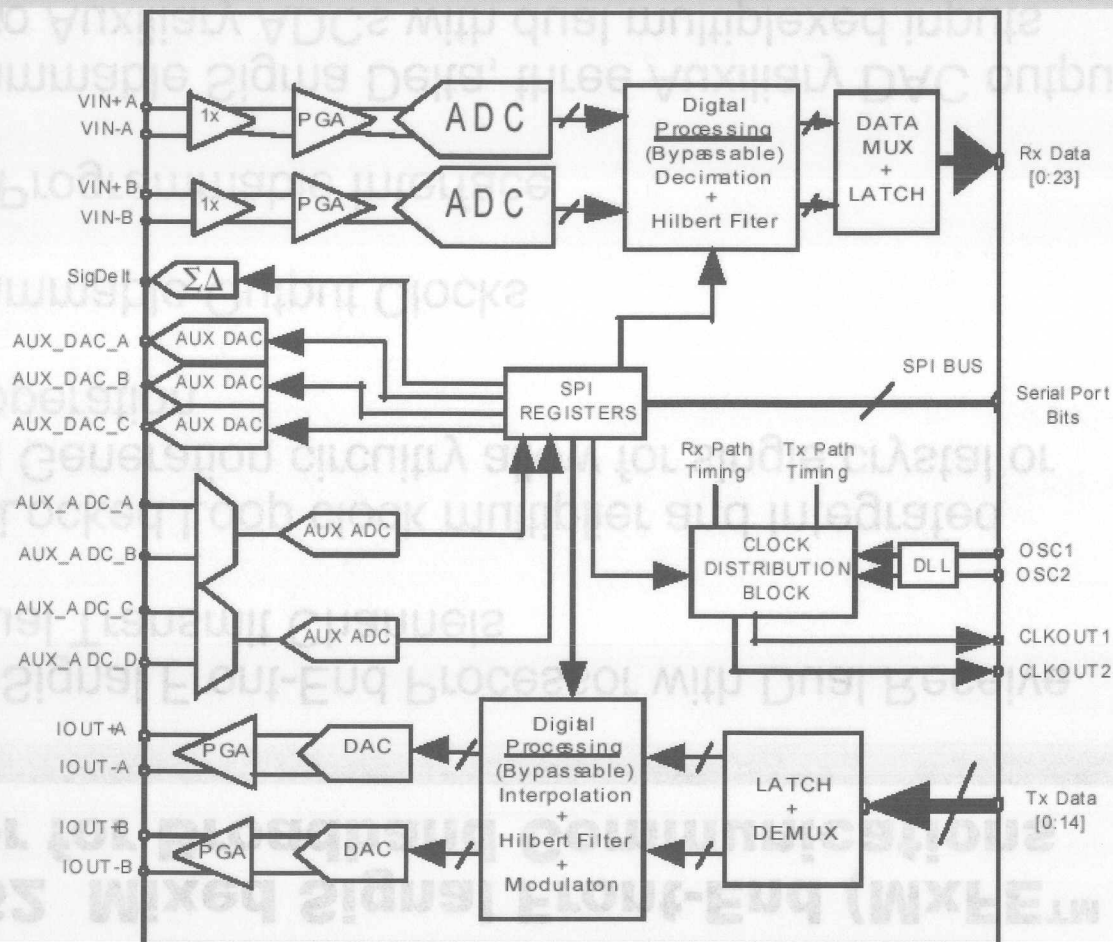
ADF7010 High Performance ISM Band ASK/ FSK/ GFSK Transmitter IC

- Single Chip Low Power Transmitter
- Frequency bands
 - 433-435 MHz
 - 866-870 MHz
 - 902-928 MHz
- Programmable Output Power
 - -20 to 10dBm
- On Chip VCO and Fractional-N PLL
- ± 1 ppm RF output accuracy possible from low-cost 100 ppm crystal
- FSK/ASK Data rates up to 64 kbits/s

ADF7010 High Performance ISM Band ASK/ FSK/ GFSK Transmitter IC

- +2.2 V to +3.6 V Power Supply
- Low Power consumption
 - 20 mA at 0 dBm Output
- Power Down Mode
- 24-pin TSSOP package
- Frequency range
- Single Chip Low Power Transmitter

AD9860/62 Mixed Signal Front-End (MxFE™) Processor for Broadband Communications



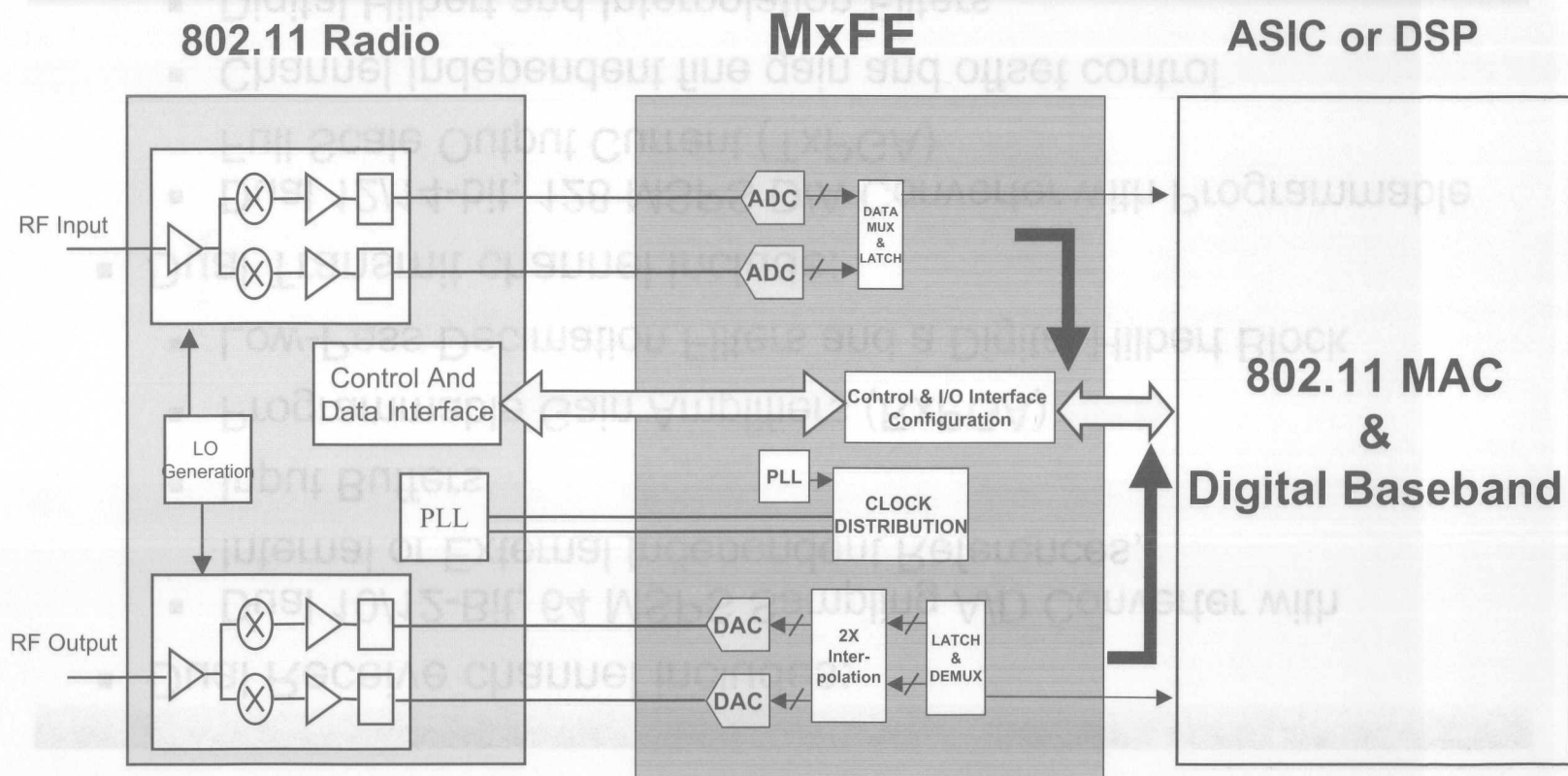
AD9860/62 Mixed Signal Front-End (MxFE™) Processor for Broadband Communications

- Mixed Signal Front-End Processor with Dual Receive and Dual Transmit Channels
- Delay-Locked Loop clock multiplier and Integrated Timing Generation circuitry allow for single crystal or clock operation
- Programmable Output Clocks
- Serial Programmable Interface
- Programmable Sigma Delta, three Auxiliary DAC outputs and two Auxiliary ADCs with dual multiplexed inputs

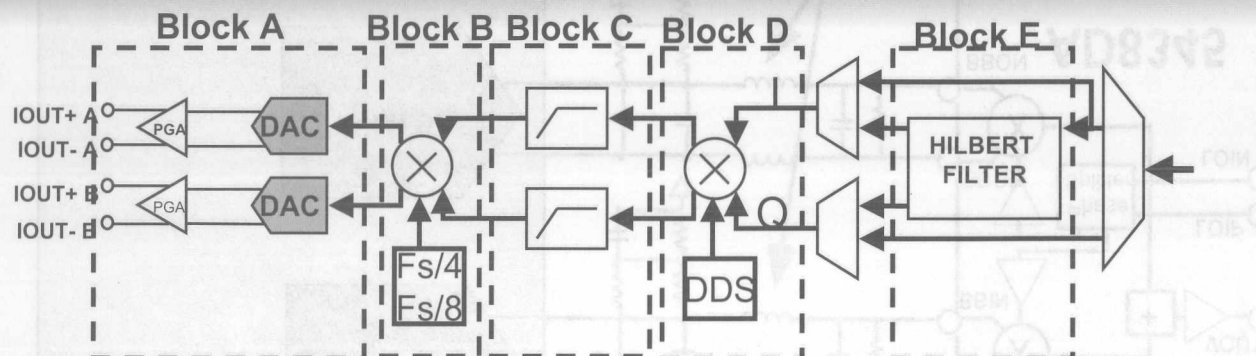
AD9860/62 Mixed Signal Front-End (MxFE™) Processor for Broadband Communications

- Dual Receive channel includes:
 - Dual 10/12-Bit, 64 MSPS Sampling A/D Converter with Internal or External Independent References,
 - Input Buffers
 - Programmable Gain Amplifiers (RxPGA)
 - Low-Pass Decimation Filters and a Digital Hilbert Block
- Dual Transmit channel include:
 - Dual 12/14-bit, 128 MSPS D/A Converter with Programmable Full Scale Output Current (TxPGA)
 - Channel Independent fine gain and offset control
 - Digital Hilbert and Interpolation Filters
 - Digital I/Q or Real-Signal Up-Converters
 - Coarse and Fine Digital Up-Converters

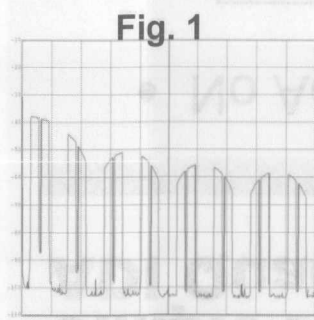
AD9860 Wireless LAN Application



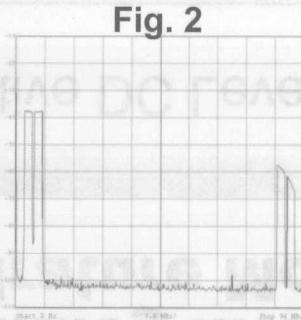
AD9860/2 MxFE™ Transmit Path



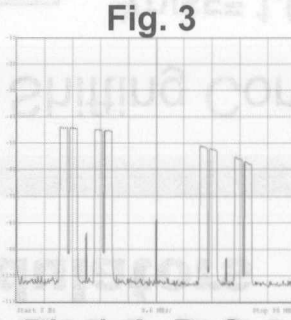
DAC output of OFDM signal using various AD9862 digital processing features:
 1.) 0 to 96 MHz spectrum of “Real” output, 2.) with 4x Interpolation, Block C,
 3.) with $F_s/4$ Up-conversion, Block B, 4.) with Hilbert Filter, Block E, enabled
 5.) Fine Tuned Modulation, Block D, enabled shifted by – 6MHz



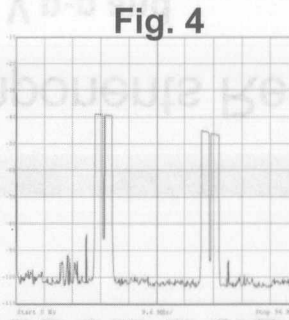
Block A



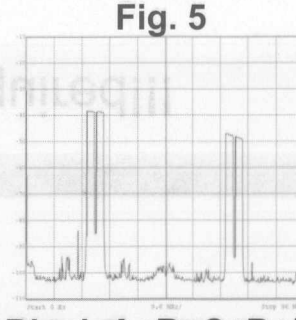
Block A+C



Block A+B+C



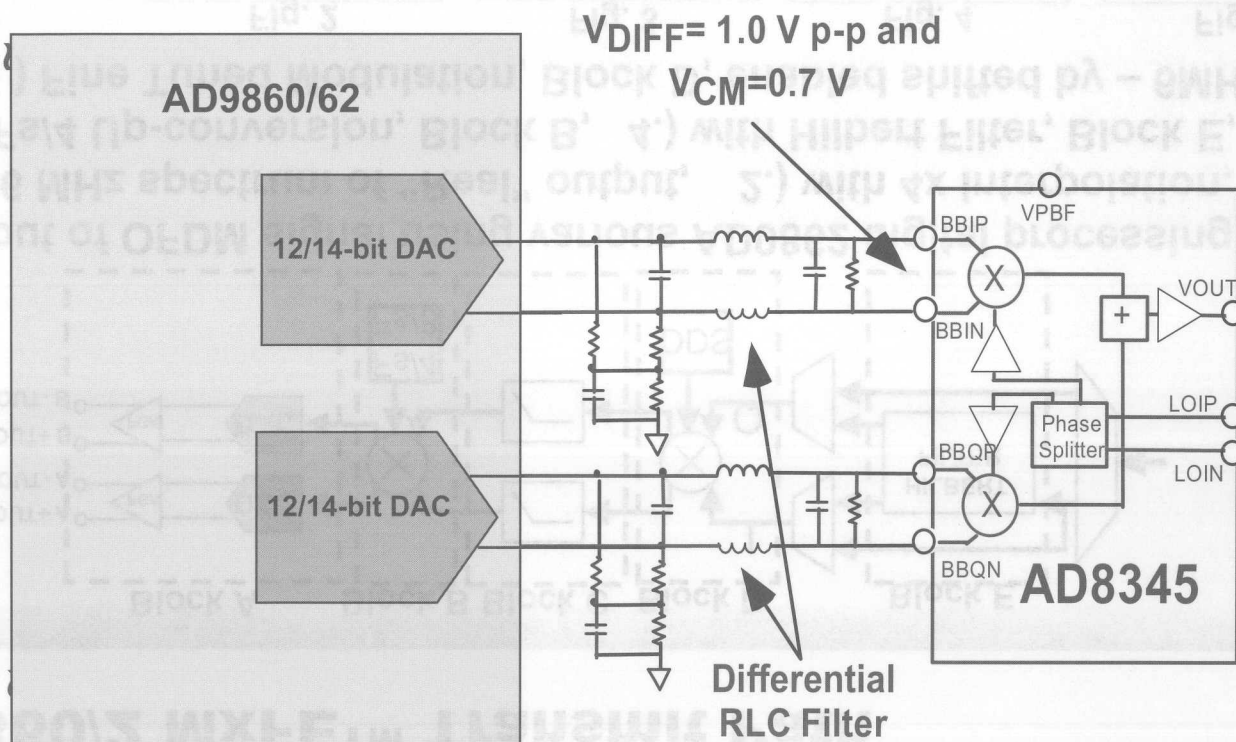
Block A+B+C+E



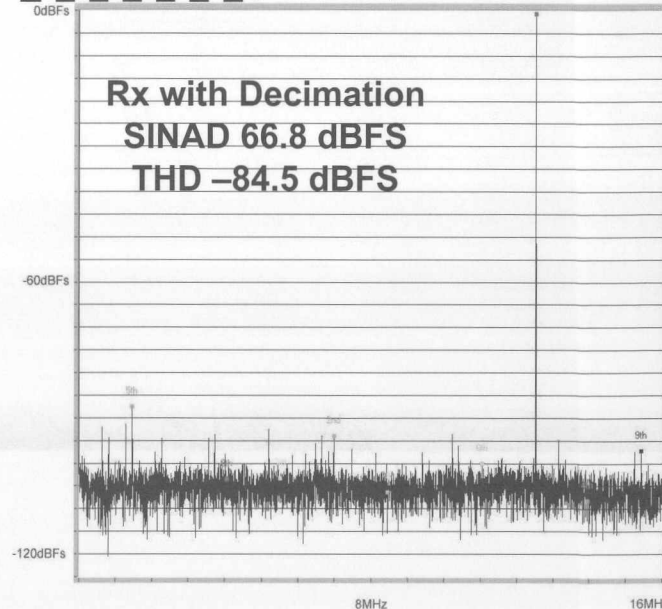
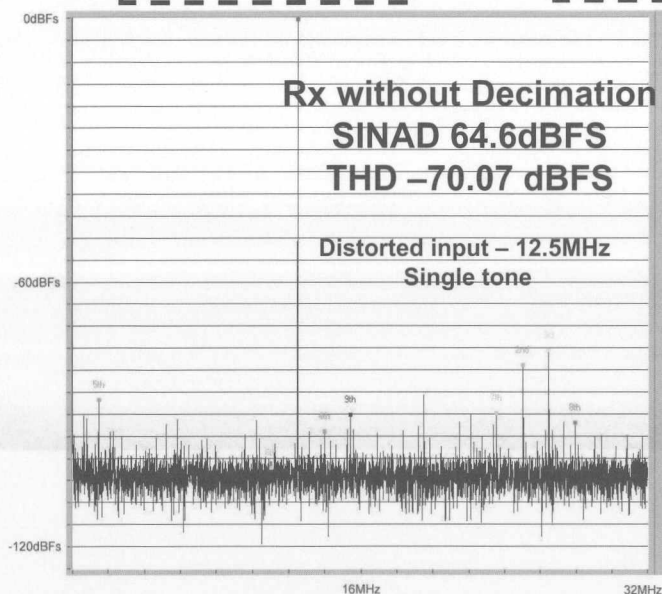
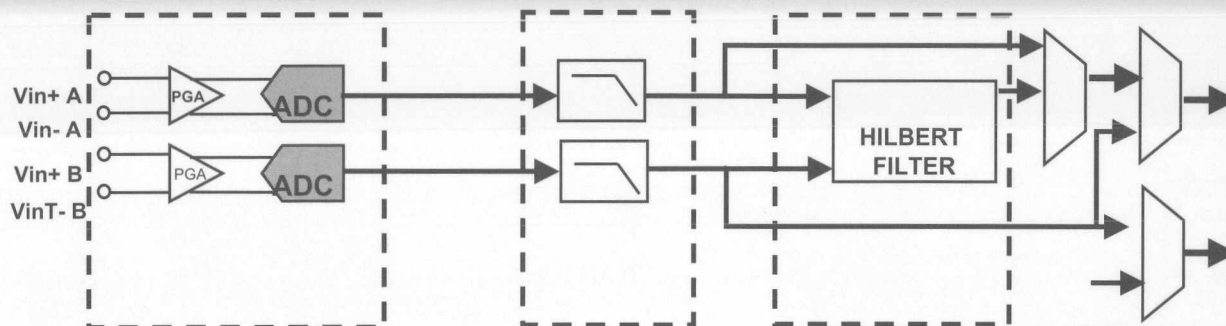
Block A+B+C+D+E

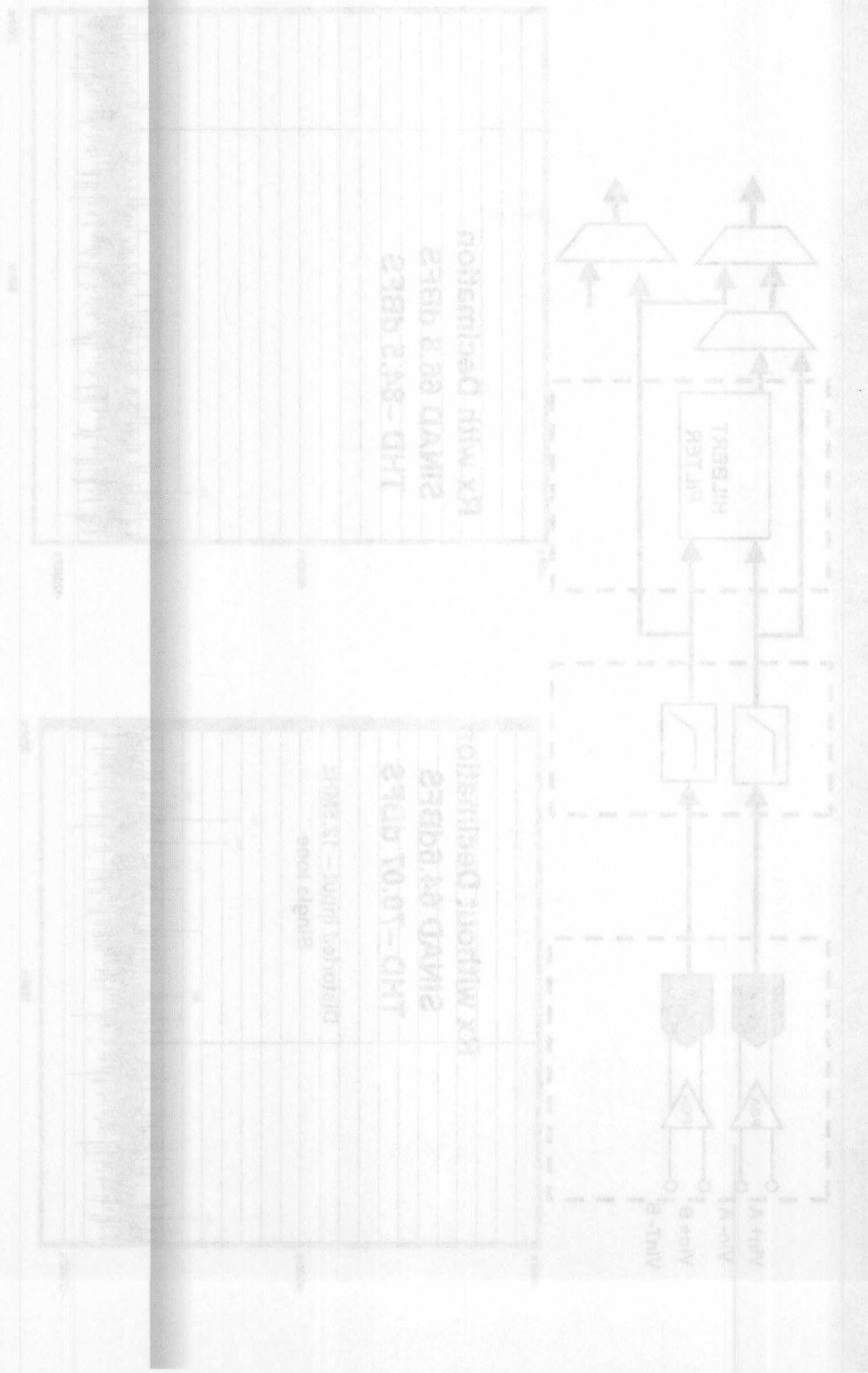
Simple Analog Interface Between TxDAC's and ADI Quadrature Modulators

- No Active DC Level Shifting Components Required!!!



AD9860/2 MxFE™ Receive Path





SECTION 9

FREQUENCY SYNTHESIS

DDS

PLL



www.analog.com

9-1

Direct Digital Synthesis

SECTION 9

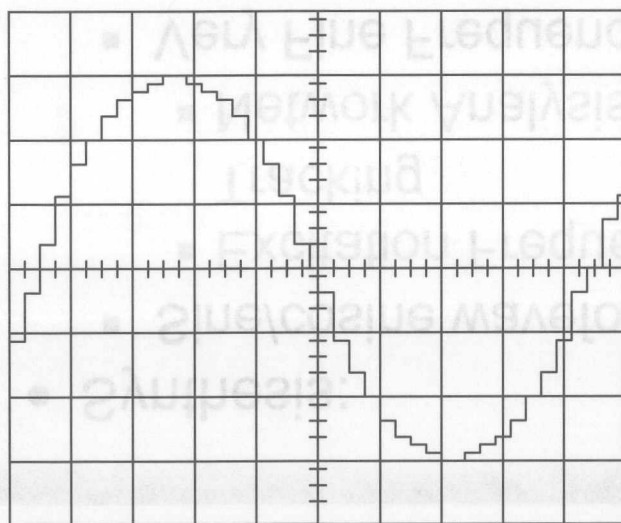


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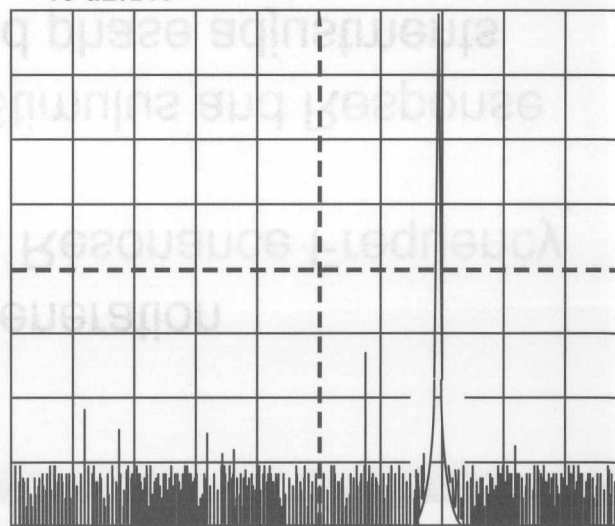
9-2

What is Direct Digital Synthesis?

Direct Digital Synthesis (DDS) is a technique that allows one to generate high-frequency, spectrally pure sinewaves of varying frequencies.



10 dB/DIV



Start : 0 Hz

Stop = 10 MHz

$f_{\text{CLOCK}} = 20 \text{ MHz}$ $f_{\text{OUT}} = 7 \text{ MHz}$

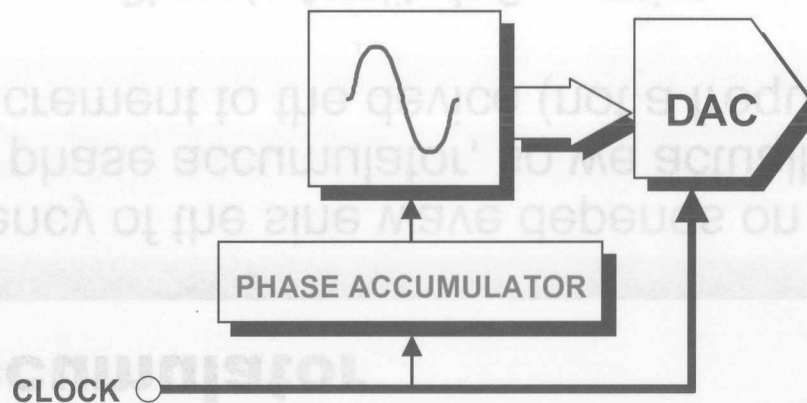
Where is Direct Digital Synthesis Used?

- Synthesis:
 - Sine/cosine waveform generation
 - Excitation Frequency, Resonance Frequency Tracking
 - Network Analysis.... Stimulus and Response
 - Very Fine Frequency and phase adjustments
- Modulation:
 - Quadrature: I and Q
 - Frequency
 - Phase
 - Amplitude

Basic Waveform Generator

- On Each Cycle of the Clock, the Phase Accumulator Is Incremented and the Desired Signal Amplitude Is Computed from the Resulting Phase, Which Yields a Sine Wave of Constant Frequency.
- But How Can We Vary the Output Frequency Without Having to Vary the Clock Speed?

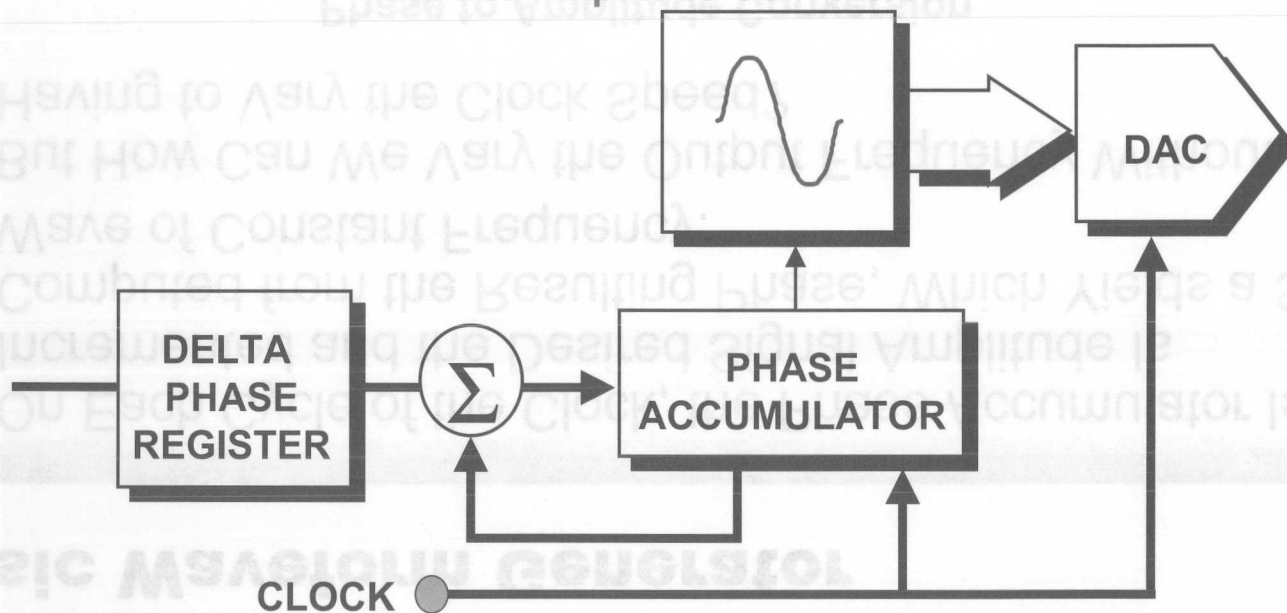
Phase to Amplitude Conversion



Phase Accumulator

The frequency of the sine wave depends on the step size of the phase accumulator, so we actually write a phase increment to the device (not a frequency).

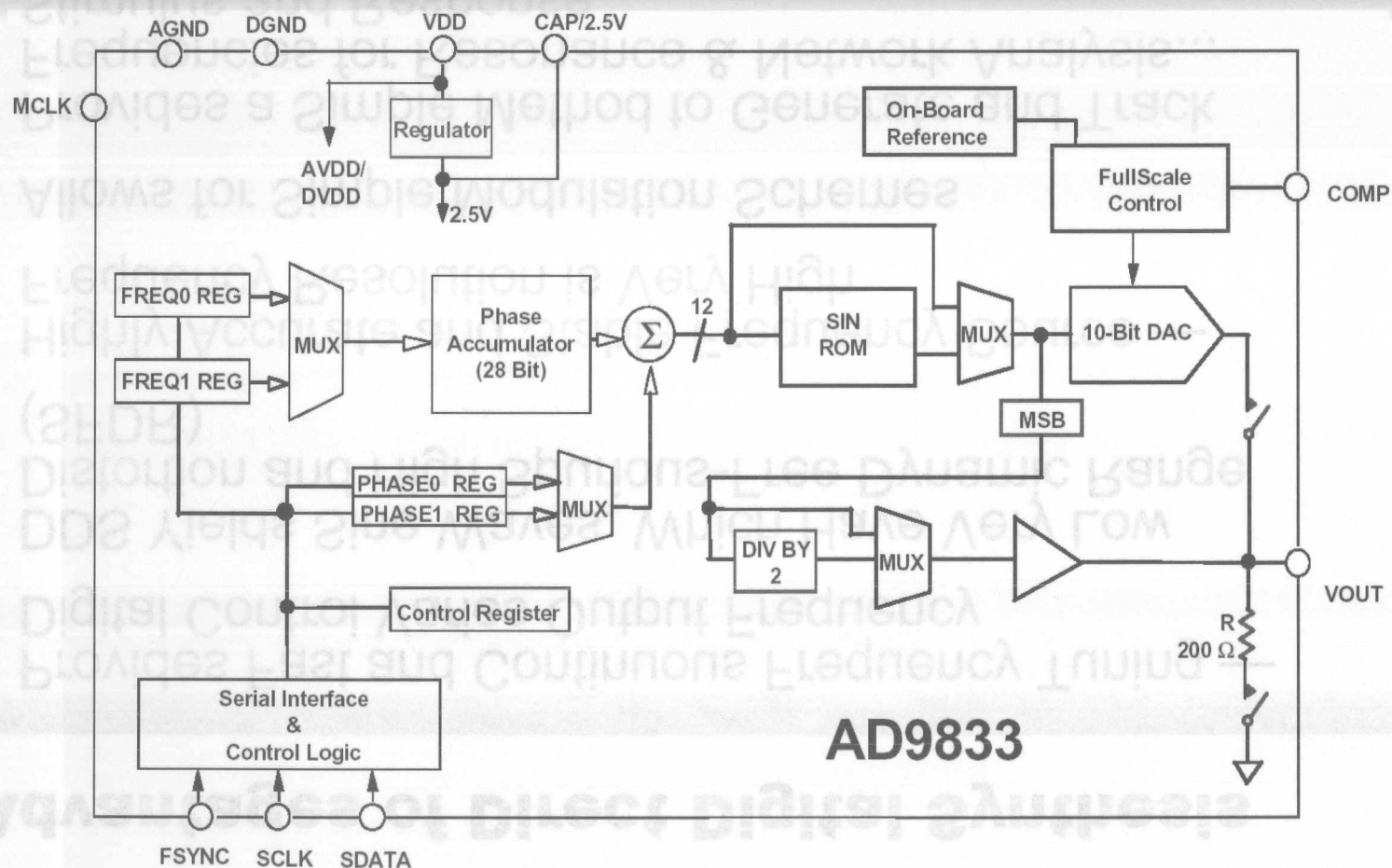
Phase to Amplitude Conversion



Advantages of Direct Digital Synthesis

- Provides Fast and Continuous Frequency Tuning — Digital Control Varies Output Frequency
- DDS Yields Sine Waves, Which Have Very Low Distortion and High Spurious-Free Dynamic Range (SFDR)
- Highly Accurate and Stable Frequency Source — Frequency Resolution is Very High
- Allows for Simple Modulation Schemes
- Provides a Simple Method to Generate and Track Frequencies for Resonance & Network Analysis... Stimulus and Response
- Can Provide Quadrature Frequency Outputs

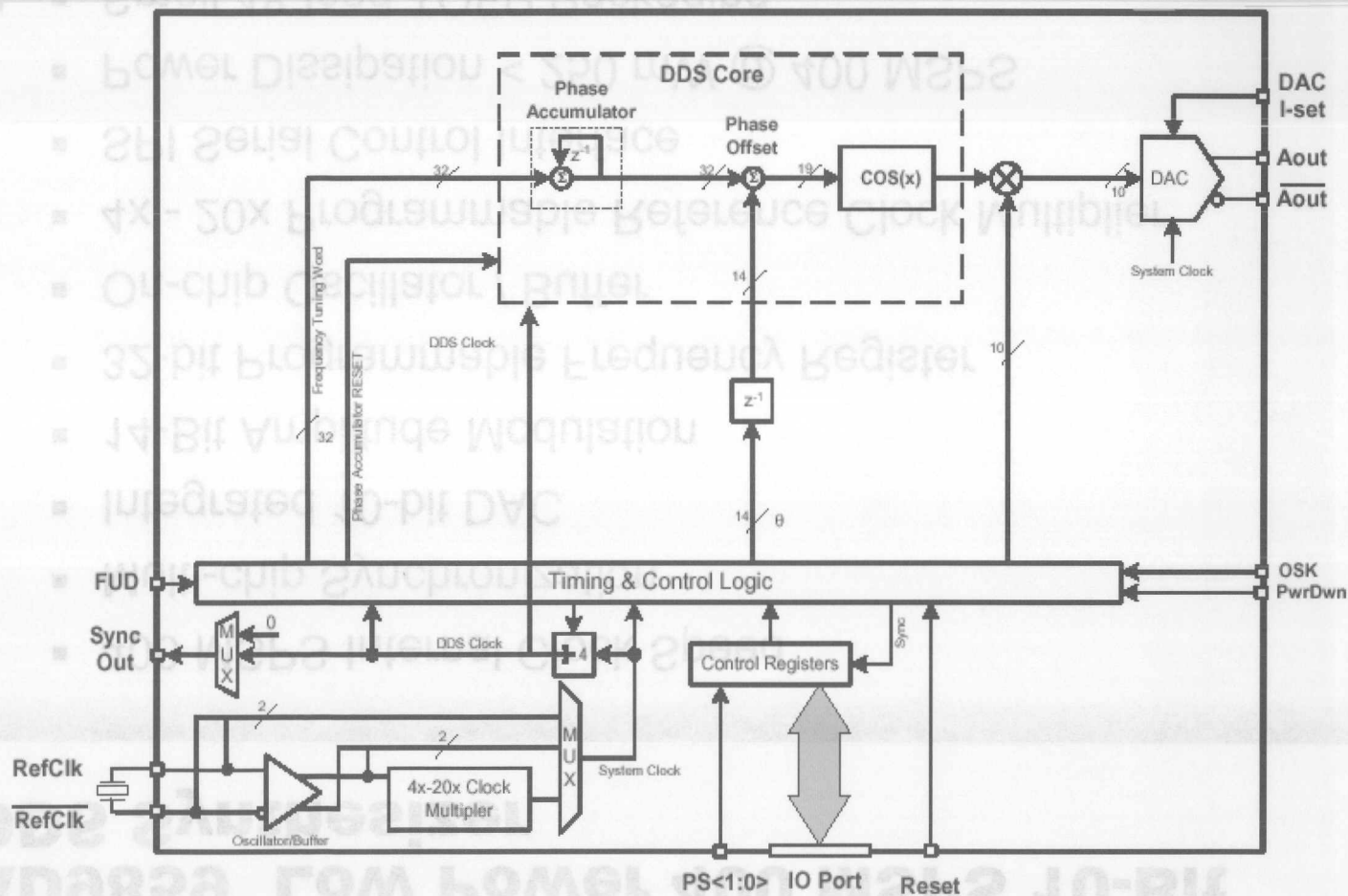
AD9833 Low Power (20mW) 25 MSPS Frequency Synthesizer



AD9833/34 Features

- Low Power (20-35mW)
- 10-Lead μ SOIC (AD9833) or 20-Lead TSSOP (AD9834)
- 10-Bit DAC
- 28-Bit Phase Accumulator
- 2.3 V to 5.5 V Operation
- Two Frequency Registers and Two-Phase Registers
- Low Jitter Clock Output
- Narrow Band SFDR >72 dB
- 40 Mhz Serial Interface

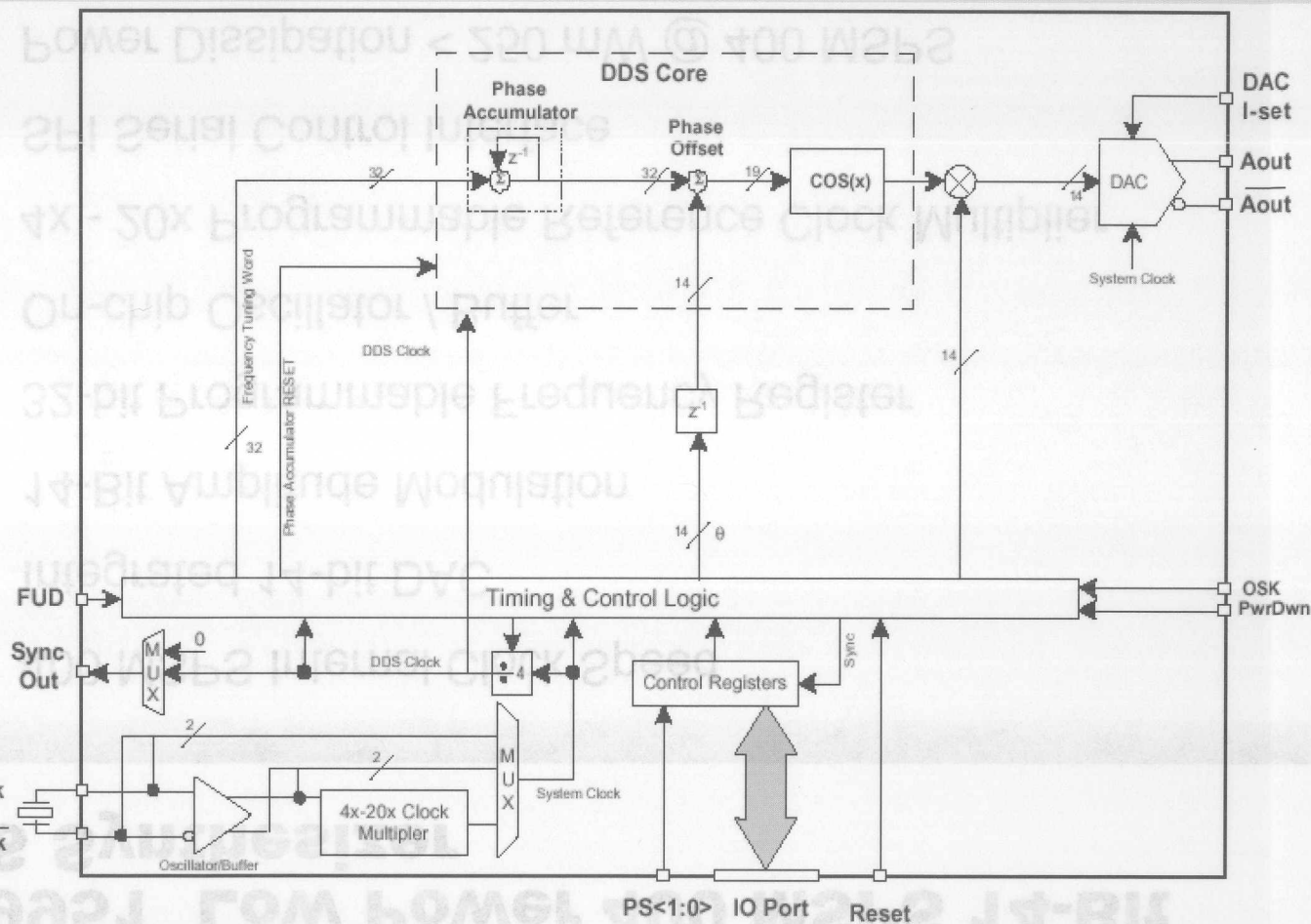
AD9859 Low Power 400 MSPS 10-Bit DDS Synthesizer



AD9859 Low Power 400 MSPS 10-Bit DDS Synthesizer

- 400 MSPS Internal Clock Speed
- Multi-chip Synchronization
- Integrated 10-bit DAC
- 14-Bit Amplitude Modulation
- 32-bit Programmable Frequency Register
- On-chip Oscillator / Buffer
- 4x - 20x Programmable Reference Clock Multiplier
- SPI Serial Control Interface
- Power Dissipation < 250 mW @ 400 MSPS
- Small 48-lead TQFP Packaging

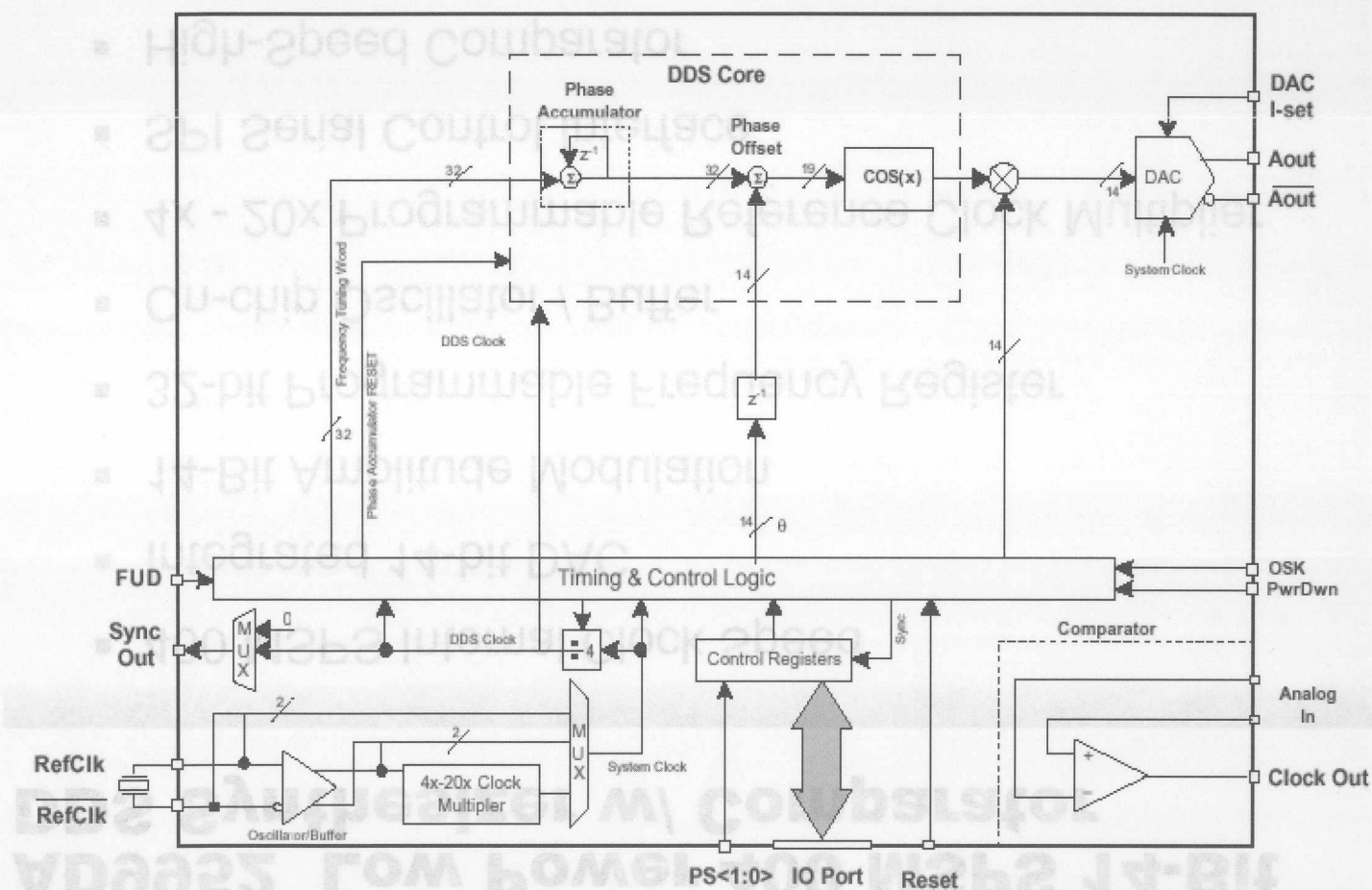
AD9951 Low Power 400 MSPS 14-Bit DDS Synthesizer



AD9951 Low Power 400 MSPS 14-Bit DDS Synthesizer

- 400 MSPS Internal Clock Speed
- Integrated 14-bit DAC
- 14-Bit Amplitude Modulation
- 32-bit Programmable Frequency Register
- On-chip Oscillator / Buffer
- 4x - 20x Programmable Reference Clock Multiplier
- SPI Serial Control Interface
- Power Dissipation < 250 mW @ 400 MSPS
- Small 48-lead TQFP Packaging

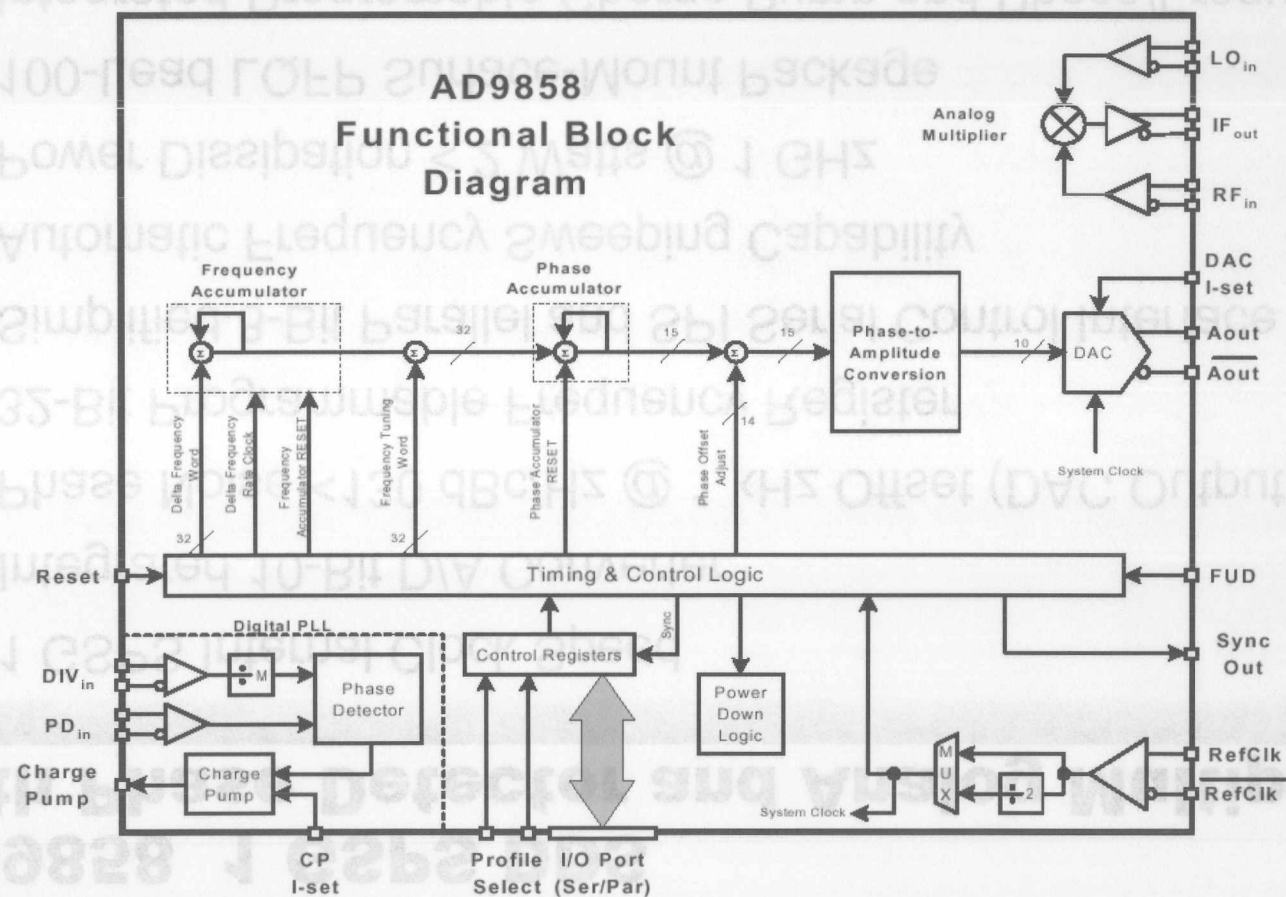
AD9952 Low Power 400 MSPS 14-Bit DDS Synthesizer w/ Comparator



AD9952 Low Power 400 MSPS 14-Bit DDS Synthesizer w/ Comparator

- 400 MSPS Internal Clock Speed
- Integrated 14-bit DAC
- 14-Bit Amplitude Modulation
- 32-bit Programmable Frequency Register
- On-chip Oscillator / Buffer
- 4x - 20x Programmable Reference Clock Multiplier
- SPI Serial Control Interface
- High-Speed Comparator
- Power Dissipation < 250 mW @ 400 MSPS
- Small 48-lead TQFP Packaging

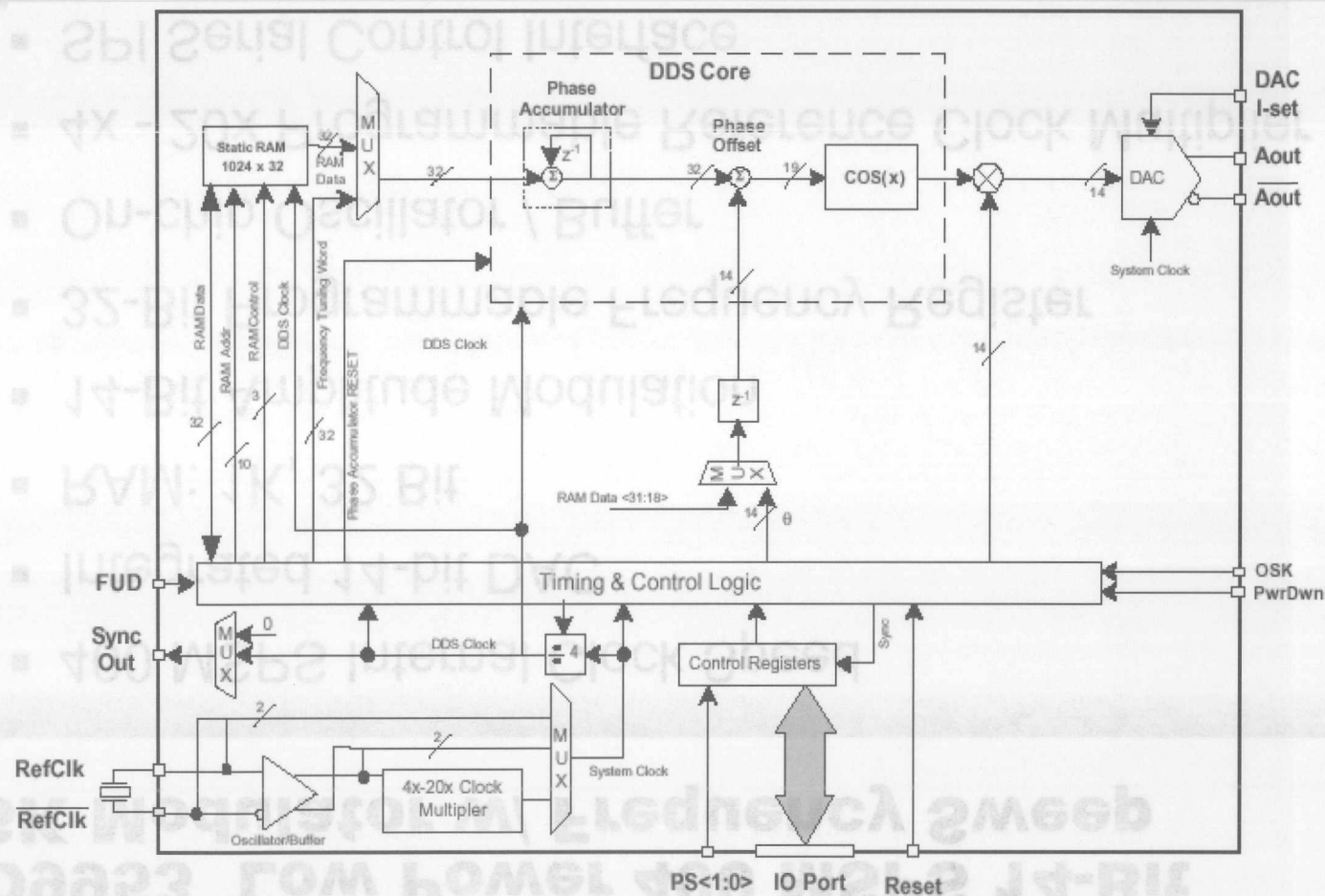
AD9858 1 GSPS DDS with Phase Detector and Analog Multiplier



AD9858 1 GSPS DDS with Phase Detector and Analog Multiplier

- 1 GSPS Internal Clock Speed
- Integrated 10-Bit D/A Converter
- Phase Noise < 130 dBc/Hz @ 1 kHz Offset (DAC Output)
- 32-Bit Programmable Frequency Register
- Simplified 8-Bit Parallel and SPI Serial Control Interface
- Automatic Frequency Sweeping Capability
- Power Dissipation < 2 Watts @ 1 GHz
- 100-Lead LQFP Surface-Mount Package
- Integrated Programable Charge Pump and Phase/Frequency Detector with Fast Lock Circuit
- Frequency Detector and Integrated Mixer

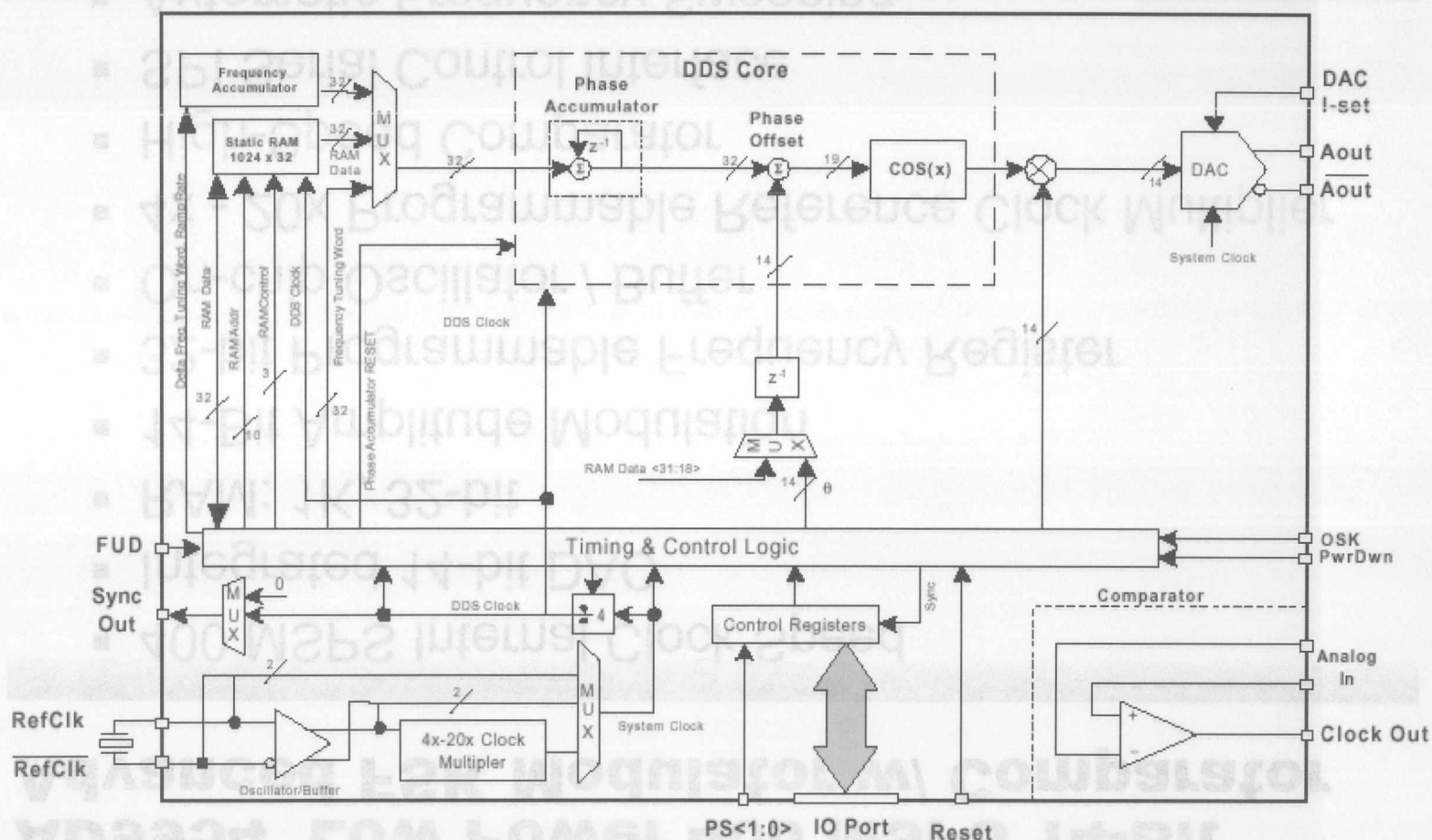
AD9953 Low Power 400 MSPS 14-Bit FSK Modulator w/ Frequency Sweep



AD9953 Low Power 400 MSPS 14-Bit FSK Modulator w/ Frequency Sweep

- 400 MSPS Internal Clock Speed
- Integrated 14-bit DAC
- RAM: 1K, 32 Bit
- 14-Bit Amplitude Modulation
- 32-Bit Programmable Frequency Register
- On-chip Oscillator / Buffer
- 4x - 20x Programmable Reference Clock Multiplier
- SPI Serial Control Interface
- Power Dissipation < 250 mW @ 400 MSPS
- Small 48-lead TQFP Packaging

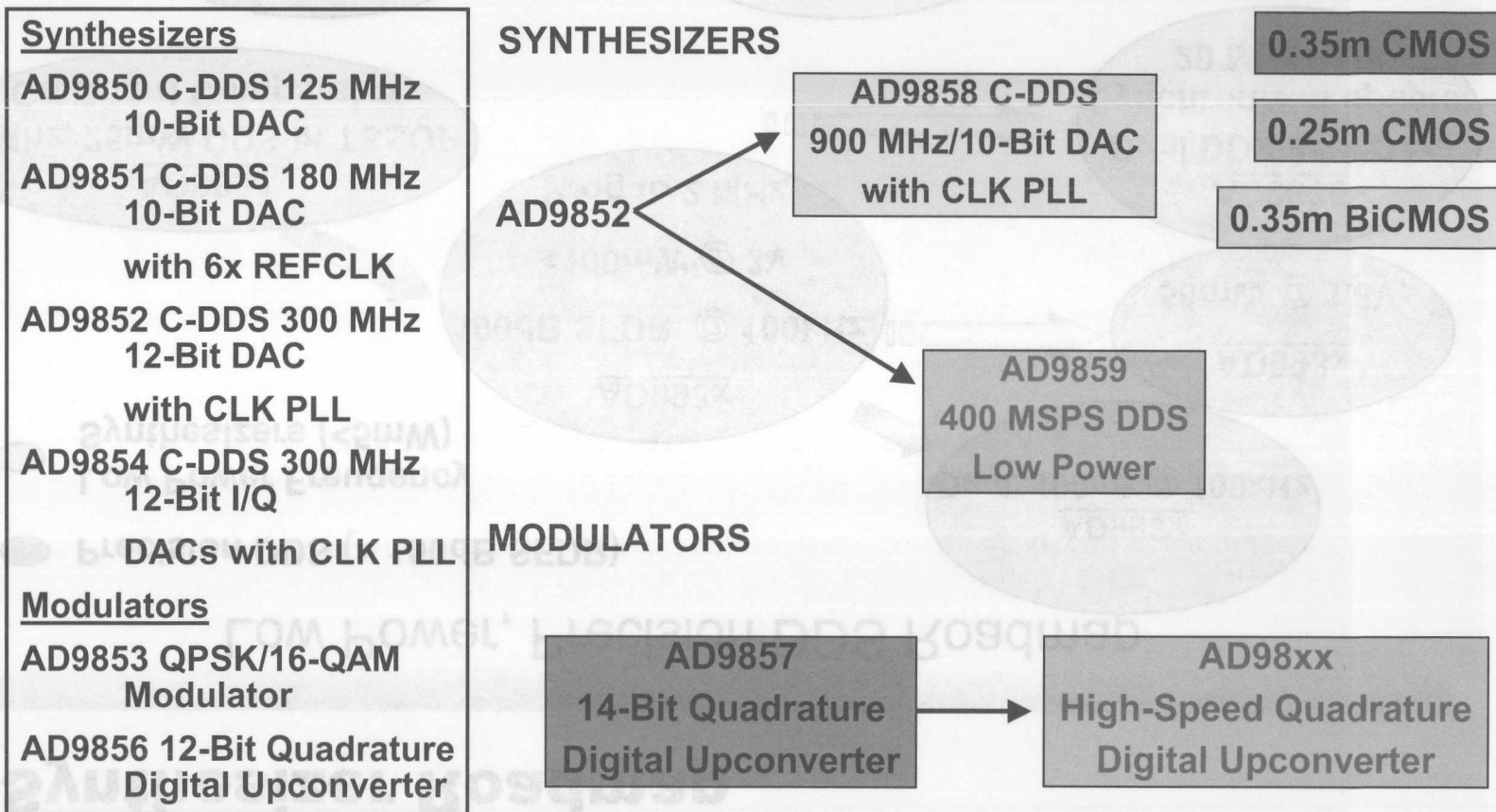
AD9954 Low Power 400 MSPS 14-Bit Advanced FSK Modulator w/ Comparator



AD9954 Low Power 400 MSPS 14-Bit Advanced FSK Modulator w/ Comparator

- 400 MSPS Internal Clock Speed
- Integrated 14-bit DAC
- RAM: 1K, 32-bit
- 14-Bit Amplitude Modulation
- 32-bit Programmable Frequency Register
- On-chip Oscillator / Buffer
- 4x - 20x Programmable Reference Clock Multiplier
- High-Speed Comparator
- SPI Serial Control Interface
- Automatic Frequency Sweeping
- Power Dissipation < 250 mW @ 400 MSPS
- Small 48-lead TQFP Packaging

DDS Product Roadmap



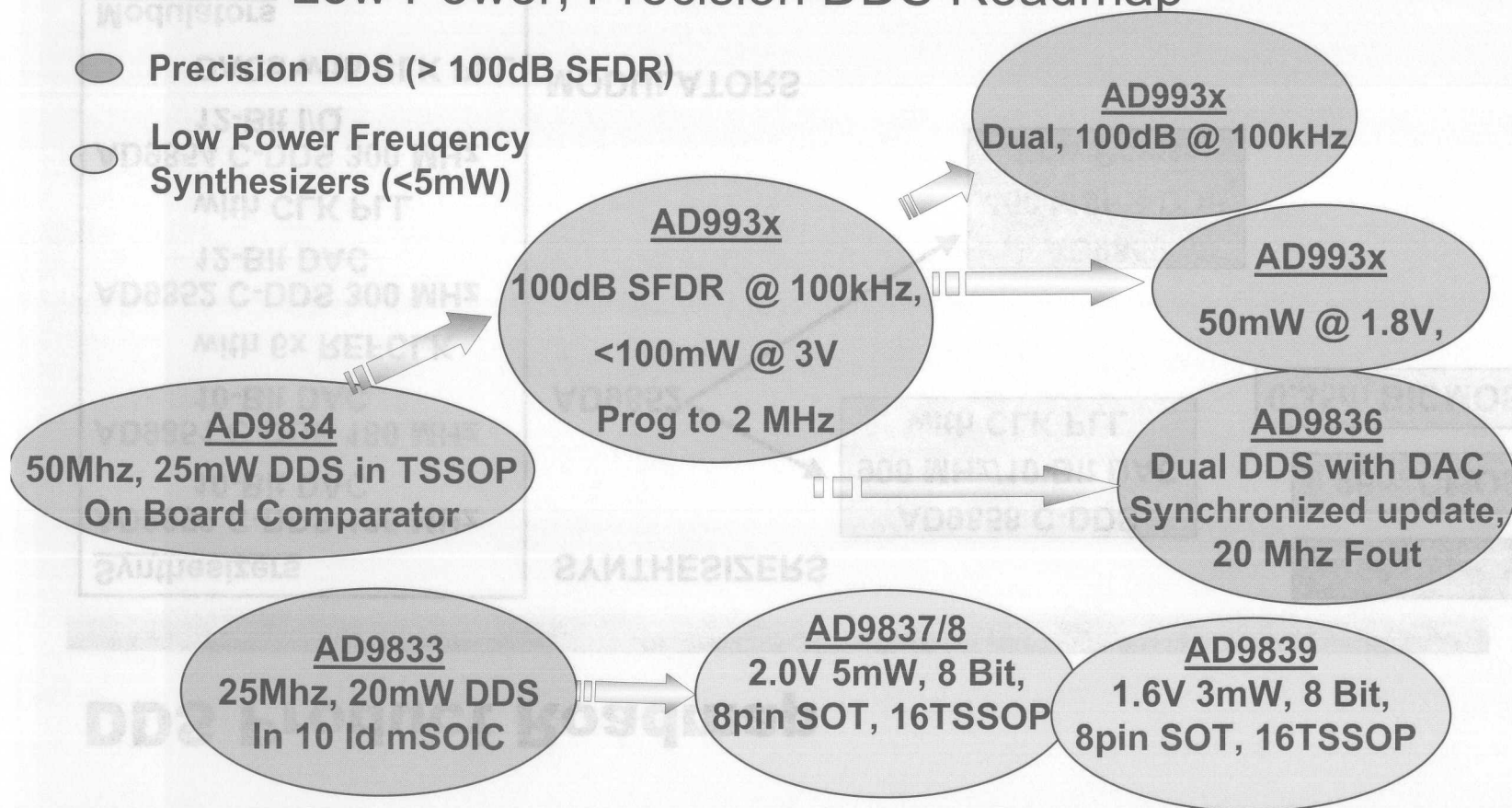
RELEASED

Low Power, Precision Frequency Synthesizer Roadmap

Low Power, Precision DDS Roadmap

● Precision DDS (> 100dB SFDR)

○ Low Power Frequency Synthesizers (<5mW)



- Instrumentation
- Wireless LAN Cards
- Wireless Base Stations
- Transmitters
- Receivers
- Wireless handsets
- Any Receiver/Transmitter System Using RF

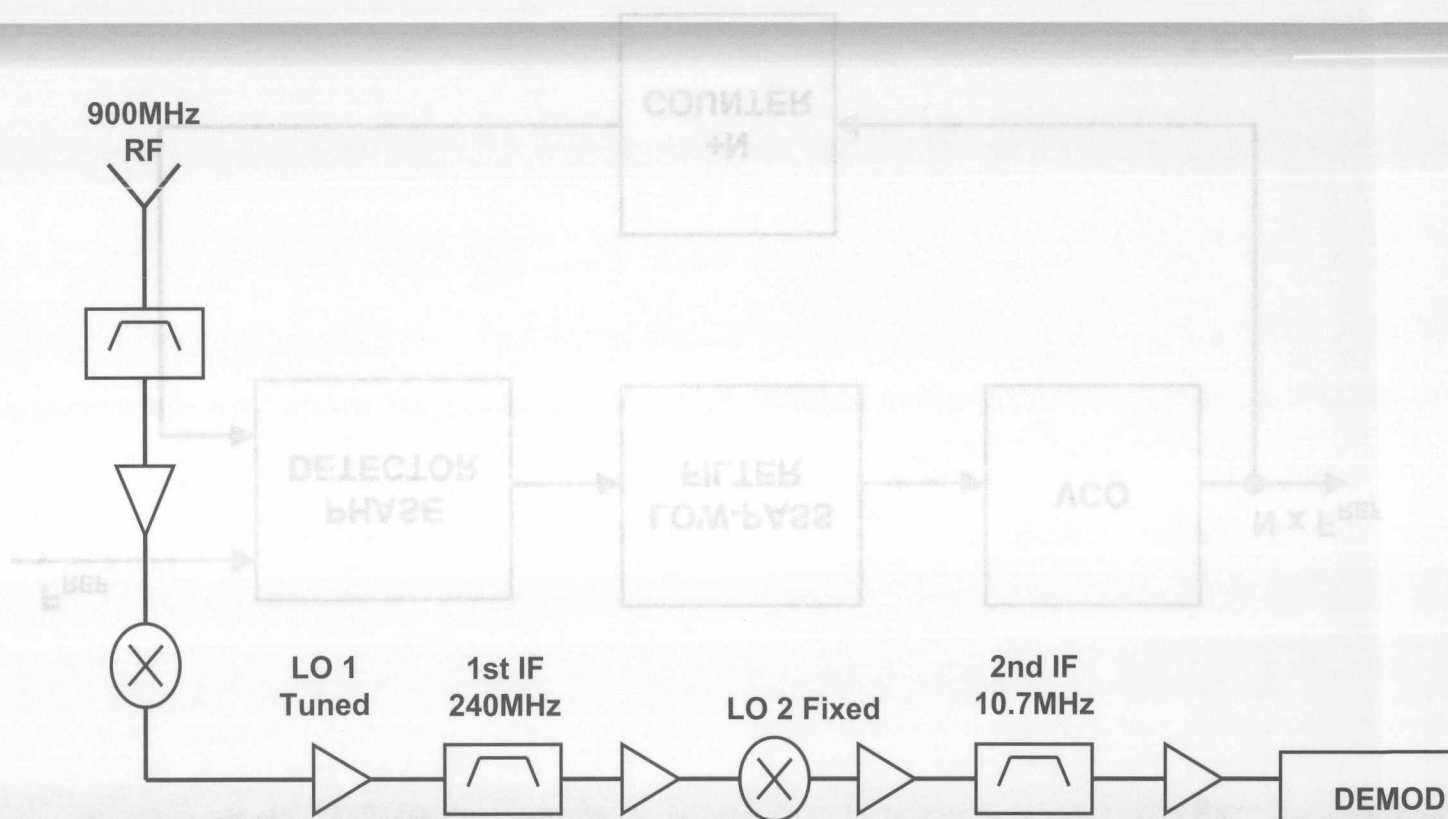
Phase Locked Loops

Where Are PLLs/VCOs Used?

Where Are PLLs/VCOs Used?

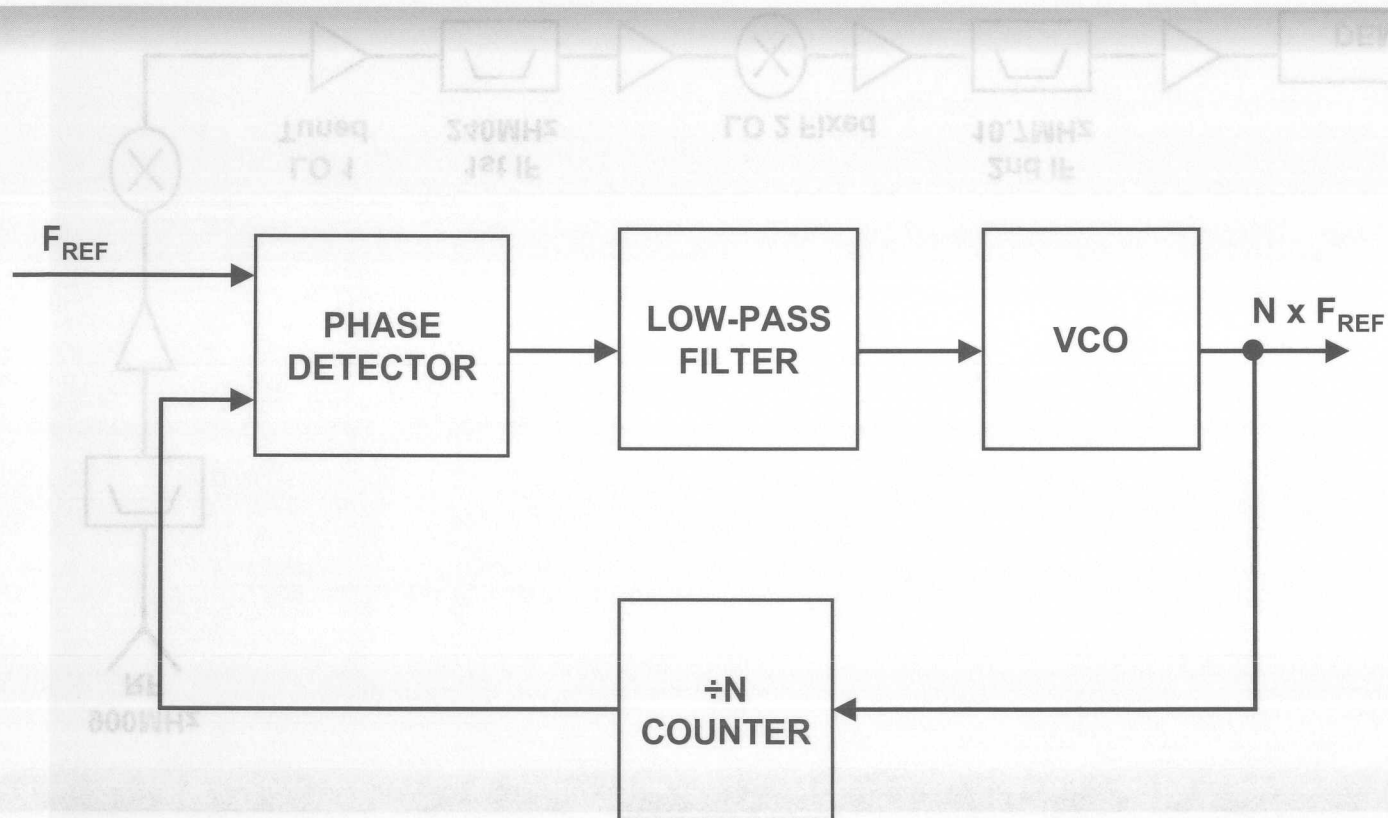
- Any Receiver/Transmitter System Using RF
 - Wireless handsets
 - Receivers
 - Transmitters
- Wireless Base Stations
- Wireless LAN Cards
- Instrumentation

Where Are PLLs/VCOs Used?

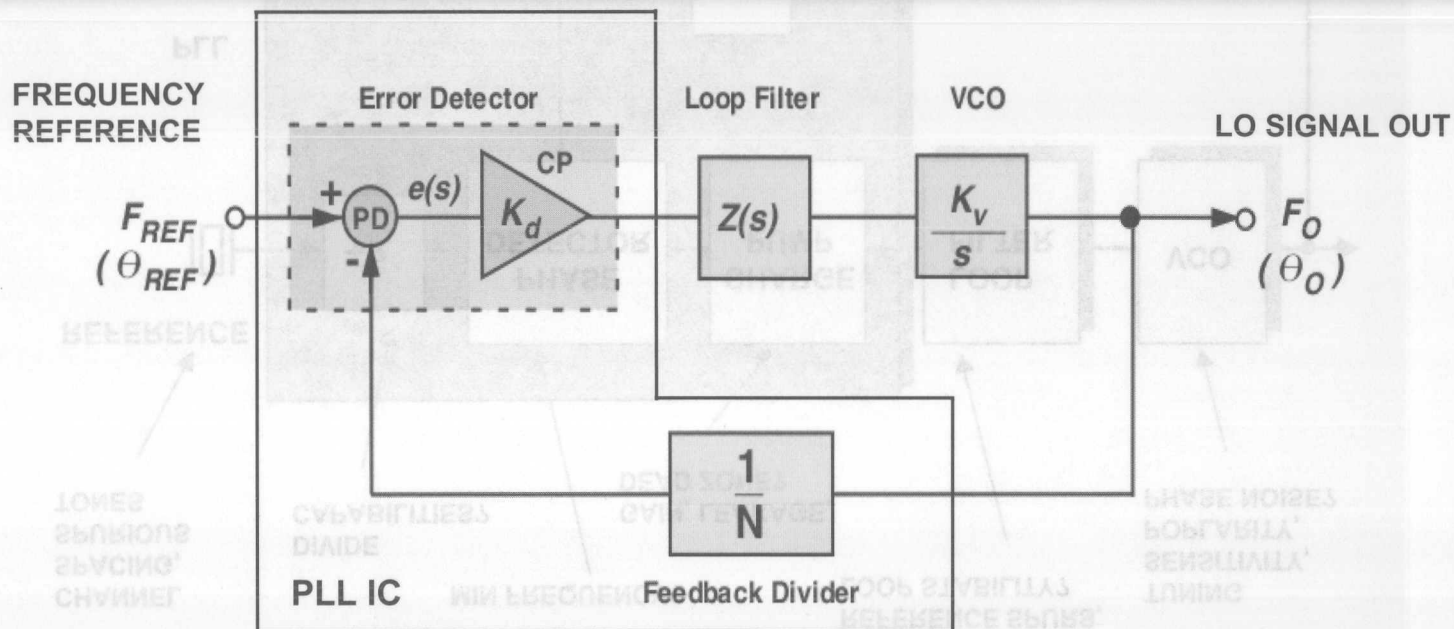


Dual Conversion Superheterodyne Receiver

Basic PLL System



Phase Locked Loop (PLL) Concept



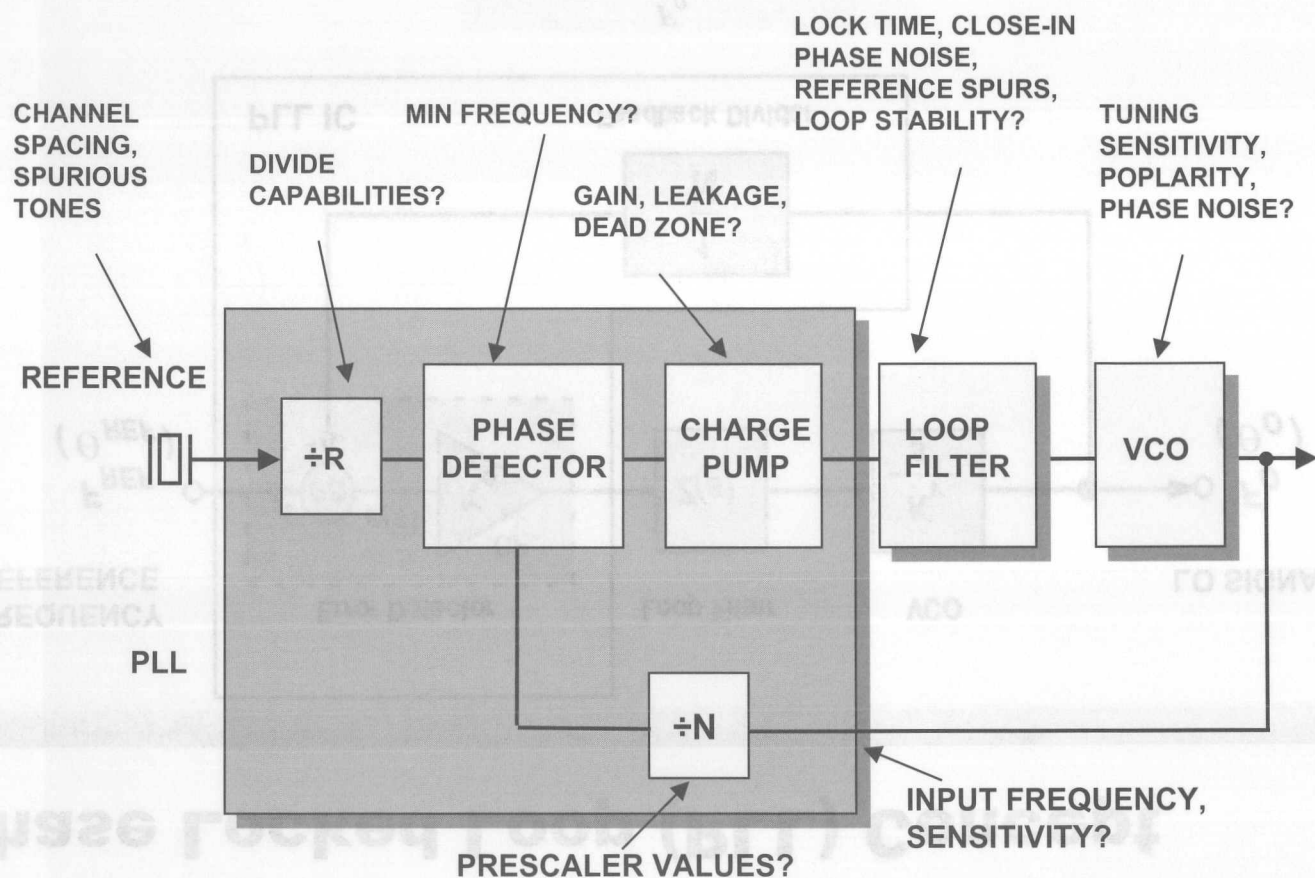
$$e(s) = F_{REF} - \frac{F_o}{N}$$

When $e(s) = 0$

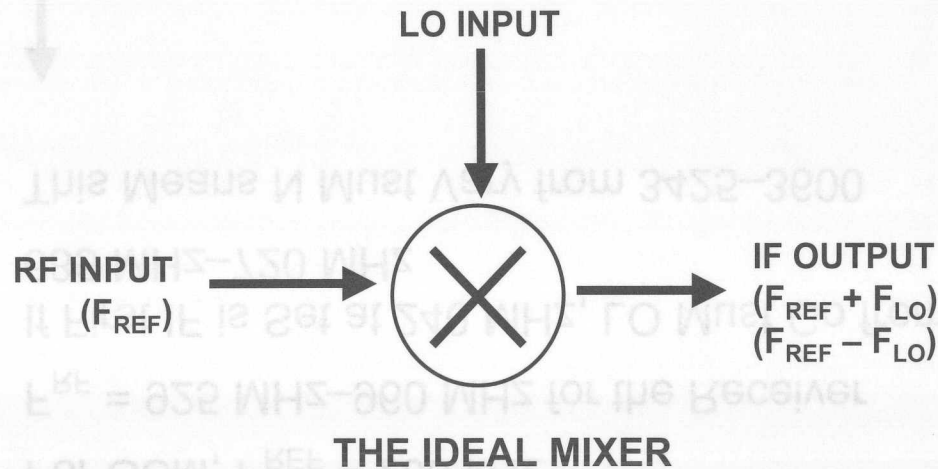
$$\frac{F_o}{N} = F_{REF}$$

$$F_o = N \cdot F_{REF}$$

PLL Performance Issues

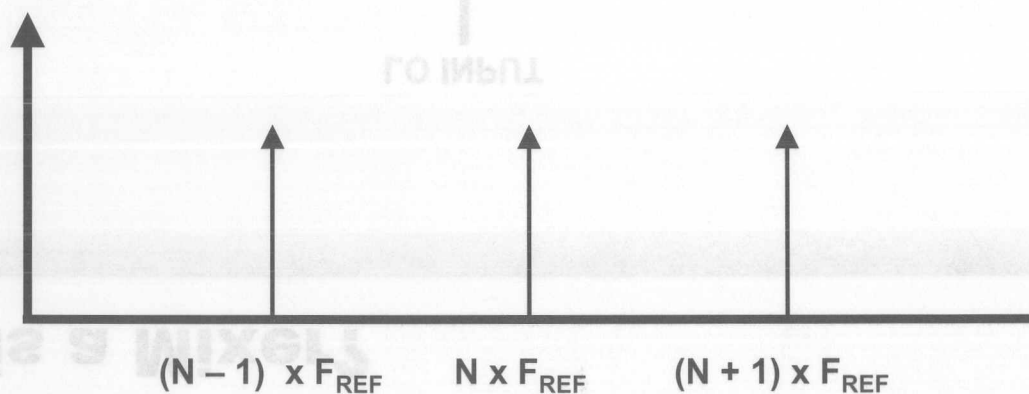


What is a Mixer?



Channel Spacing for Integer N PLL

- $DF = F_{REF}$
- For GSM, $F_{REF} = 200$ kHz
- $F_{RF} = 925$ MHz–960 MHz for the Receiver
- If First IF is Set at 240 MHz, LO Must Go from 685 MHz–720 MHz
- This Means N Must Vary from 3425–3600

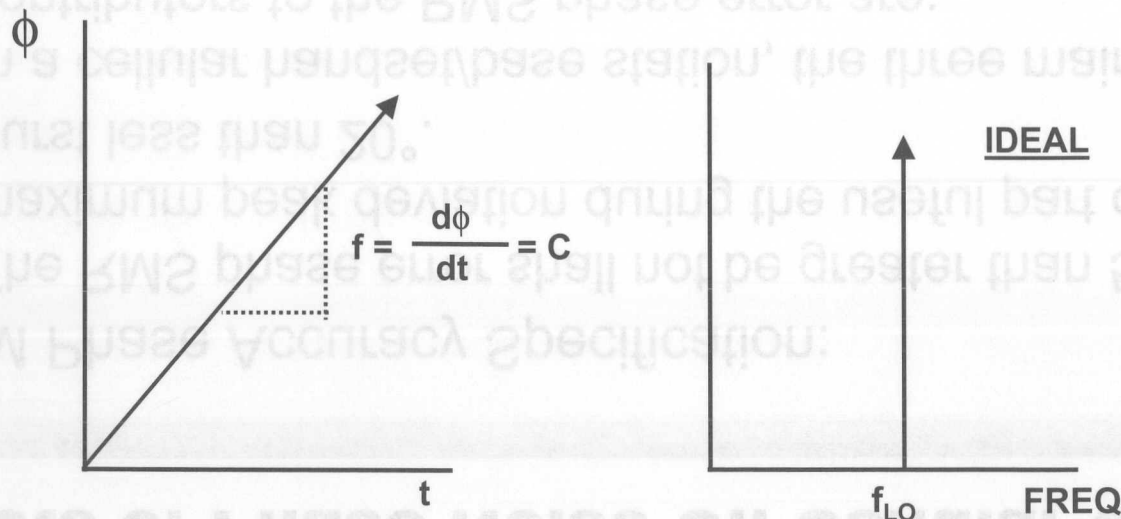


Effects of Phase Noise On Cellular Systems

- GSM Phase Accuracy Specification:
 - The RMS phase error shall not be greater than 5° with a maximum peak deviation during the useful part of the burst less than 20° .
 - In a cellular handset/base station, the three main contributors to the RMS phase error are:
 - Q Synt—the integrated phase error due to the LO PLL synthesizer
 - Q Baseband—the integrated phase error due to the baseband converter
 - Q (I and Q)—the integrated phase error due to the IQ modulator

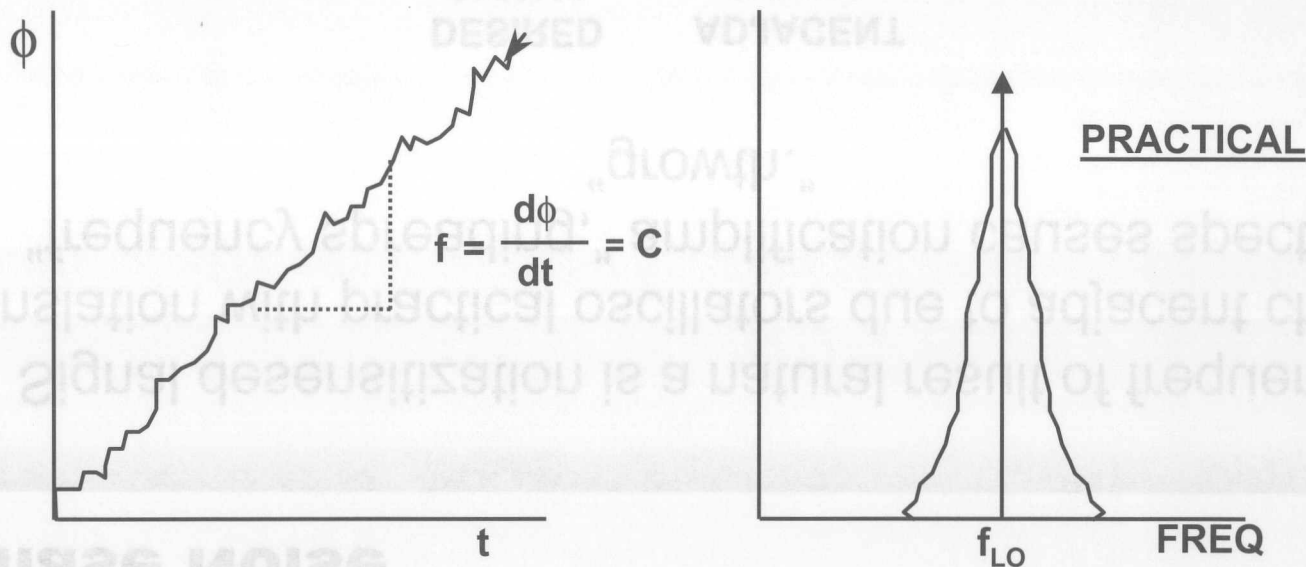
Phase Noise

An oscillator frequency is equal to the time derivative of phase. Constant oscillator phase slope equates to unique frequency in the frequency domain.



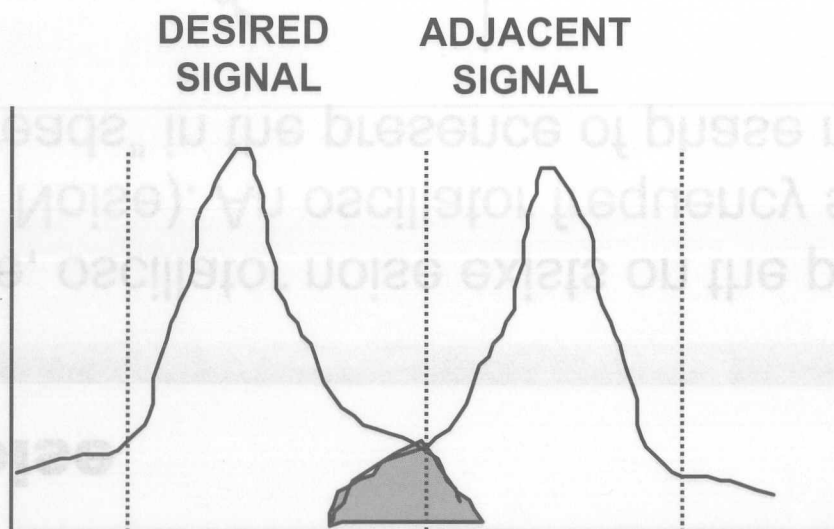
Phase Noise

In practice, oscillator noise exists on the phase slope (Phase Noise). An oscillator frequency spectrum “spreads” in the presence of phase noise.

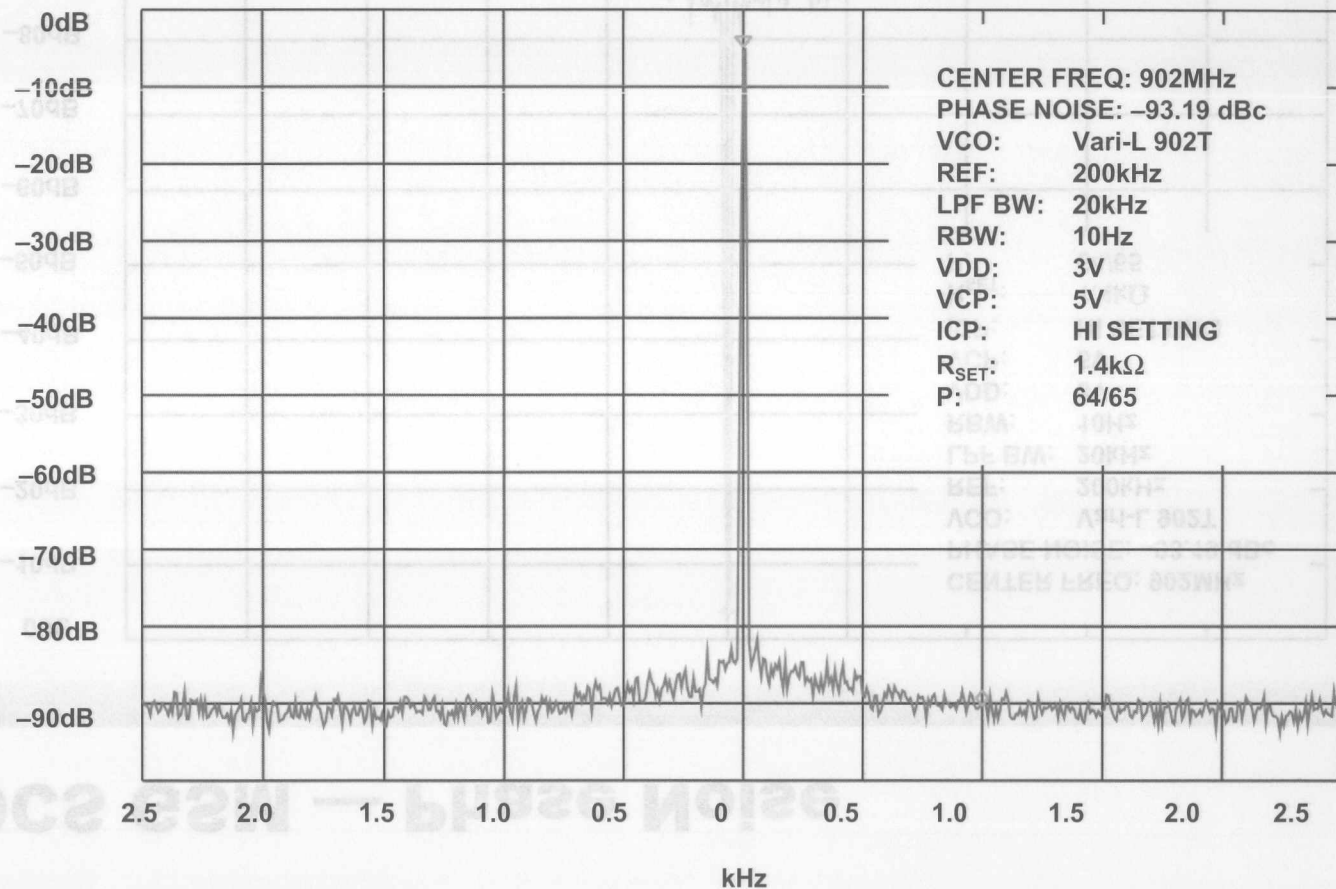


Phase Noise

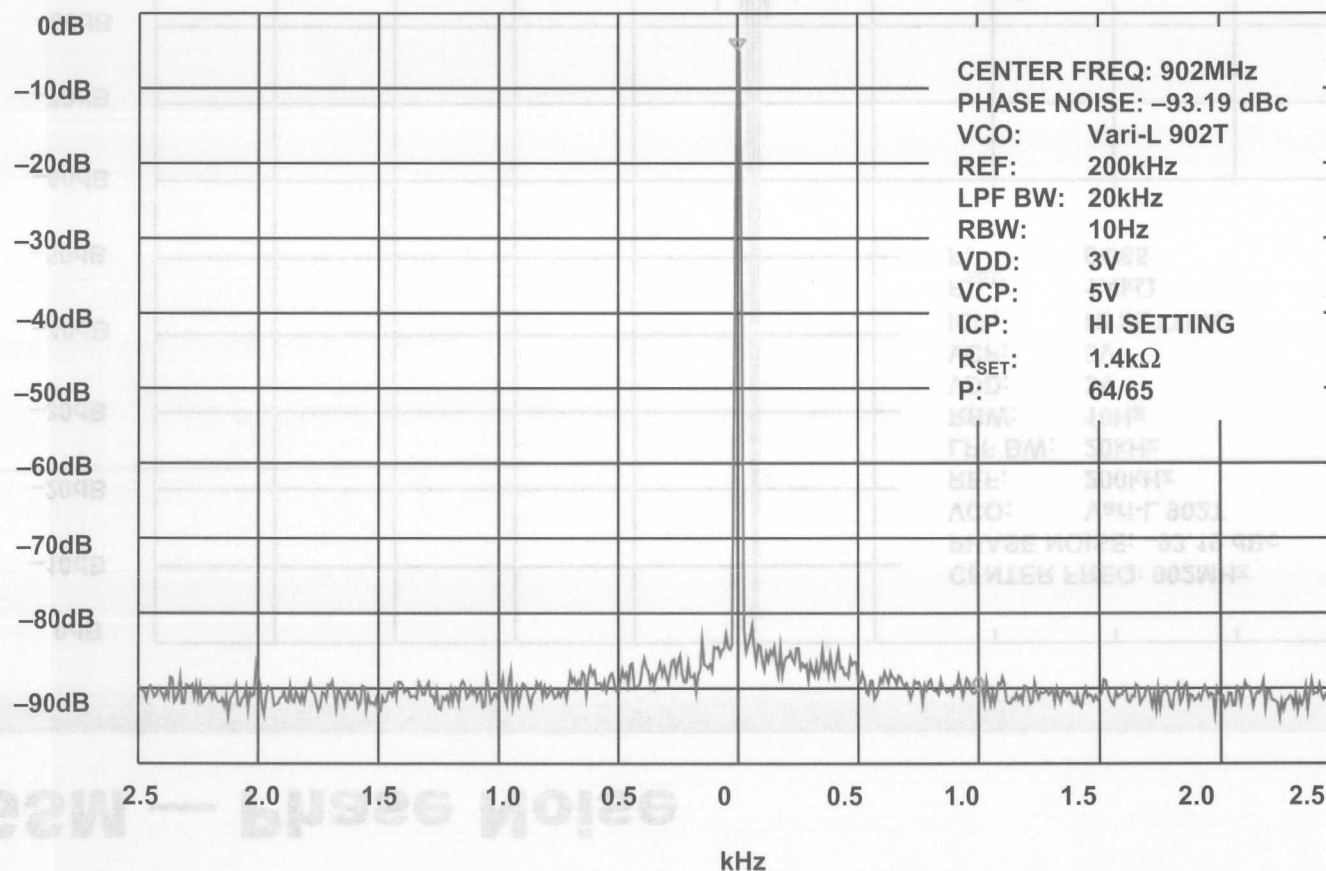
Signal desensitization is a natural result of frequency translation with practical oscillators due to adjacent channel “frequency spreading,” amplification causes spectral “growth.”



GSM — Phase Noise



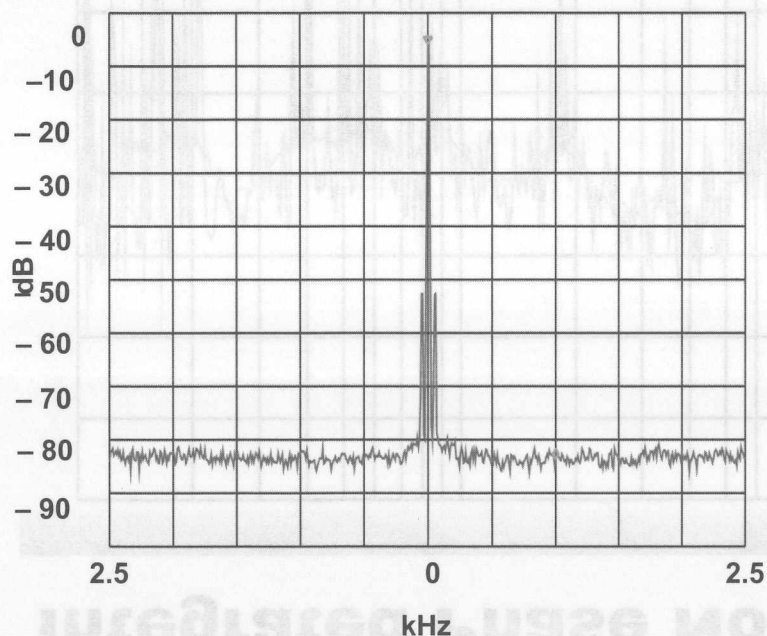
DCS GSM — Phase Noise



Measured ADI Phase Noise vs. Industry

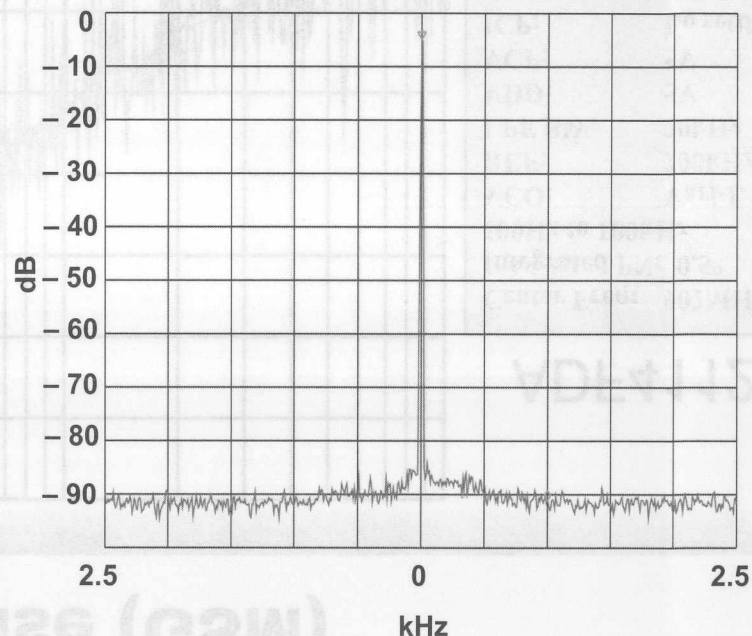
LMX2326 (900 MHz)

Phase Noise –85 dBc/Hz



ADF4112 (900 MHz)

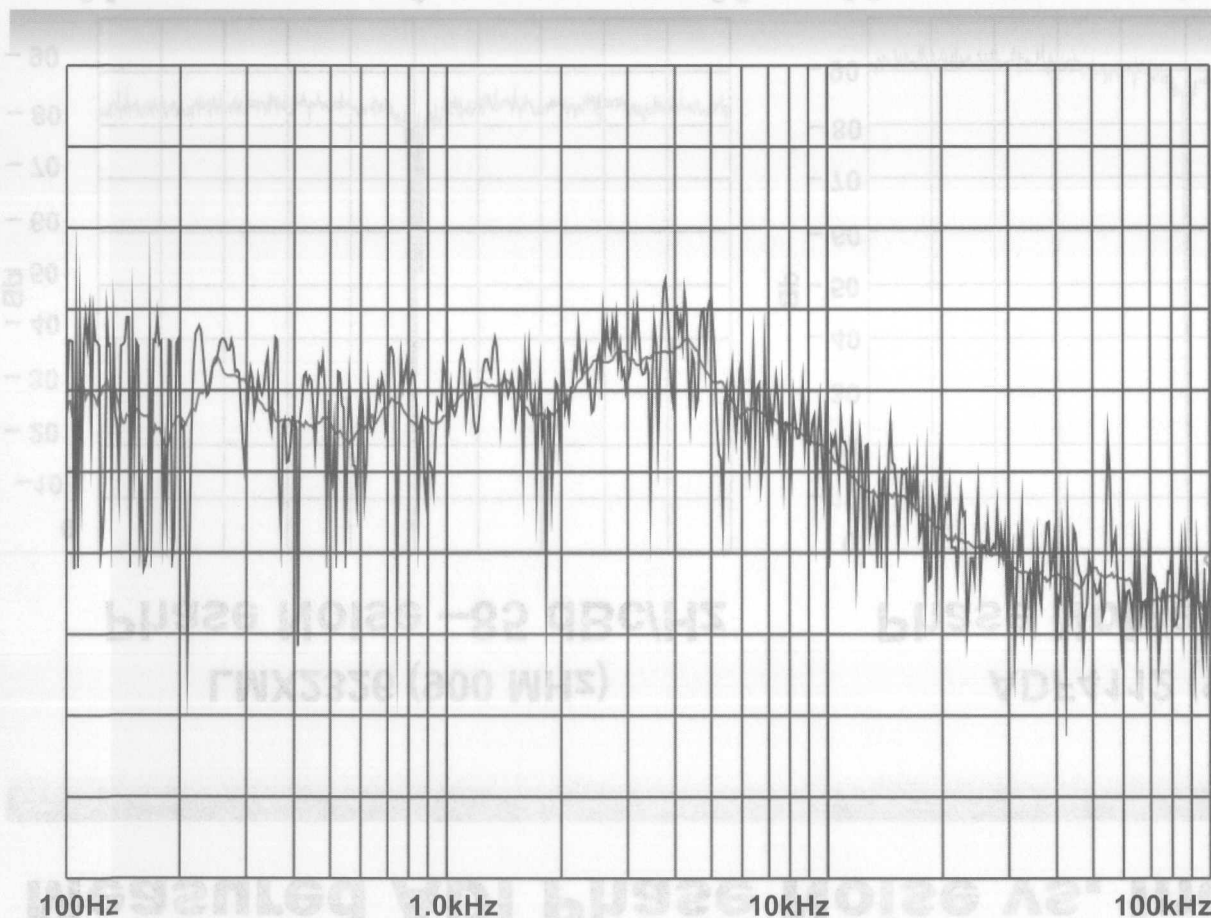
Phase Noise –92 dBc/Hz



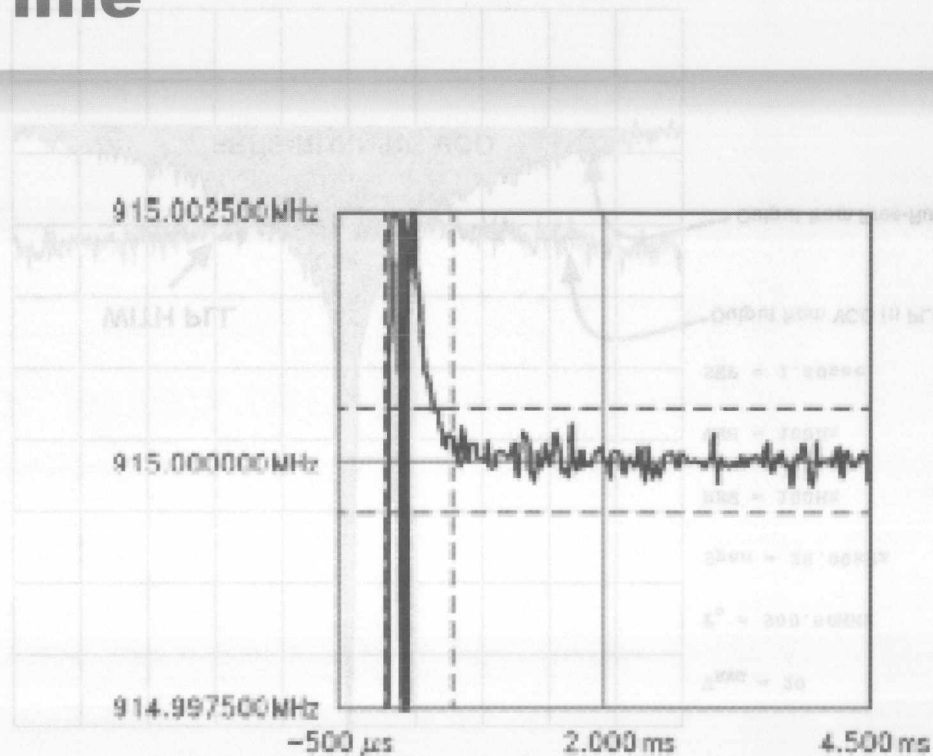
Integrated Phase Noise (GSM)

ADF4112

Center Freq: 902MHz
Integrated PN: 0.5°
100Hz to 100kHz
VCO: Vari-L 902T
REF: 200kHz
LPF BW: 20kHz
VDD: 5V
VCP: 5V
ICP: Lo setting
R_{SET}: 4.7kΩ
P: 32/33



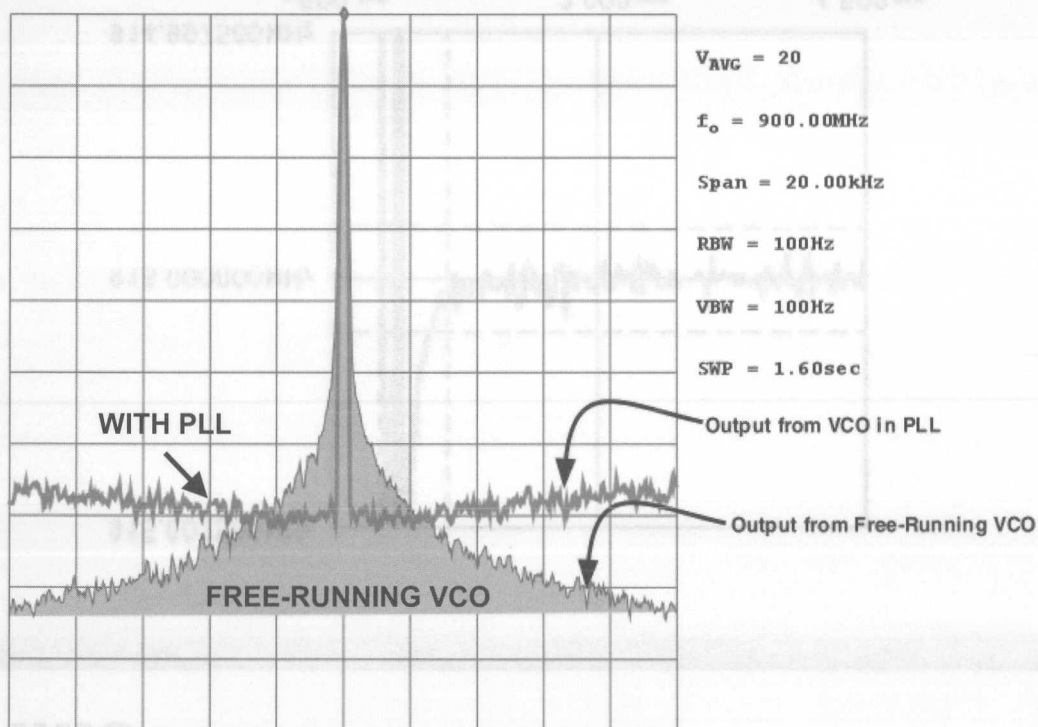
Lock Time



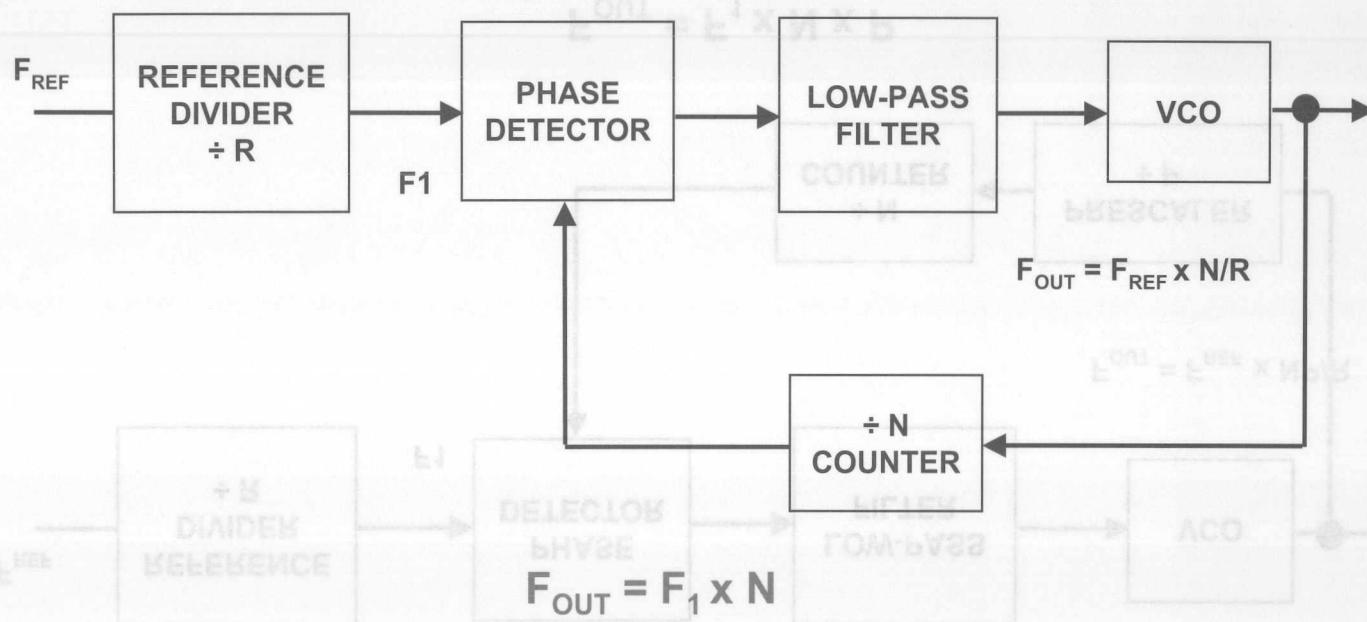
Settling Time Is Proportional to F_{REF} and the Loop Bandwidth

Comparing Locked and Open PLL LO Noise Performance

LO WITH ADF4xxx



Using a Reference Divider



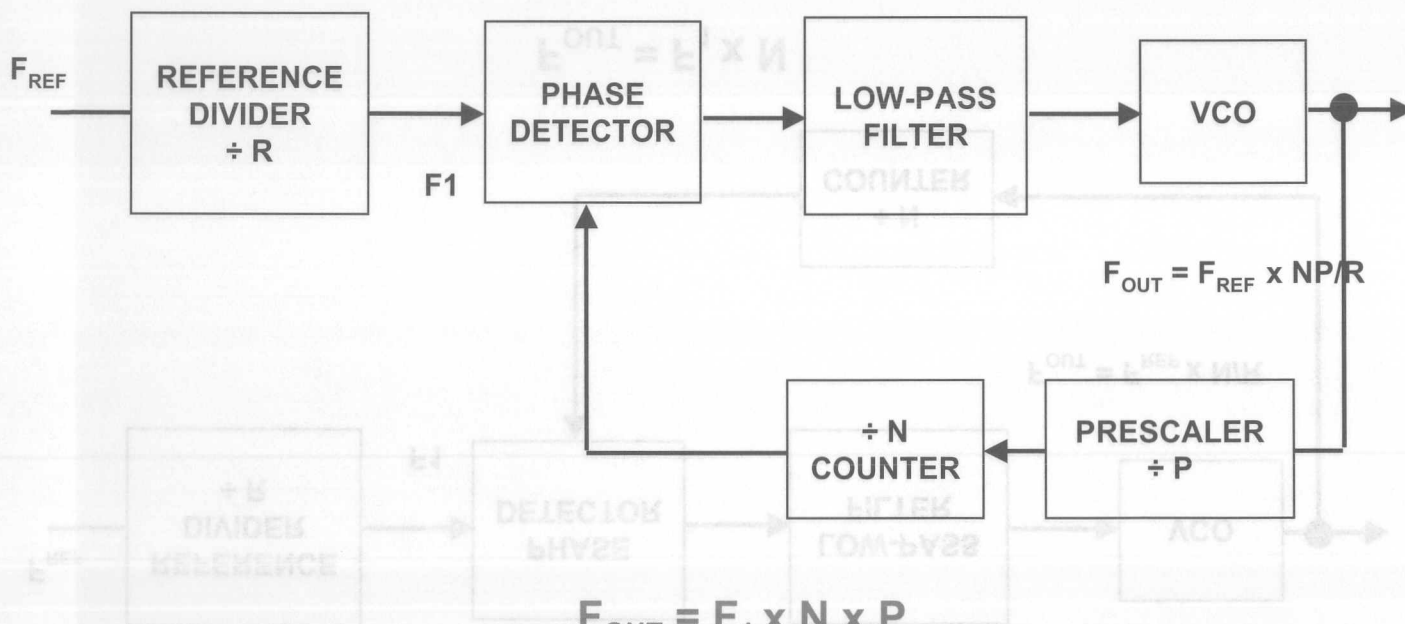
$$F_{OUT} = F_1 \times N$$

$$F_1 = F_{REF}/R$$

$$F_{OUT} = (F_{REF}/R) \times N$$

$$F_{OUT} = F_{REF} \times (N/R)$$

Prescaler

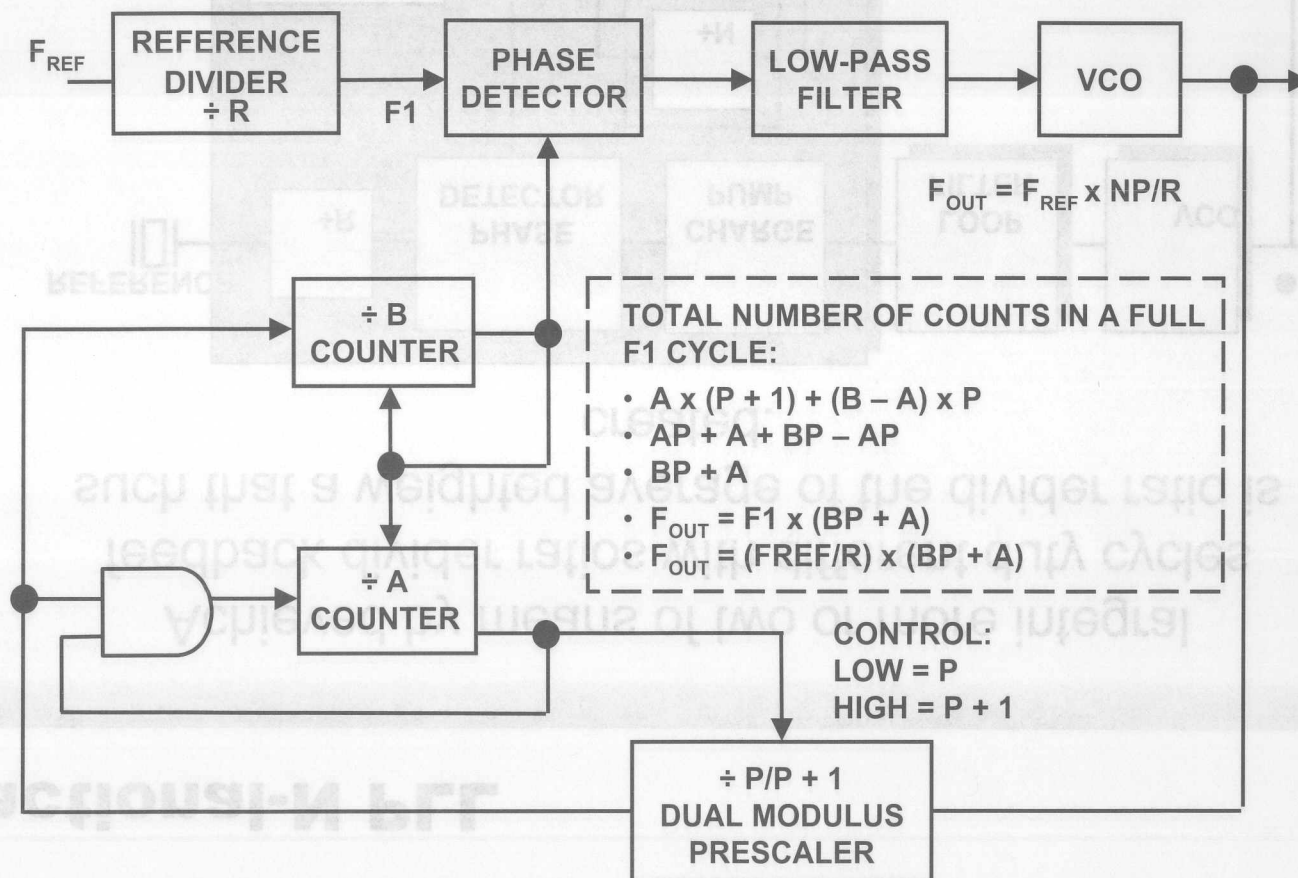


$$F_{OUT} = F_1 \times N \times P$$

$$F_{OUT} = (F_{REF}/R) \times N \times P$$

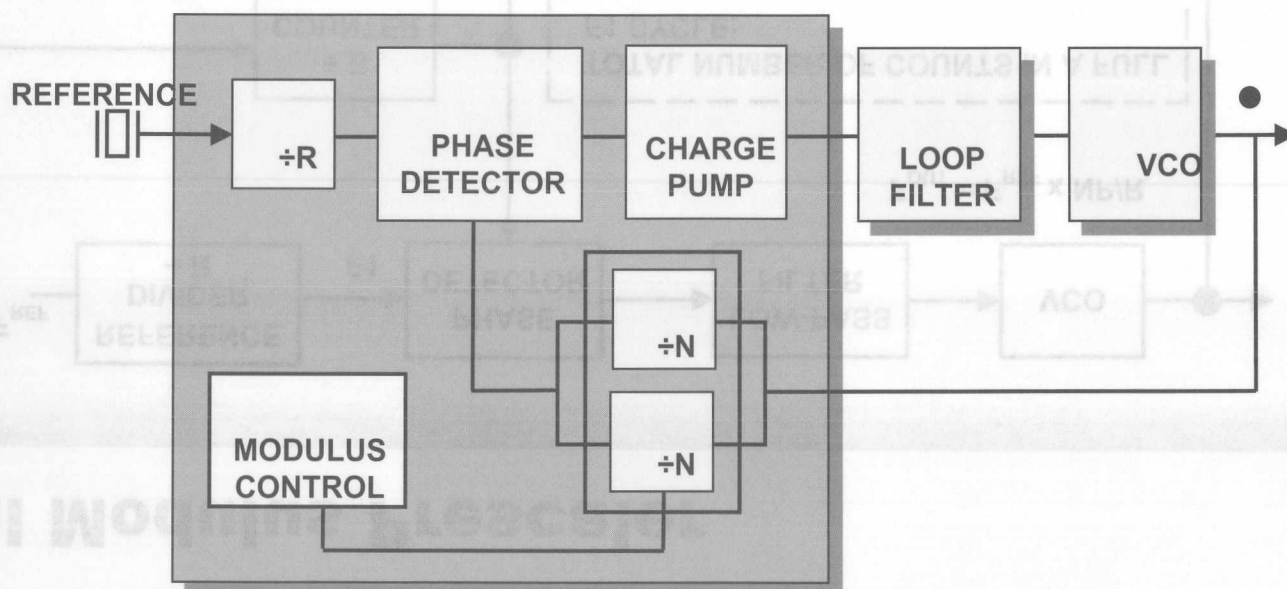
$$F_{OUT} = F_{REF} \times (NP/R)$$

Dual Modulus Prescaler

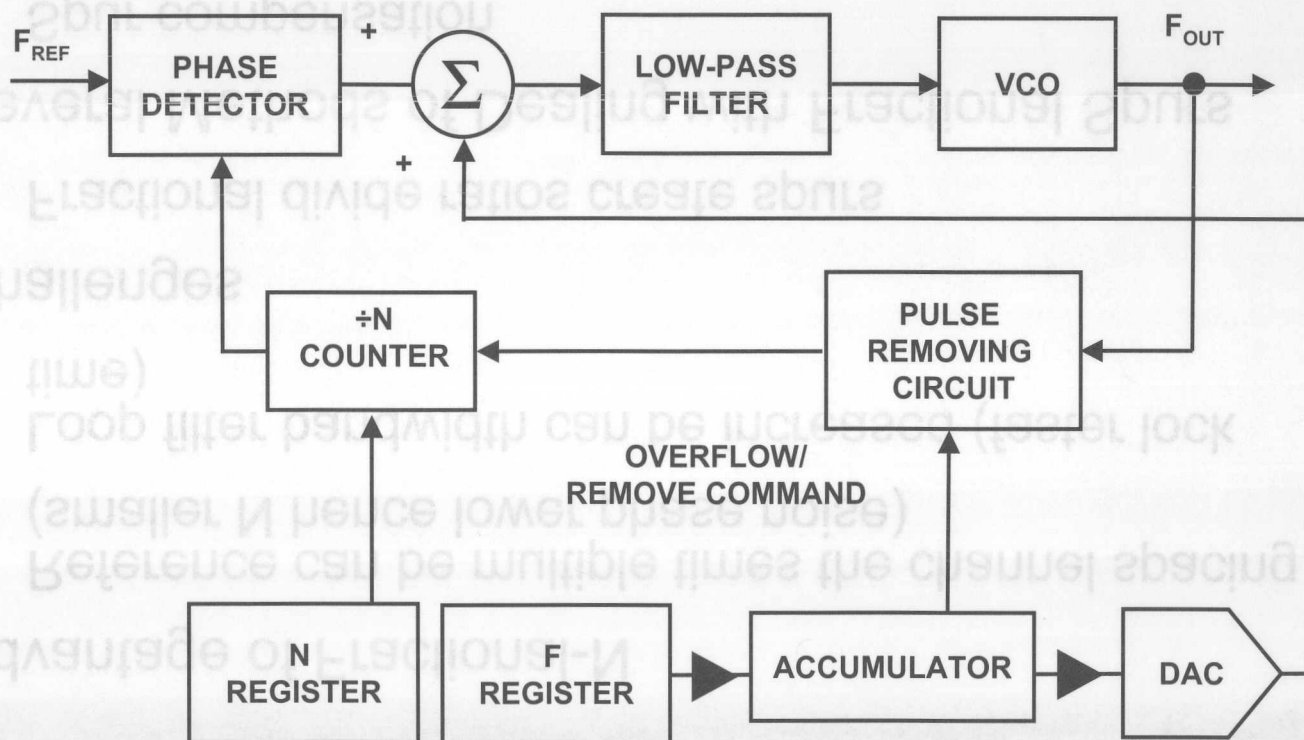


Fractional-N PLL

Achieved by means of two or more integral feedback divider ratios with different duty cycles such that a weighted average of the divider ratio is created.



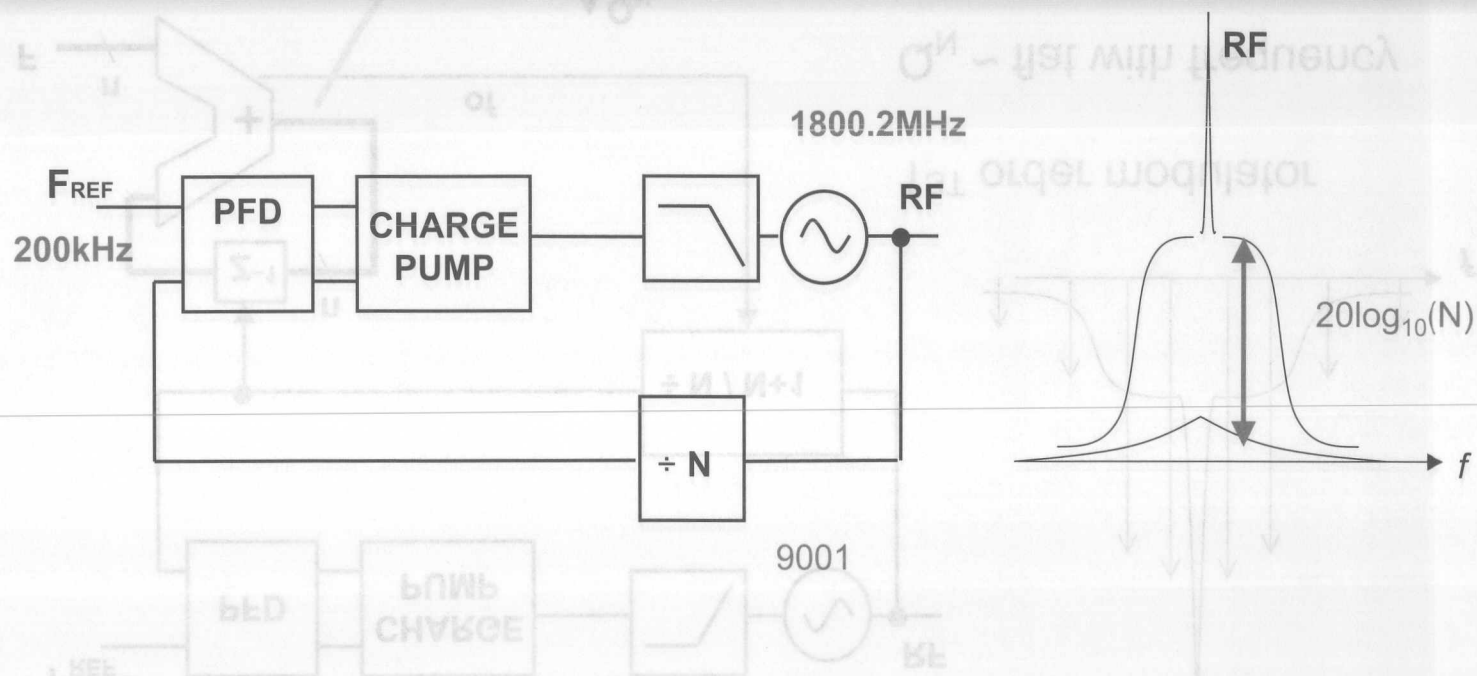
Fractional-N PLL



Fractional-N PLL

- Advantage of Fractional-N
 - Reference can be multiple times the channel spacing (smaller N hence lower phase noise)
 - Loop filter bandwidth can be increased (faster lock time)
- Challenges
 - Fractional divide ratios create spurs
- Several Methods of Dealing with Fractional Spurs
 - Spur compensation
 - Noise shaping
 - Combination of both

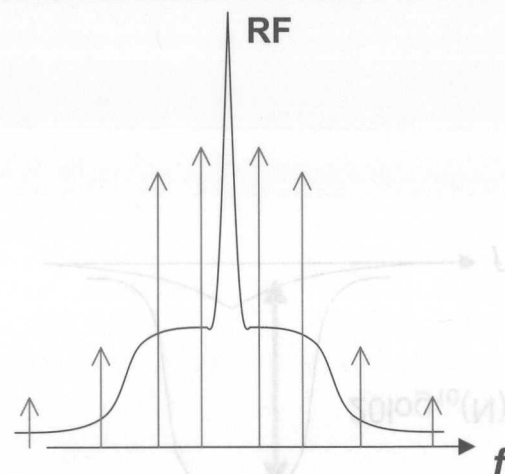
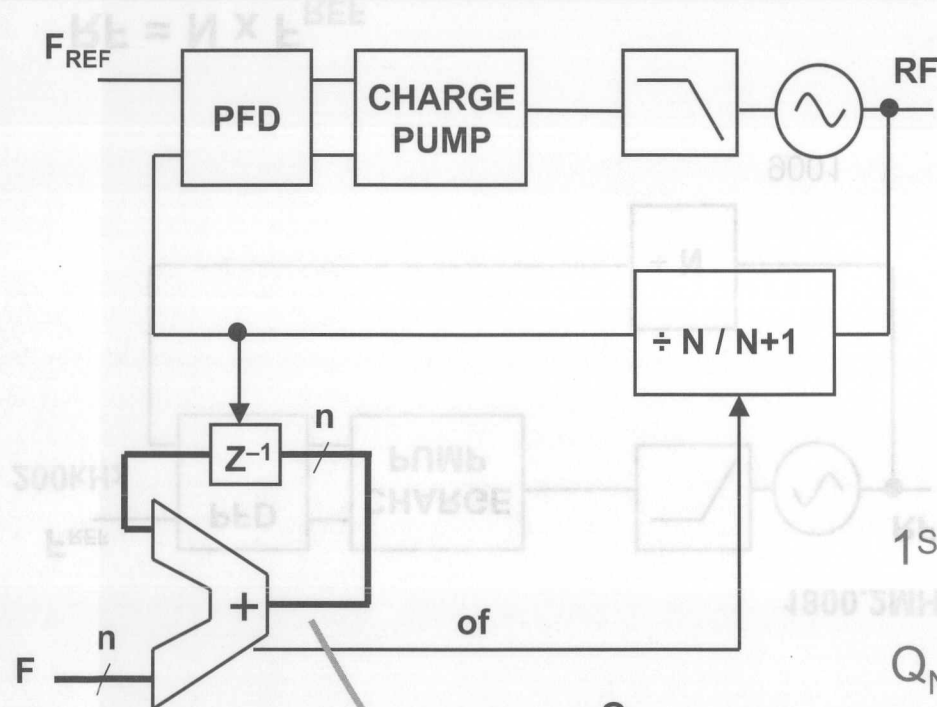
Integer-N PLL Synthesizer: Limitations



$$RF = N \times F_{REF}$$

Large $N \Rightarrow$ Large phase noise gain inside loop bandwidth

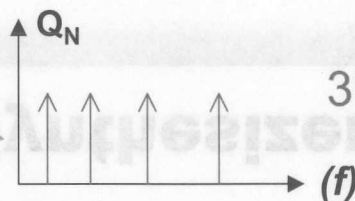
Quantization Noise Spurs



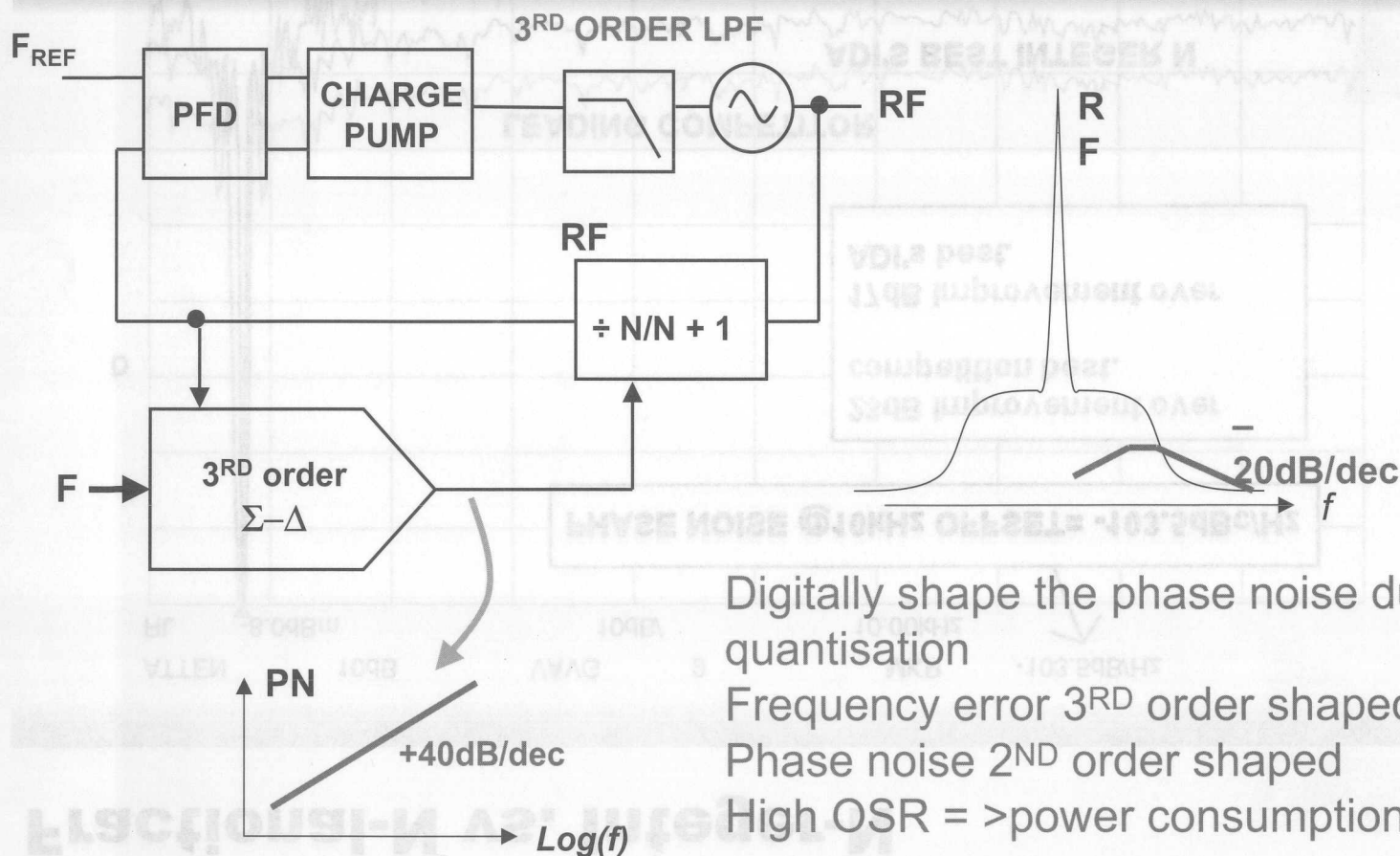
1ST order modulator

$Q_N \sim \text{flat with frequency}$

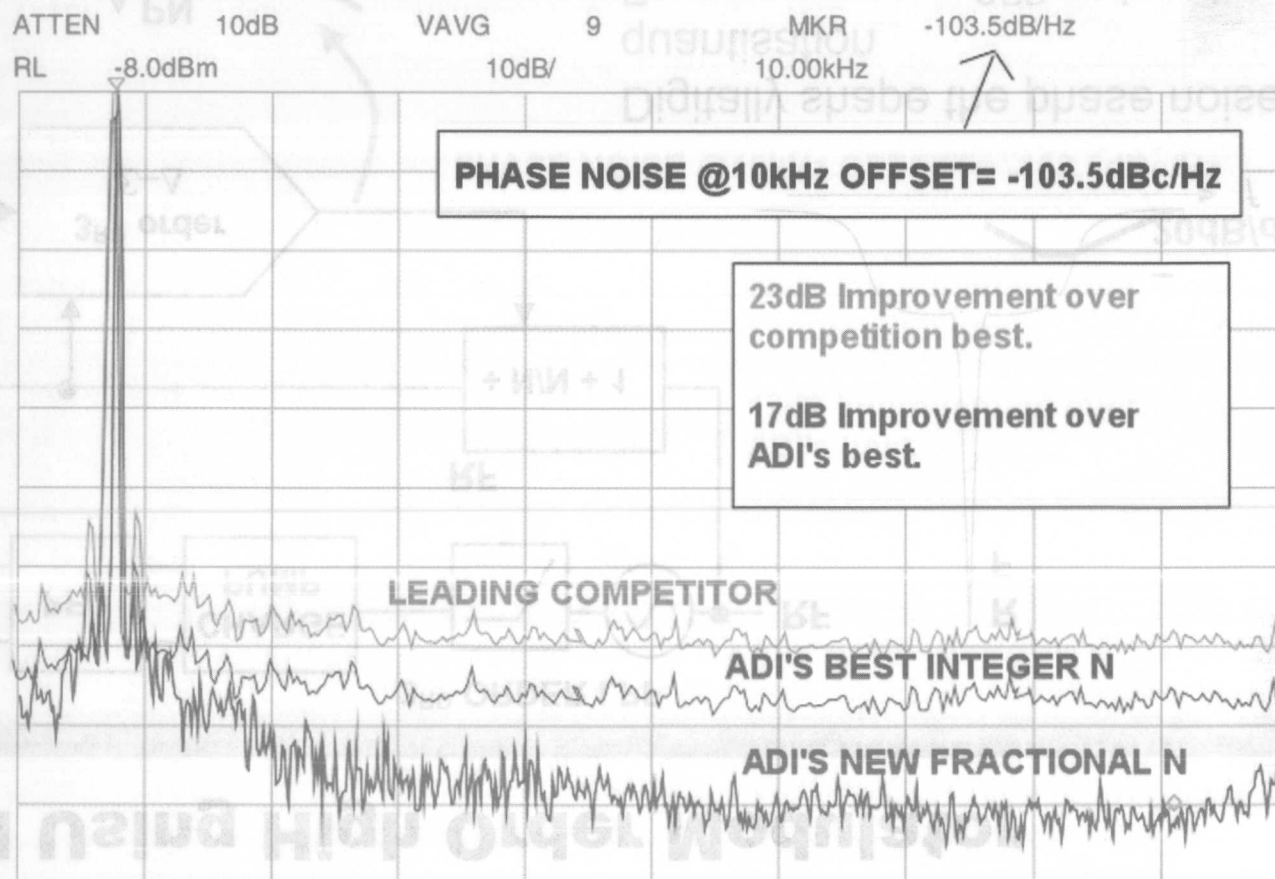
3RD order roll-off from loop filter



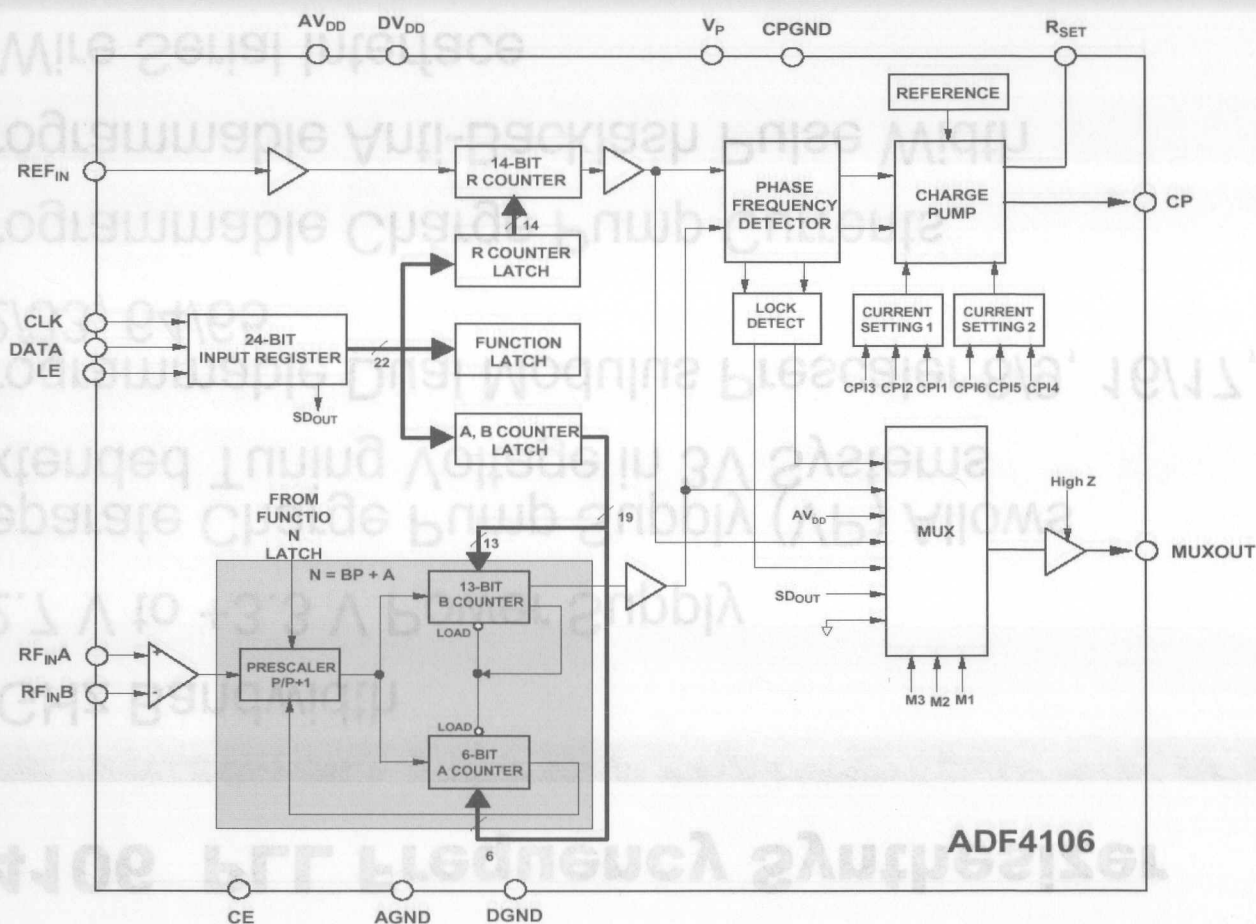
F-N Using High Order Modulator



Fractional-N vs. Integer-N



ADF4106 PLL Frequency Synthesizer

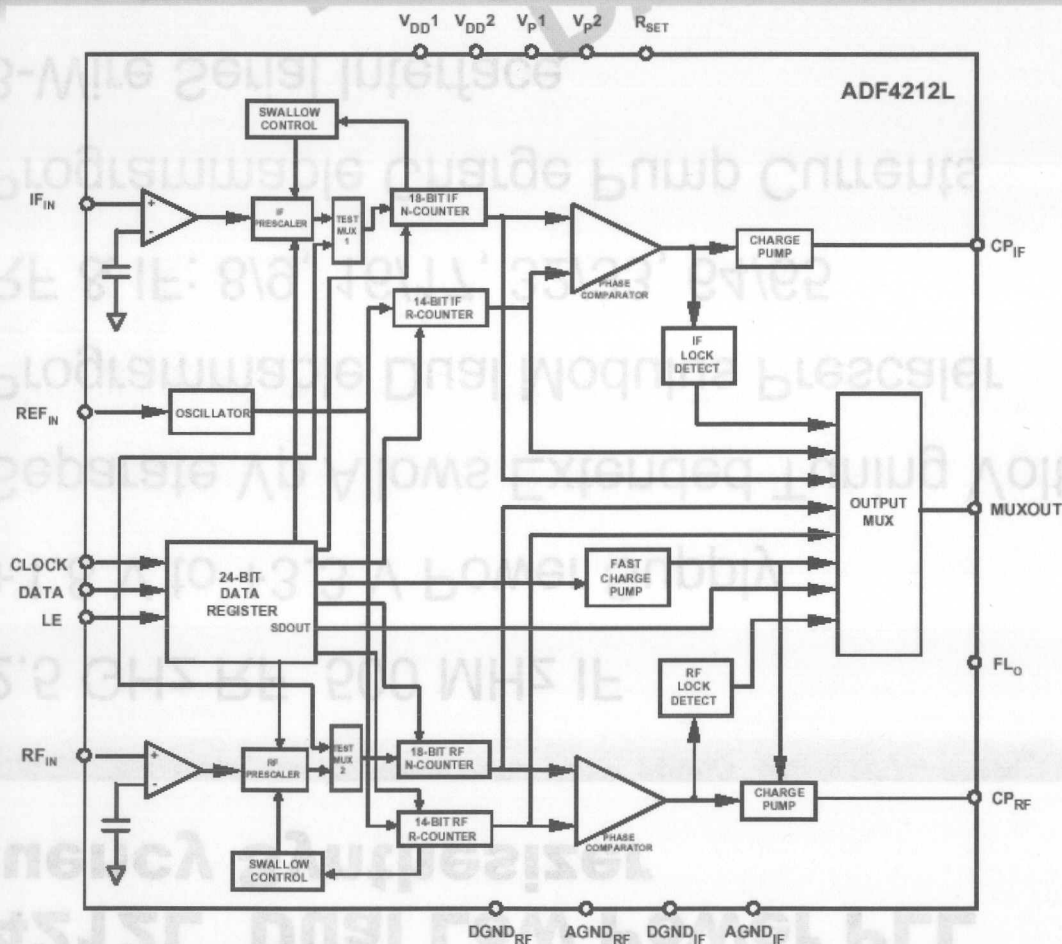


ADF4106

ADF4106 PLL Frequency Synthesizer

- 6 GHz Bandwidth
- +2.7 V to +3.3 V Power Supply
- Separate Charge Pump Supply (VP) Allows Extended Tuning Voltage in 3V Systems
- Programmable Dual Modulus Prescaler 8/9, 16/17, 32/33, 64/65
- Programmable Charge Pump Currents
- Programmable Anti-Backlash Pulse Width
- 3-Wire Serial Interface
- Analog and Digital Lock Detect
- Hardware and Software Power Down Mode

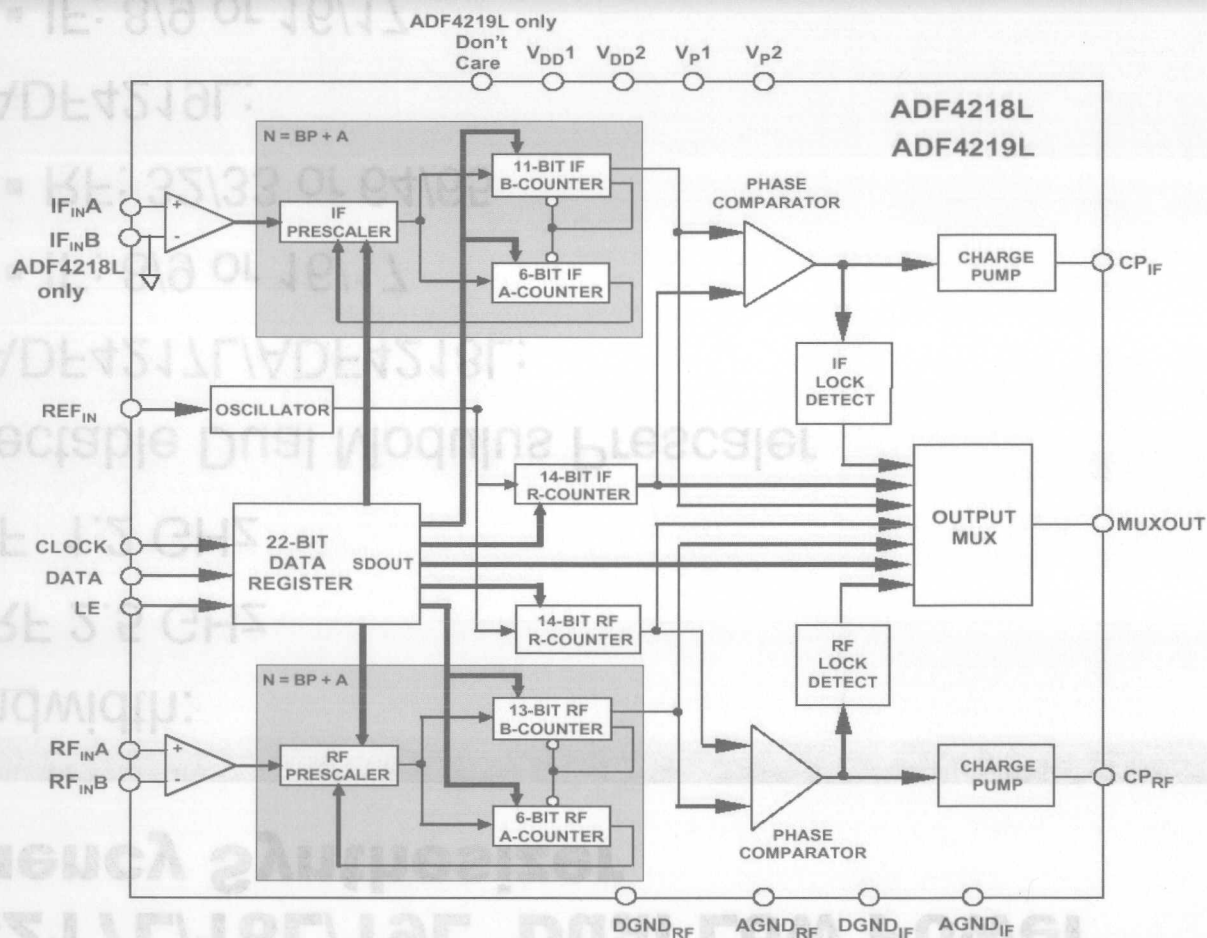
ADF4212L Dual Low Power PLL Frequency Synthesizer



ADF4212L Dual Low Power PLL Frequency Synthesizer

- 2.5 GHz RF 500 MHz IF
- +1.8 V to +3.3 V Power Supply
- Separate V_p Allows Extended Tuning Voltage
- Programmable Dual Modulus Prescaler
- RF & IF: 8/9, 16/17, 32/33, 64/65
- Programmable Charge Pump Currents
- 3-Wire Serial Interface
- 5 mA Total Supply Current
- Power Down Mode

ADF4217L/18L/19L Dual Low Power Frequency Synthesizer



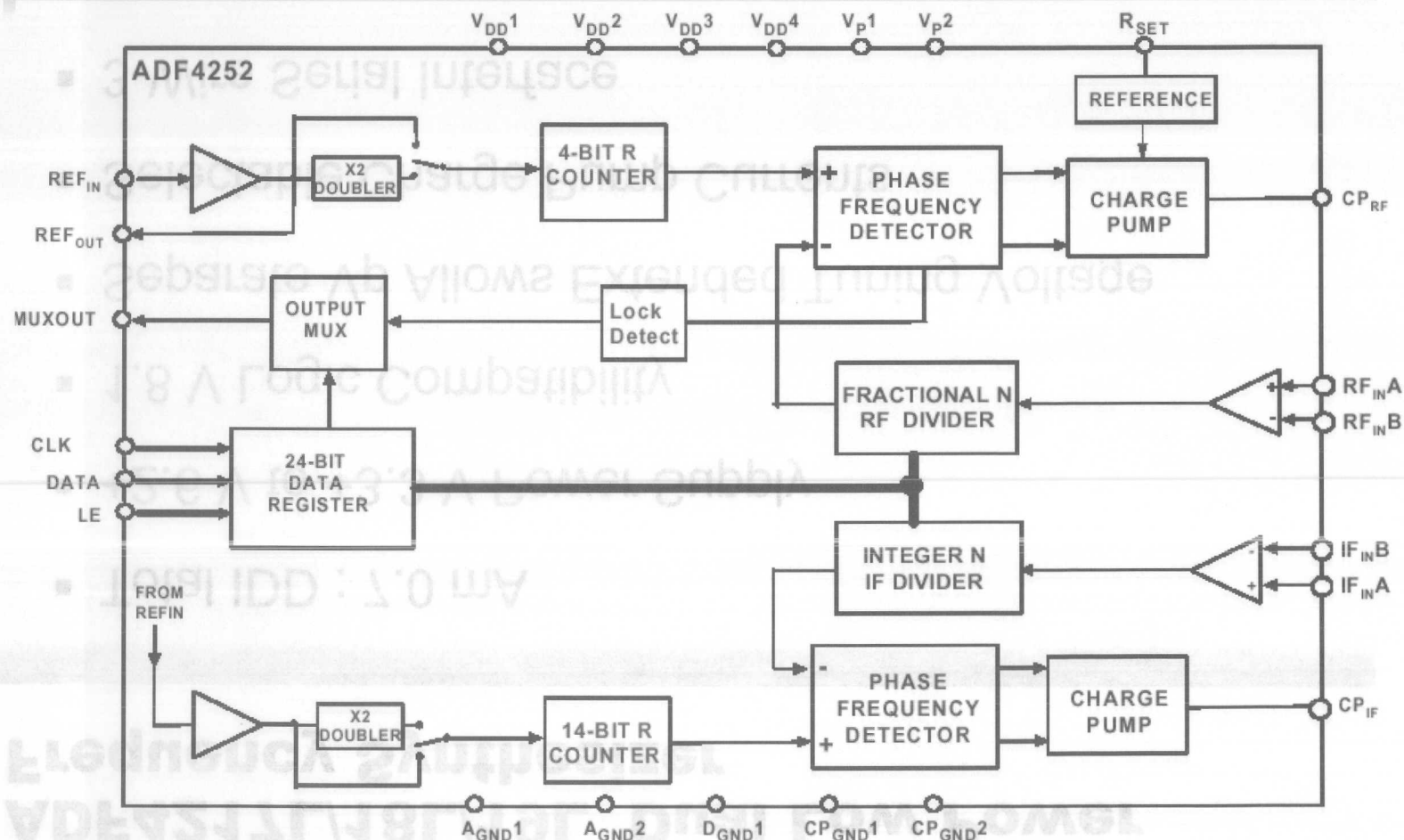
ADF4217L/18L/19L Dual Low Power Frequency Synthesizer

- Bandwidth:
 - RF 2.5 GHz
 - IF 1.2 GHz
- Selectable Dual Modulus Prescaler
 - ADF4217L/ADF4218L:
 - IF: 8/9 or 16/17
 - RF: 32/33 or 64/65
 - ADF4219L:
 - IF: 8/9 or 16/17
 - RF: 16/17 or 32/33

ADF4217L/18L/19L Dual Low Power Frequency Synthesizer

- Total I_{DD} : 7.0 mA
- +2.6 V to +3.3 V Power Supply
- 1.8 V Logic Compatibility
- Separate V_p Allows Extended Tuning Voltage
- Selectable Charge Pump Currents
- 3-Wire Serial Interface
- Power Down Mode

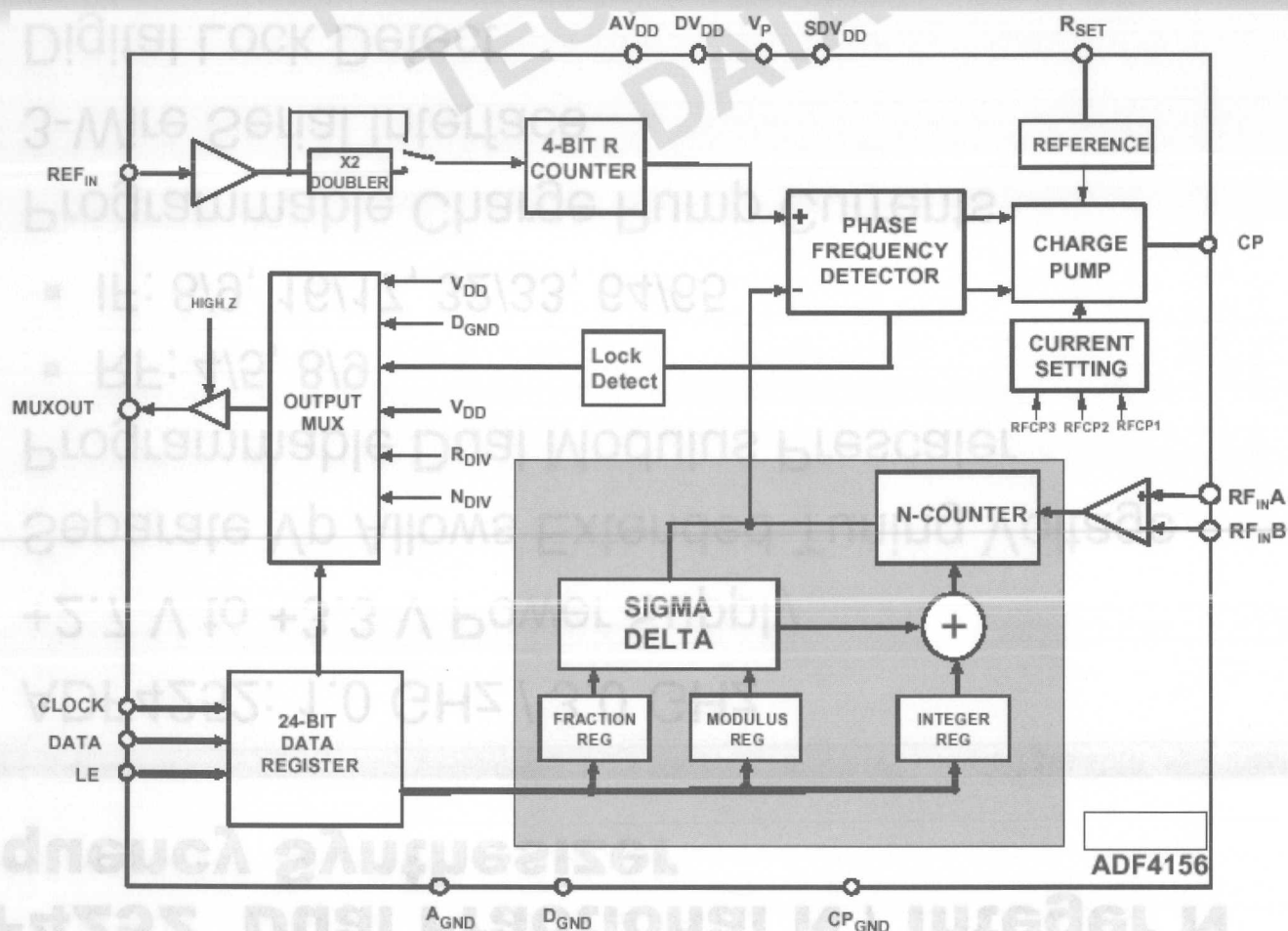
ADF4252 Dual Fractional N / Integer N Frequency Synthesizer



ADF4252 Dual Fractional N / Integer N Frequency Synthesizer

- ADF4252: 1.0 GHz / 3.0 GHz
- +2.7 V to +3.3 V Power Supply
- Separate V_p Allows Extended Tuning Voltage
- Programmable Dual Modulus Prescaler
 - RF: 4/5, 8/9
 - IF: 8/9, 16/17, 32/33, 64/65
- Programmable Charge Pump Currents
- 3-Wire Serial Interface
- Digital Lock Detect
- Power Down Mode
- Programmable Modulus Interpolator

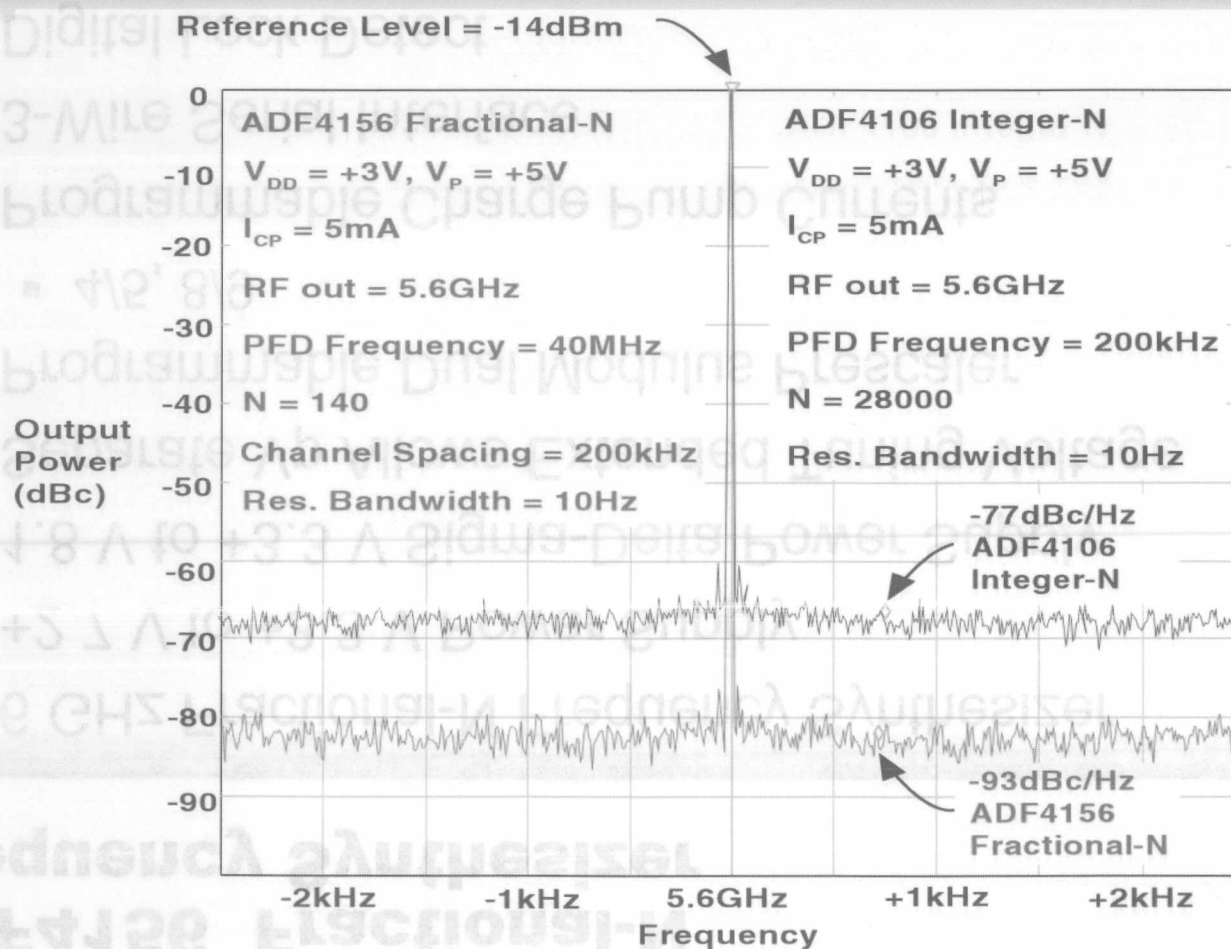
ADF4156 Fractional-N Frequency Synthesizer



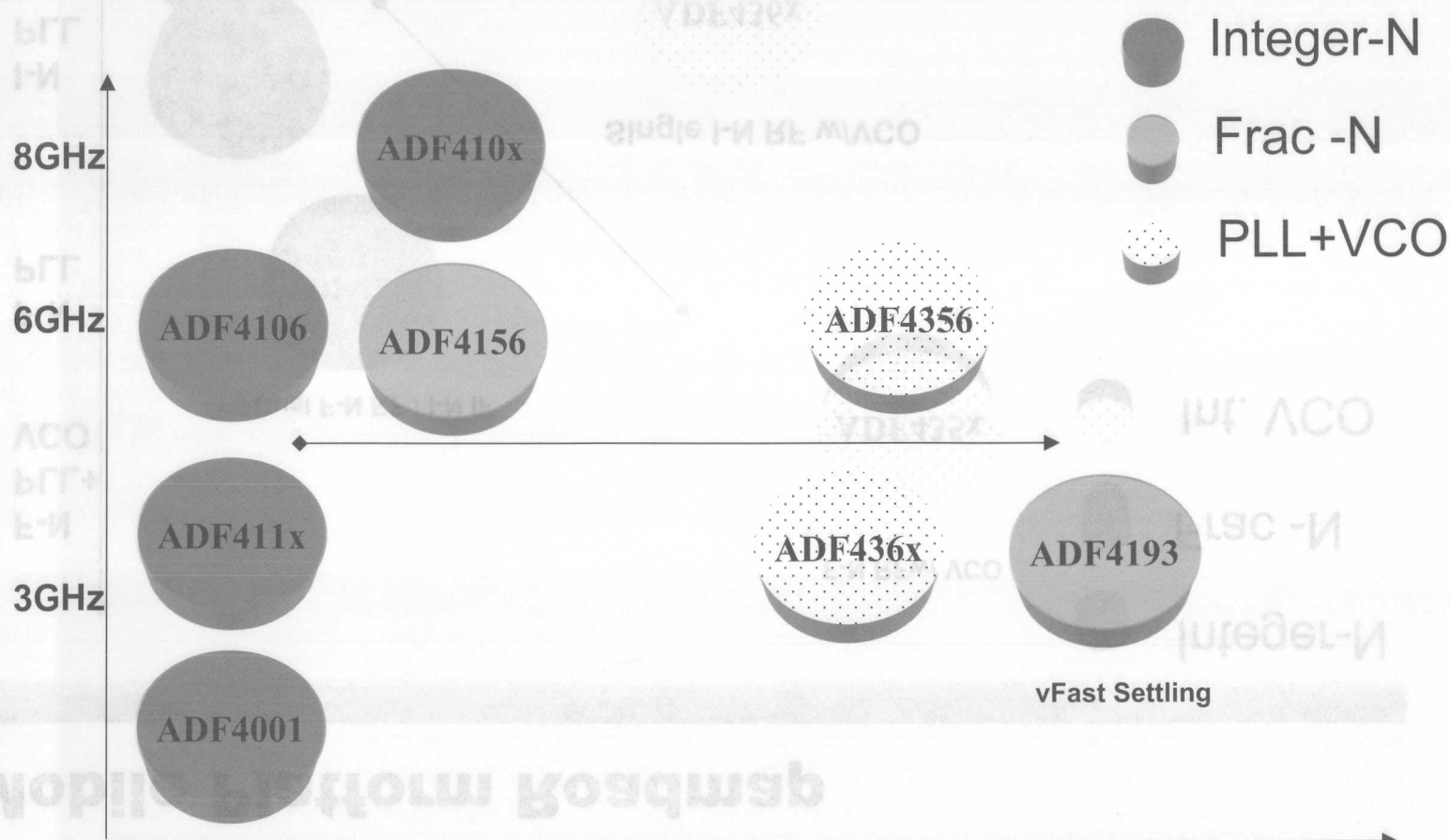
ADF4156 Fractional-N Frequency Synthesizer

- 6 GHz Fractional-N Frequency Synthesizer
- +2.7 V to +3.3 V Power Supply
- 1.8 V to +3.3 V Sigma-Delta Power Supply
- Separate Vp Allows Extended Tuning Voltage
- Programmable Dual Modulus Prescaler
 - 4/5, 8/9
- Programmable Charge Pump Currents
- 3-Wire Serial Interface
- Digital Lock Detect
- Power Down Mode
- Pin Compatible With The ADF4110/1/2/3 Integer N

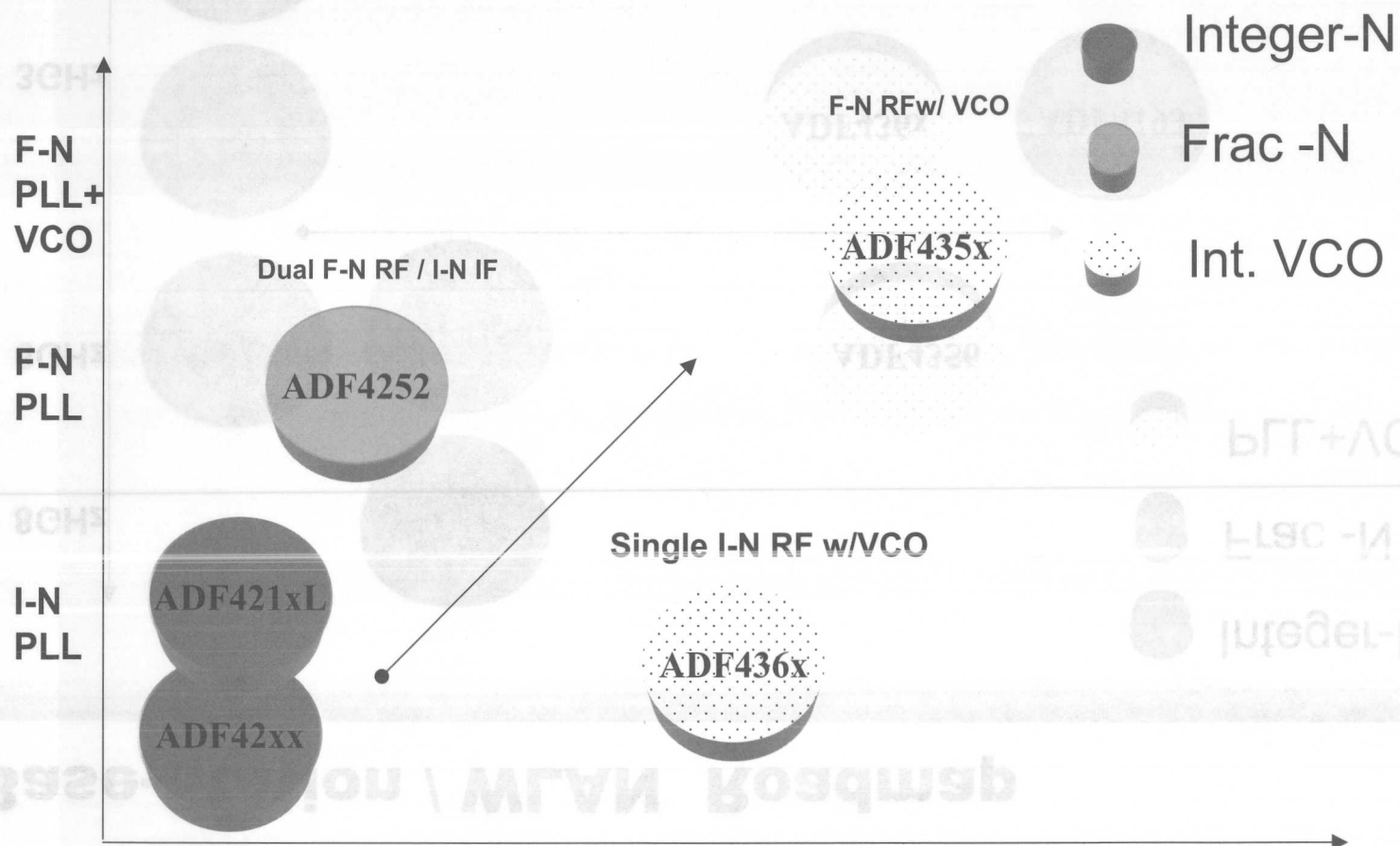
1st Silicon Results on ADF4156



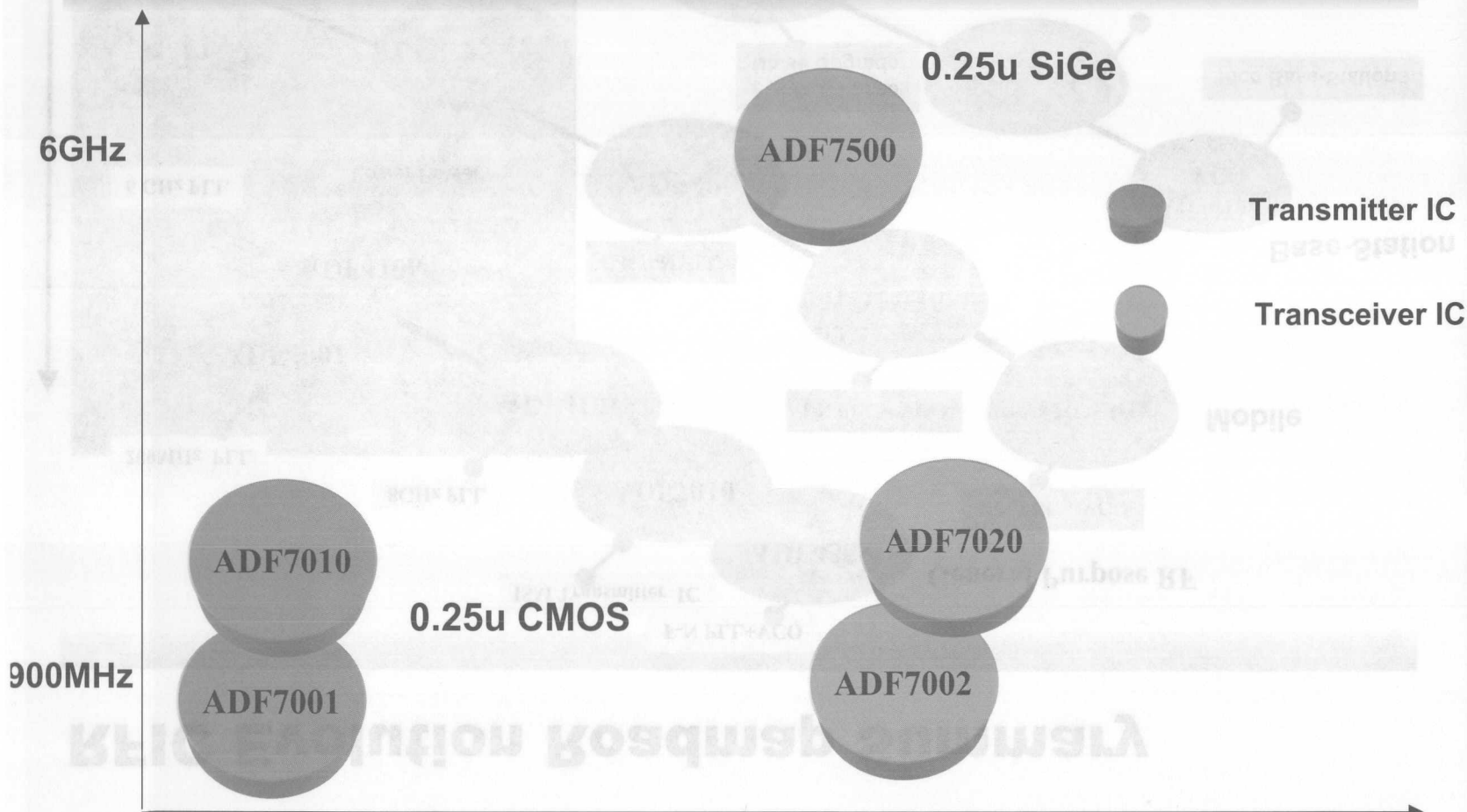
Base-Station / WLAN Roadmap



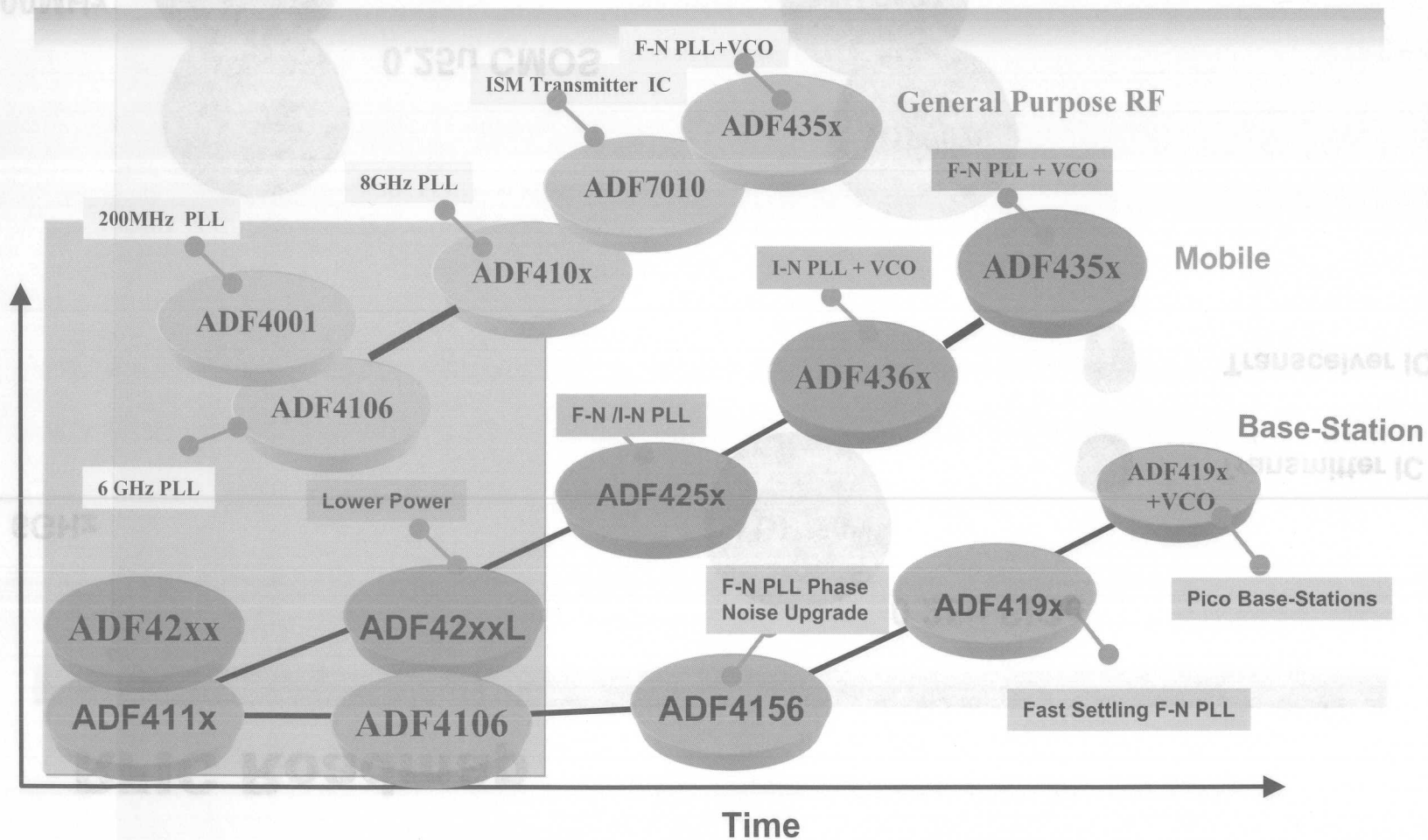
Mobile Platform Roadmap



RFIC Roadmap



RFIC Evolution Roadmap Summary



PLL Design Software

ADI SimPLL™

*PLL Design & Simulation
for Analog Devices PLL's*



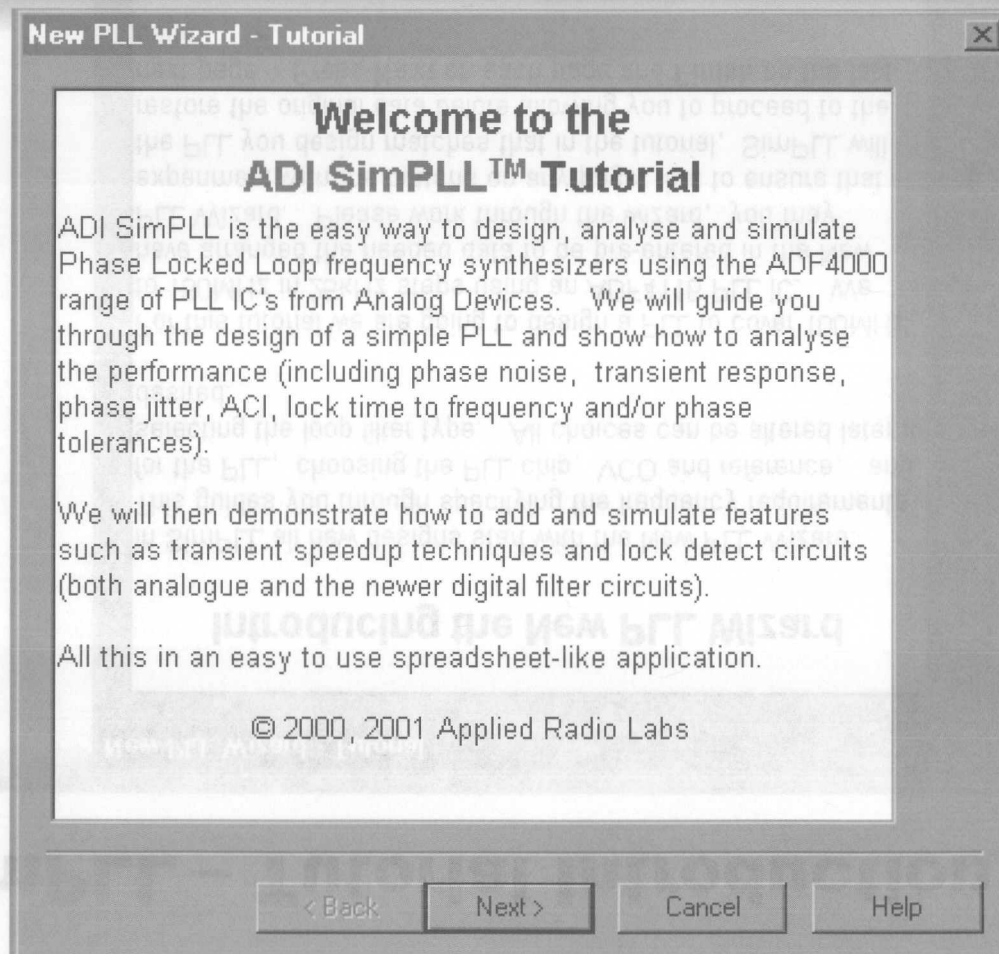
**Applied
Radio
Labs**

ADIsimPLL

PLL DESIGN AND SIMULATION SOFTWARE

This software has been developed for the sole purpose of optimizing PLL designs, making it faster and easier to accomplish individual goals. From the entry-level engineer to the seasoned veteran, ADIsimPLL has an arsenal of onboard tools and options that are guaranteed to maximize the efficiency of PLL circuit design.

ADIsimPLL – Tutorial Opening Screen



ADIsimPLL – Tutorial Introduction

New PLL Wizard - Tutorial

Introducing the New PLL Wizard

In SimPLL all new designs start with the New PLL Wizard. This guides you through specifying the frequency requirements for the PLL, choosing the PLL chip, VCO and reference, and selecting the loop filter type. All choices can be altered later if desired.

For this tutorial we are going to design a PLL to cover 100MHz to 130MHz in 25kHz steps using an ADF4116 PLL IC. We have arranged the needed data to be pre-entered in the New PLL Wizard. Please work through the wizard, you may experiment with the buttons on any page, but to ensure that the PLL you design matches that in the tutorial, SimPLL will restore the original data before allowing you to proceed to the next page. Press **Next** on each page and **Finish** on the last page.

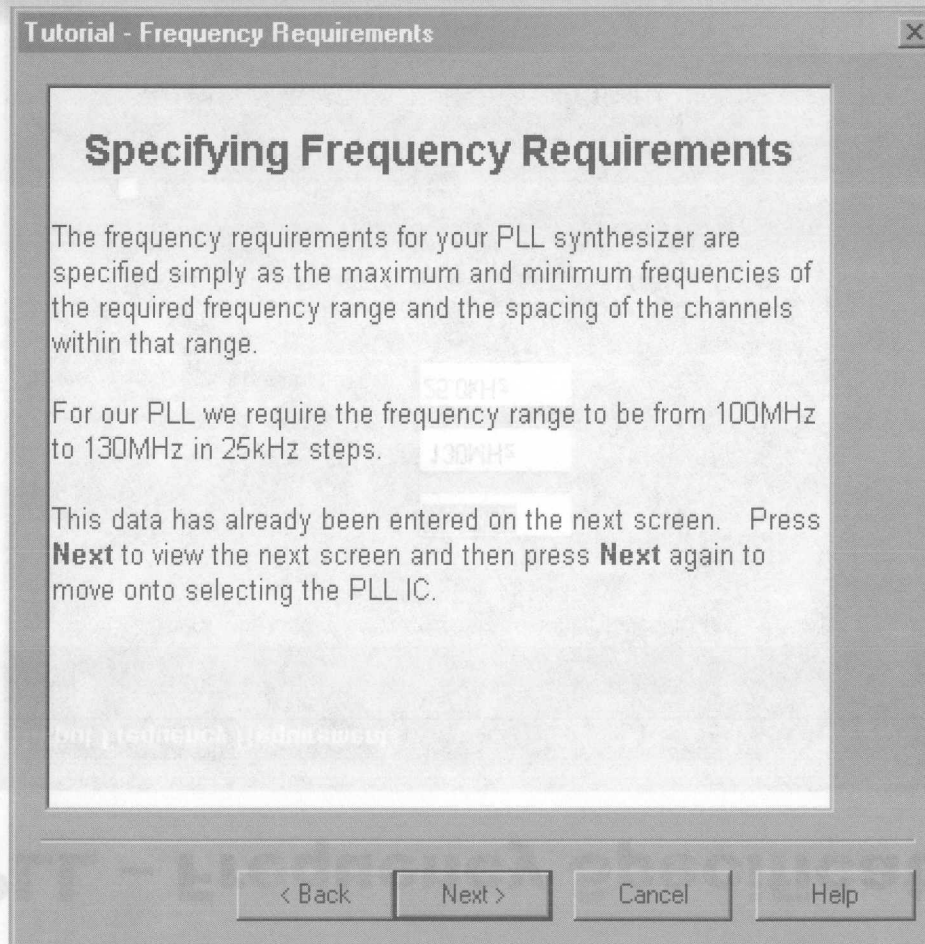
< Back

Next >

Cancel

Help

ADIsimPLL – Specification Instructions



ADIsimPLL – Frequency Specifications

Output Frequency Requirements

Specify the Output Frequency requirements for your PLL synthesizer

Minimum Frequency

Maximum Frequency

Channel Spacing

If you have a given reference frequency that you must use then check the box below and enter the frequency. Otherwise the reference frequency can be selected later.

☐ Use Reference Frequency of:

All frequencies are entered in Hz. To enter 10MHz simply type "10M" or "10e6", to enter 22.5kHz type "22.5k" or "22.5e3" and so on.

< Back

Next >

Cancel

Help

ADIsimPLL – Chip Selection

PLL Chip Selection

Select PLL Chip

☒ Integer-N
 ☐ Fractional-N

Select the ADF series PLL synthesizer chip

View Selection Guide

☒ Only show chips covering frequency range

Chip

ADF4116

View Datasheet

ADF4116 - Integer-N PLL chip

Frequency range from 80.0MHz to 550MHz

Reference Frequency to 100MHz

Phase Detector Maximum Frequency: 55.0MHz

Select Chip options to use:

Lock Detect

☐ None
 ☐ Voltage O/P
 ☒ Open Drain O/P
 ☐ Digital Filter

Speedup Type

☒ None
 ☐ Switched R1

< Back

Next >

Cancel

Help

ADIsimPLL – VCO Selection

VCO Selection

Select the VCO you wish to use, or choose 'custom' to enter detailed VCO characteristics later

☐ From Library

VCO Library

VCO Model

☒ Custom

Kv

For a custom VCO, enter the desired Kv in Hz/V (this can be changed later). For example, to enter 10MHz/V simply enter '10M' or '10e6'. Phase noise data can be entered later.

< Back

Next >

Cancel

Help

ADIsimPLL – Reference Selection

PLL Reference Selection

Reference frequency must be between 25.00kHz and 100.0MHz
and a multiple of 25.00kHz

To use a crystal oscillator choose "custom" and enter the
crystal frequency. For an external reference oscillator
select it from the library, or use custom and enter the

☐ From Library

Ref. Library

Ref. Model

☒ Custom Frequency

For a custom Reference, enter the desired frequency in
Hz. For example, to enter 10MHz simply enter '10M' or
'10e6' Phase noise details can be entered later.

< Back

Next >

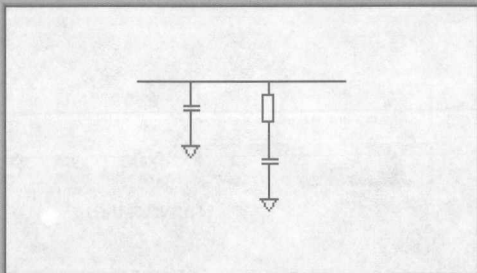
Cancel

Help

ADIsimPLL – Loop Filter Selection

Loop Filter Selection

Select the Loop Filter configuration. Filters shown match the Phase Detector and Speedup Mode selected earlier.



<< Prev
Select
Next >>

Op Amp Selection

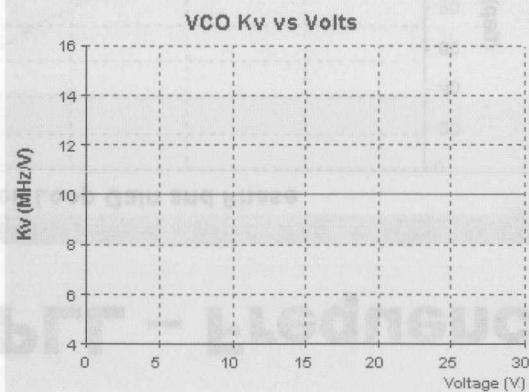
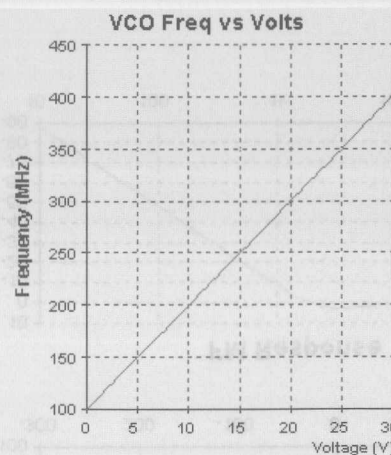
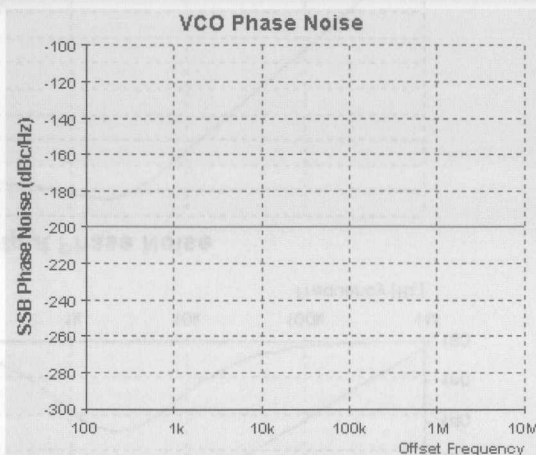
☒ Ideal
Op Amp Library
AnalogDevices

☐ Custom
Op Amp Model
AD711

☐ Library

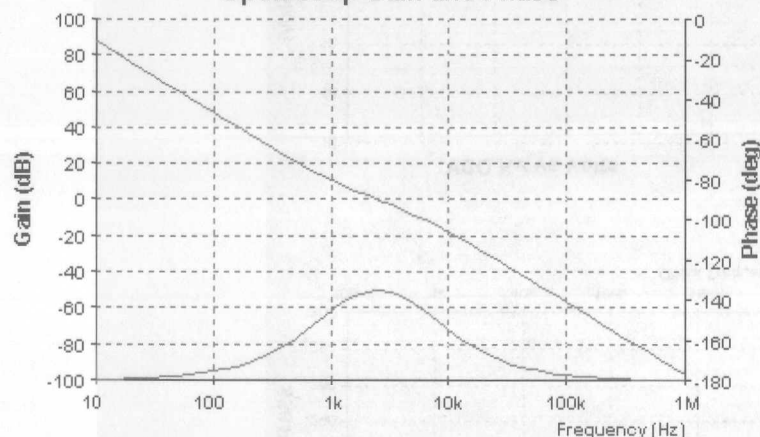
< Back
Finish
Cancel
Help

ADIsimPLL – VCO Results

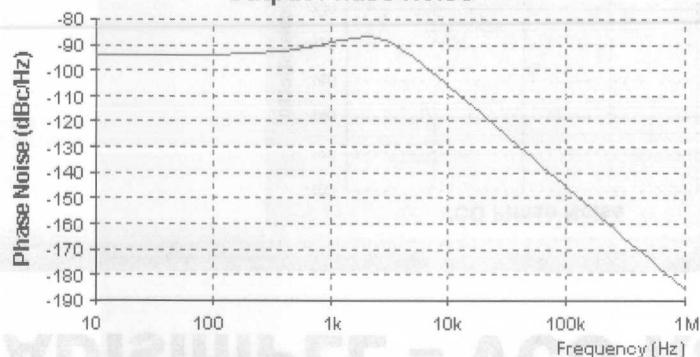


ADIsimPLL – Frequency Domain Results

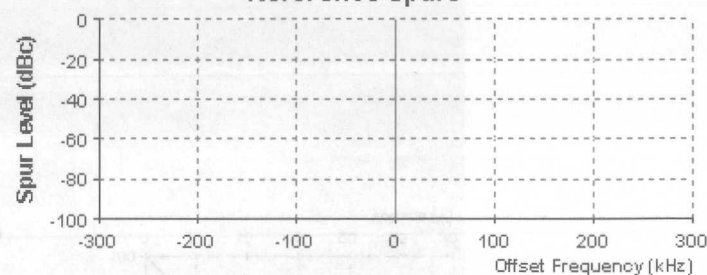
Open Loop Gain and Phase



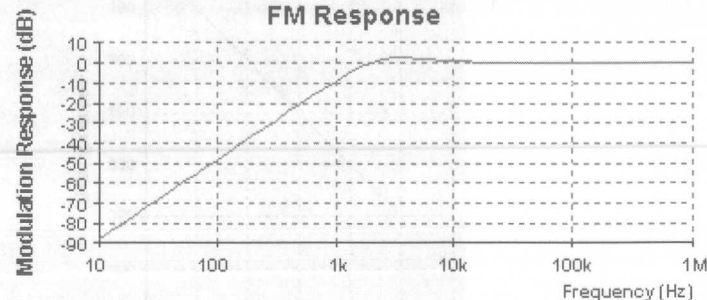
Output Phase Noise



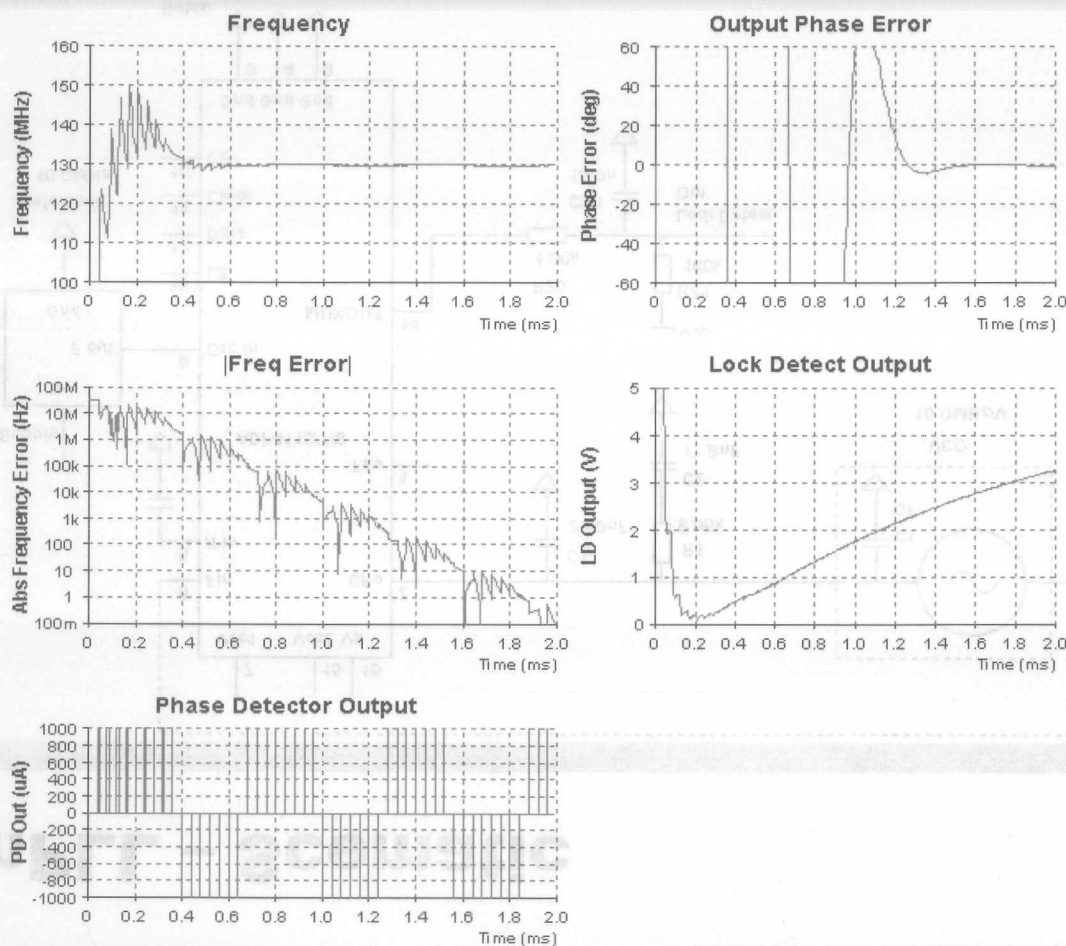
Reference Spurs



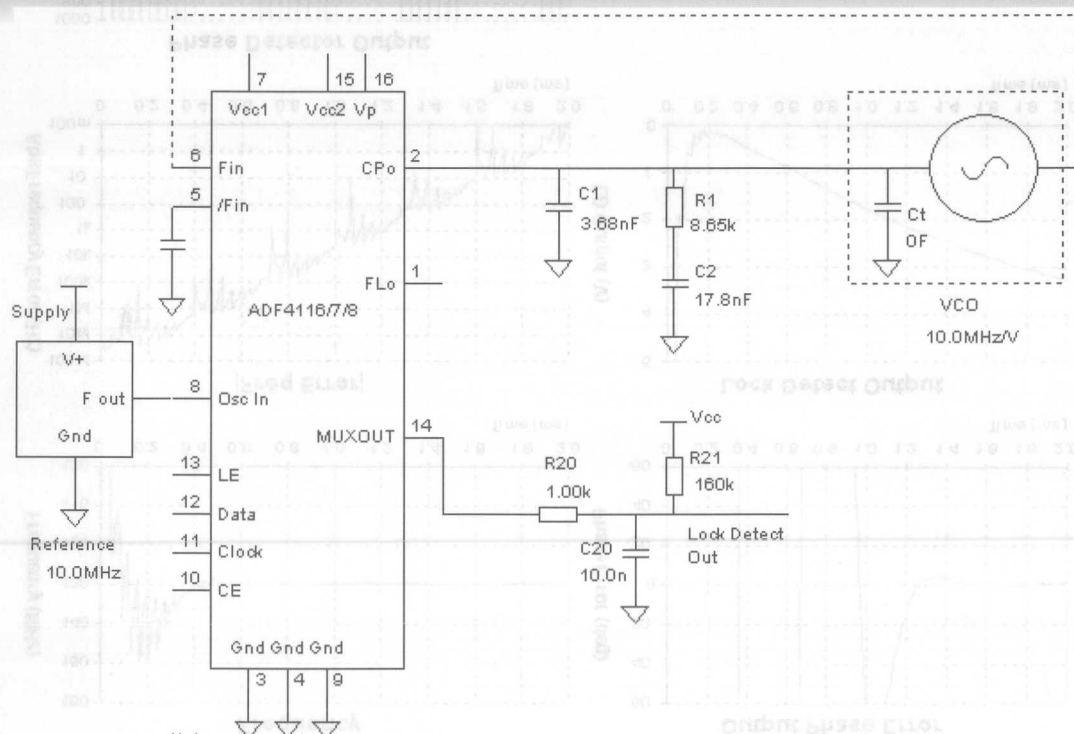
FM Response



ADIsimPLL – Time Domain Results



ADIsimPLL – Schematic



Notes:

1. TSSOP pin numbers shown
2. Vcc1 Analog Vcc
3. Vcc2 Digital Vcc
4. Vp Charge Pump power supply
5. Vcc1 = Vcc2, Vp >= Vcc1,2
6. CE = 0V powers down chip
7. Consult manufacturer's data sheet for full details

ADIsimPLL – Frequency Domain Report

Design1 analysed at 07/23/02 07:02:53

PLL Chip is ADF4116

VCO is custom

Reference is custom

Frequency Domain Analysis of PLL

Analysis at PLL output frequency of 114MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-93.73	--	--	-93.81	-111.5
1.00k	-88.97	--	--	-91.73	-92.25
10.0k	-106.0	--	--	-110.5	-107.9
100k	-145.7	--	--	-150.3	-147.6
1.00M	-185.7	--	--	-190.3	-187.6

Phase jitter using brick wall filter

from 10.0kHz to 100kHz

Phase Jitter **0.02 degrees rms**

Carrier Recovery phase jitter

Carrier recovery bandwidth 6.40kHz damping factor 0.7071

Symbol Filter cutoff 32.0kHz Butterworth with 3 poles

Phase Jitter **0.09 degrees rms**

Residual FM

from 300 Hz to 5.00kHz is **8.52 Hz**

FM SNR

sinusoidal modulation with 10.0kHz peak deviation

Signal to Noise Ratio = **58.4 dB**

ACP - Channel 1

Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz

Power in channel = **-78.6dBc**

---- End of Frequency Domain Results ----

ADIsimPLL – Time Domain Report

Transient Analysis of PLL

Frequency change from 100MHz to 130MHz

Simulation run for 2.00ms

Frequency Locking

Time to lock to 1.00kHz is 1.21ms

Time to lock to 10.0 Hz is 1.60ms

Phase Locking (VCO Output Phase)

Time to lock to 10.0 deg is 1.21ms

Time to lock to 1.00 deg is 1.48ms

Lock Detect Threshold

Time to lock detect exceeds 2.50 V is 1.42ms

---- End of Time Domain Results ----

ADIsimPLL

- Support
- User's Forum:
 - <http://www.radiolab.com.au/Forums/>



more products view

0-83



- <http://www.analog.com/formulas>
- User's Forum

Products

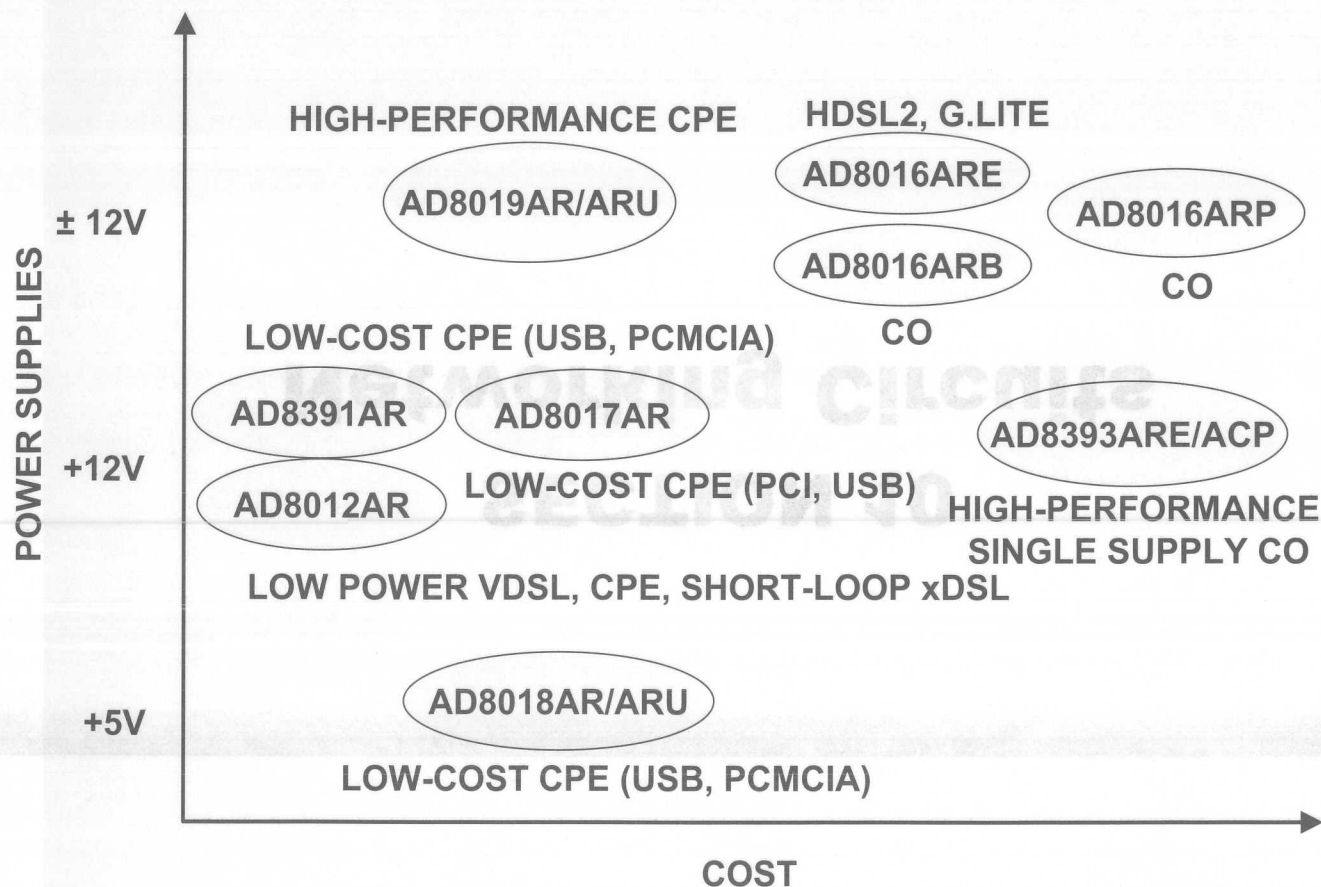
ADISIMB1



www.analog.com

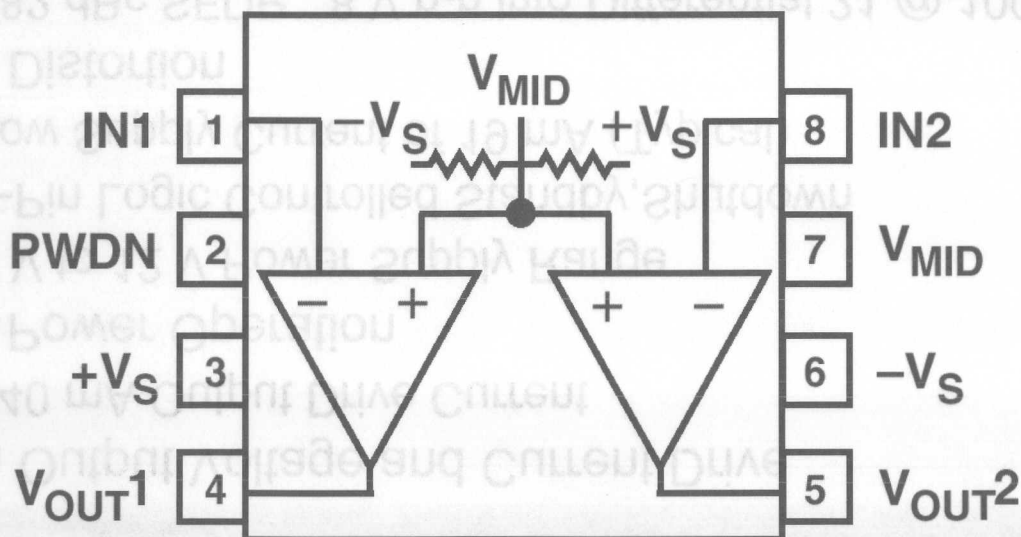
9-86

Current DSL Line Driver Positioning



AD8391 xDSL Line Driver

Ideal xDSL line driver for V_O DSL or low power applications such as USB, PCMCIA, or PCI-based Customer Premise Equipment (CPE).



Thermal Coastline
8-Pin SOIC

AD8391 xDSL Line Driver

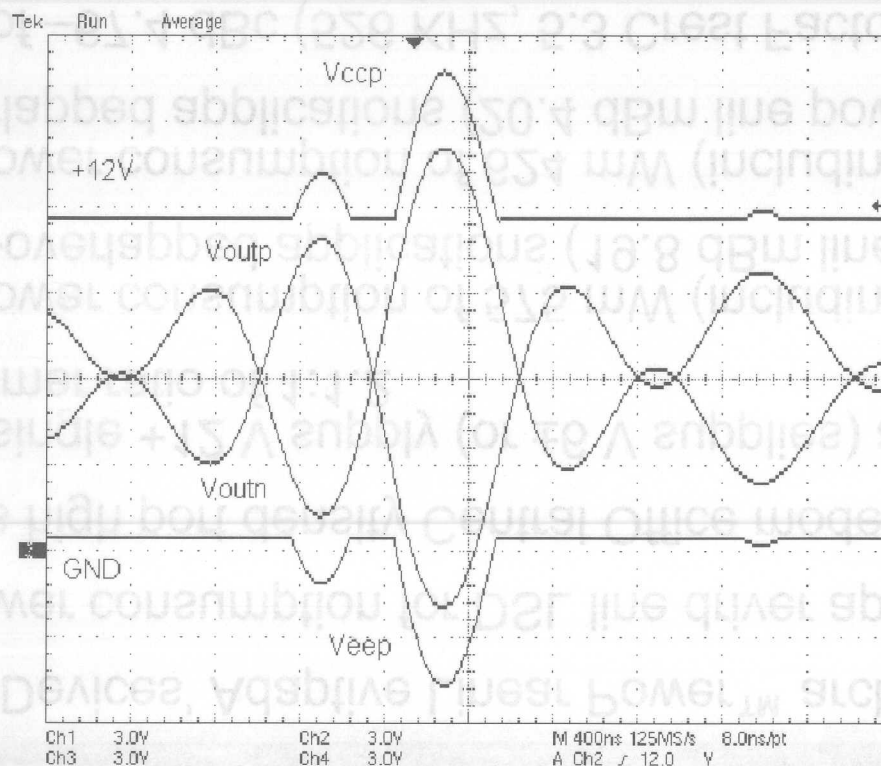
3 V to 12 V with Power-Down

- High Output Voltage and Current Drive
 - 340 mA Output Drive Current
- Low Power Operation
 - 3 V to 12 V Power Supply Range
 - 1-Pin Logic Controlled Standby, Shutdown
 - Low Supply Current of 19 mA (Typical)
- Low Distortion
 - -82 dBc SFDR, 8 V p-p into Differential 21 Ω @ 100 kHz
 - 4.5 nV/ $\sqrt{\text{Hz}}$ Input Voltage Noise Density, 100 kHz
 - Out-of-Band SFDR = -72 dBc, 144 kHz to 500 kHz, $Z_{\text{LINE}} = 100$, $P_{\text{LINE}} = 13.5$ dBm
- High Speed
 - 40 MHz Bandwidth (-3 dB)
 - 375 V/ μs Slew Rate

AD8393 Adaptive Linear Power™ **+12V ADSL-CO Line Driver**

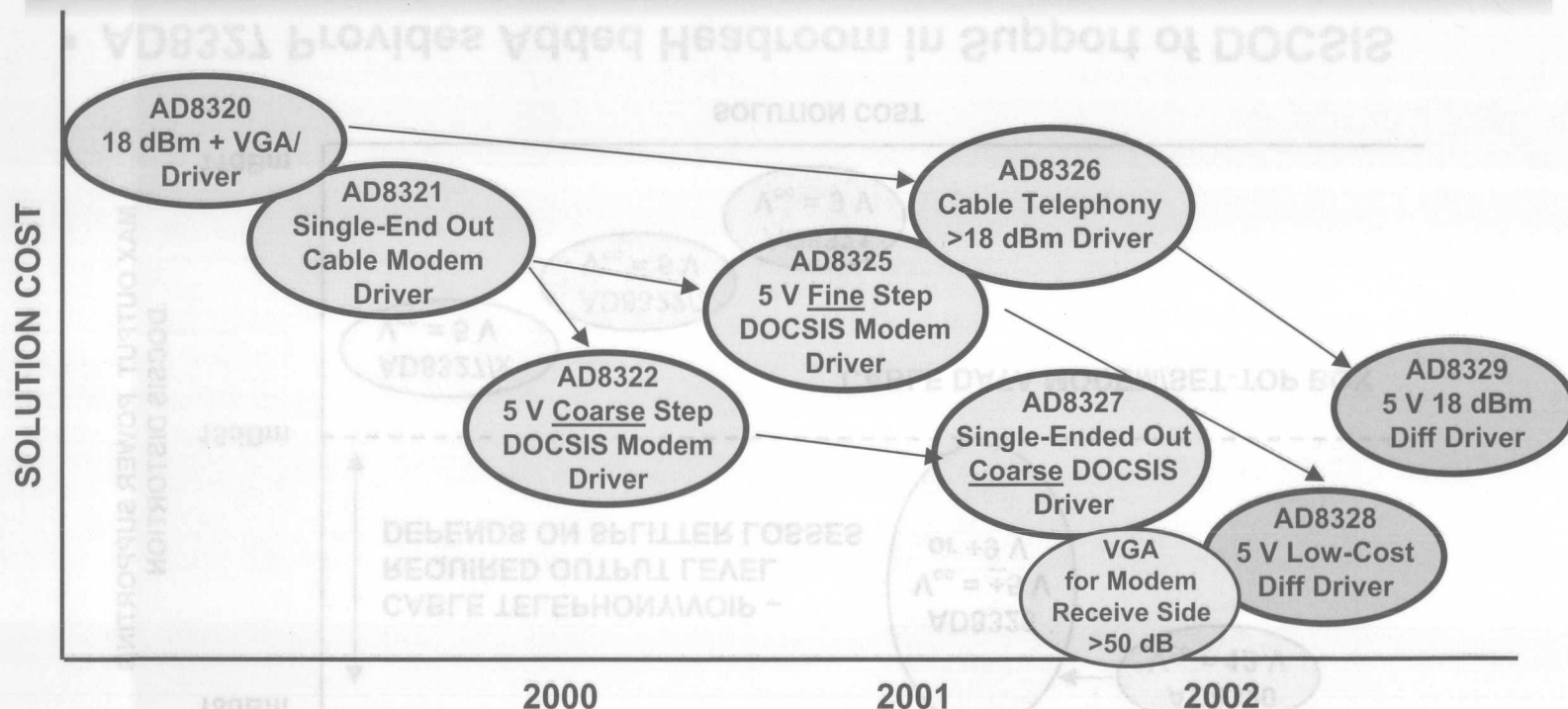
- Analog Devices' Adaptive Linear Power™ architecture
- Low power consumption for DSL line driver applications
- Enables high port density Central Office modems.
- Allows single +12 V supply (or ± 6 V supplies) and a transformer ratio of 1:1.2
- Total Power consumption of 575 mW (including line power) for non-overlapped applications (19.8 dBm line power)
- Total Power consumption of 624 mW (including line power) for overlapped applications (20.4 dBm line power).
- MTPR of -67.4 dBc (526 KHz, 5.3 Crest Factor, non-overlapped, $R_L = 70 \Omega$)
- Available in 32L 5 x 5 mm LFCSP and 28L TSSOP and packages.

AD8393 Adaptive Linear Power™ +12V ADSL-CO Line Driver



AD8393 single +12V supply operation showing Adaptive Linear Power™ supplies and driver outputs. Internally, the supplies (Vccp, Vcep) are brought outside the rails to accommodate peaks above 12 V and below GND.

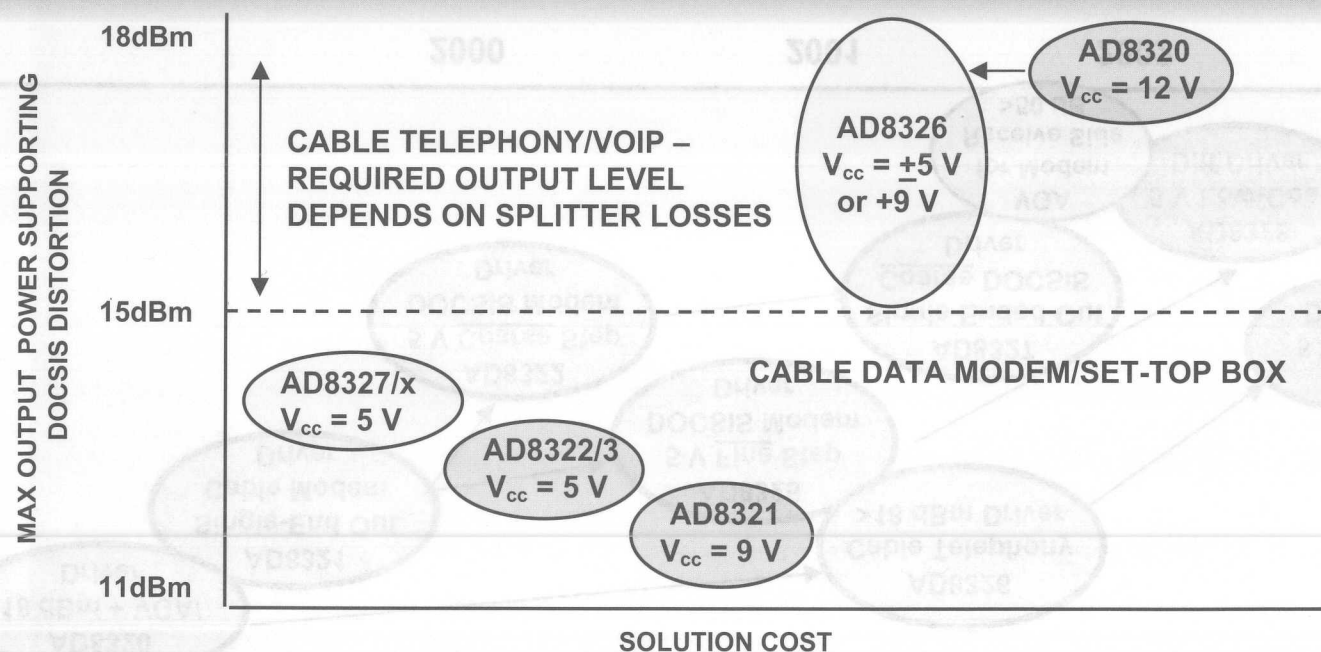
CATV Product Roadmap



- Value Proposition
- Continued Focus on Solution Cost Reduction for DOCSIS Cable Modems and Set-Top Boxes
 - CMOS driver (AD8328) will have lowest "solution cost" in the market available
 - BiCMOS driver (AD8329) will have a higher output power while maintaining a low cost

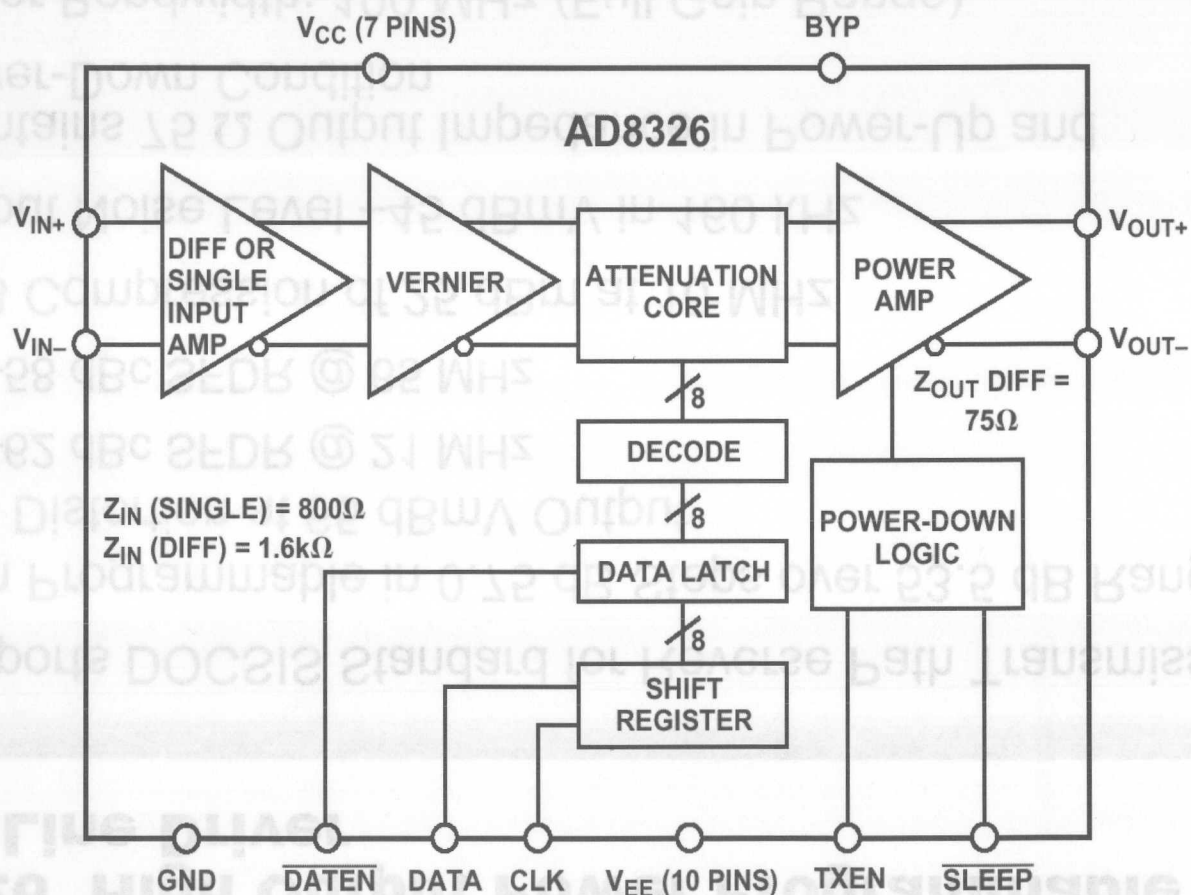
CATV Line Driver Positioning

Output Power Performance vs. Solution Cost



- AD8327 Provides Added Headroom in Support of DOCSIS Distortion Performance
- Low Distortion Results in Reduced “Adjacent Channel Power” (ACP) “Splatter” and Yielding Lower System Bit Error Rate

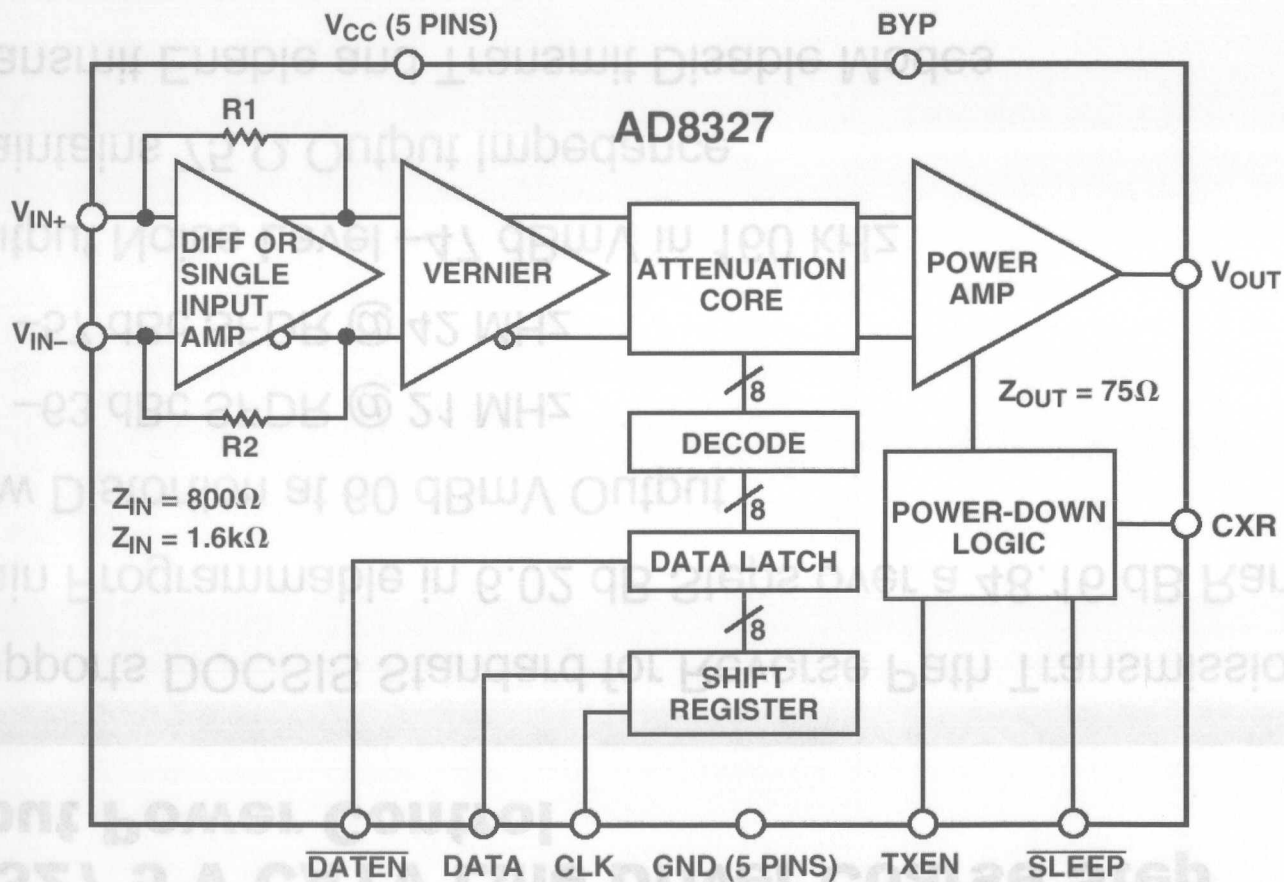
AD8326 High Output Power Programmable CATV Line Driver



AD8326 High Output Power Programmable CATV Line Driver

- Supports DOCSIS Standard for Reverse Path Transmission
- Gain Programmable in 0.75 dB Steps over 53.5 dB Range
- Low Distortion at 65 dBmV Output
 - -62 dBc SFDR @ 21 MHz
 - -58 dBc SFDR @ 65 MHz
- 1 dB Compression of 25 dBm at 10 MHz
- Output Noise Level -45 dBmV in 160 kHz
- Maintains 75 Ω Output Impedance in Power-Up and Power-Down Condition
- Upper Bandwidth: 100 MHz (Full Gain Range)
- Single- or Dual-Supply Operation

AD8327 5 V CATV Line Driver Coarse Step Output Power Control



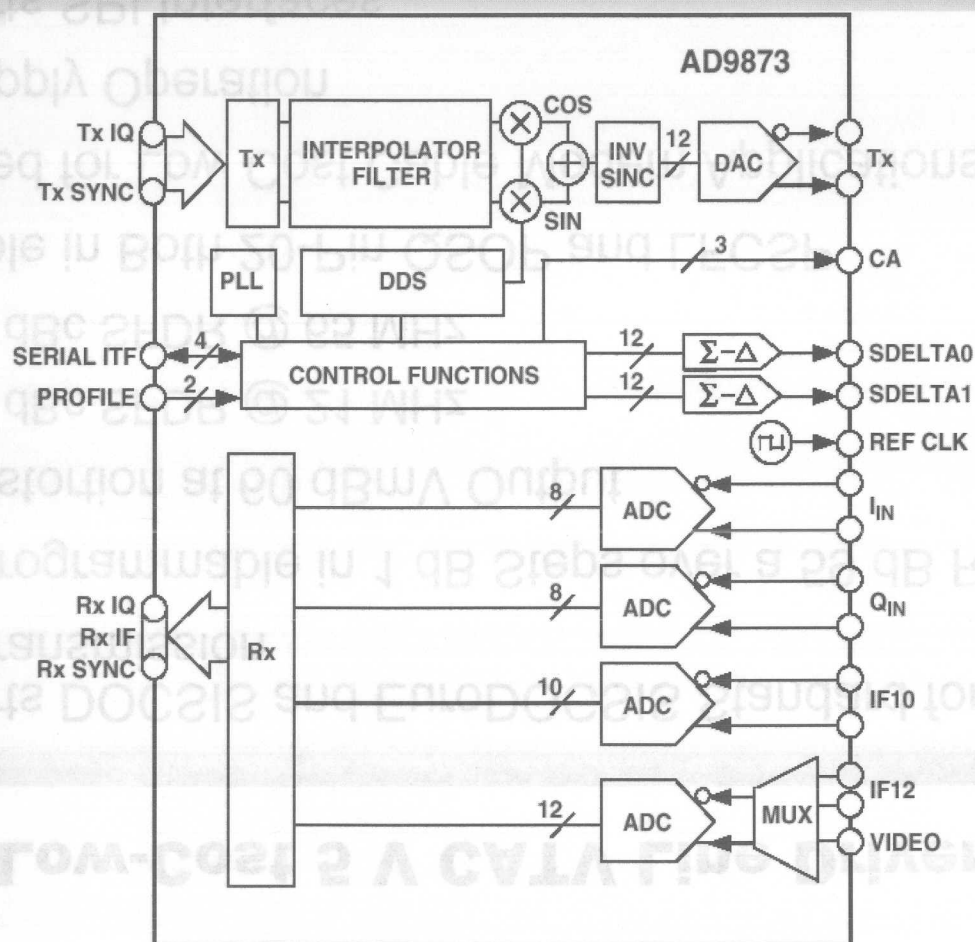
AD8327 5 V CATV Line Driver Coarse Step Output Power Control

- Supports DOCSIS Standard for Reverse Path Transmission
- Gain Programmable in 6.02 dB Steps over a 48.16 dB Range
- Low Distortion at 60 dBmV Output
 - -63 dBc SFDR @ 21 MHz
 - -57 dBc SFDR @ 42 MHz
- Output Noise Level -47 dBmV in 160 kHz
- Maintains 75 Ω Output Impedance
- Transmit Enable and Transmit Disable Modes
- 5 V Supply Operation
- Supports SPI Interfaces

AD8328 Low-Cost 5 V CATV Line Driver

- Supports DOCSIS and EuroDOCSIS Standard for Reverse Path Transmission
- Gain Programmable in 1 dB Steps over a 59 dB Range
- Low Distortion at 60 dBmV Output
 - -54 dBc SFDR @ 21 MHz
 - -52 dBc SFDR @ 65 MHz
- Available in Both 20-Pin QSOP and LFCSP
- Targeted for Low Cost Cable Modem Applications
- 5 V Supply Operation
- Supports SPI Interfaces

AD9873 Analog Front End Converter for Set-Top Box, Cable Modem



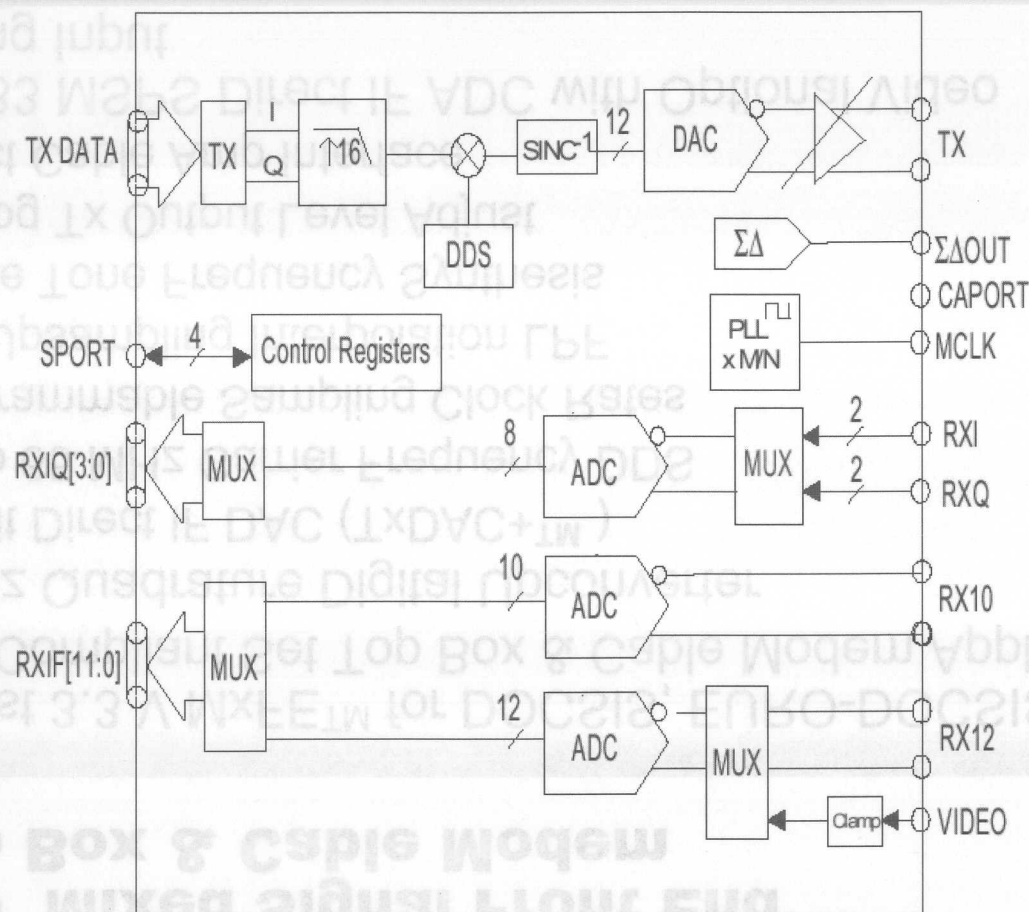
AD9873 Analog Front End Converter for Set-Top Box, Cable Modem

- Low-Cost 3.3 V CMOS Analog Front End Converter for MCNS-DOCSIS,DVB,DAVIC-Compliant Set-Top Box,Cable Modem Applications
- Direct interface to AD9873 153 65V Cable Driver
- 232 MHz Quadrature Digital Upconverter
 - DC to 65 MHz Output Bandwidth
 - 12-Bit Direct IF D/A Converter (TxDAC+®)
 - Programmable Reference Clock Multiplier (PLL)
 - Direct Digital Synthesis
 - Interpolator
 - SIN(x)/x Compensation Filter
 - Four Programmable,Pin-Selectable Modulator Profiles
 - Single-Tone Mode for Frequency Synthesis Applications

AD9873 Analog Front End Converter for Set-Top Box, Cable Modem

- 12-Bit, 33 MSPS Sampling Direct IF A/D Converter with Auxiliary Automatic Clamp Video Input Multiplexer
- 10-Bit, 33 MSPS Sampling Direct IF A/D Converter
- Dual 8-Bit, 16.5 MSPS Sampling IQ A/D Converter
- Two Independently Programmable Sigma-Delta Converters
- Direct Interface to AD8321/23 PGA Cable Driver
- Programmable Frequency Output
- Power-Down Modes

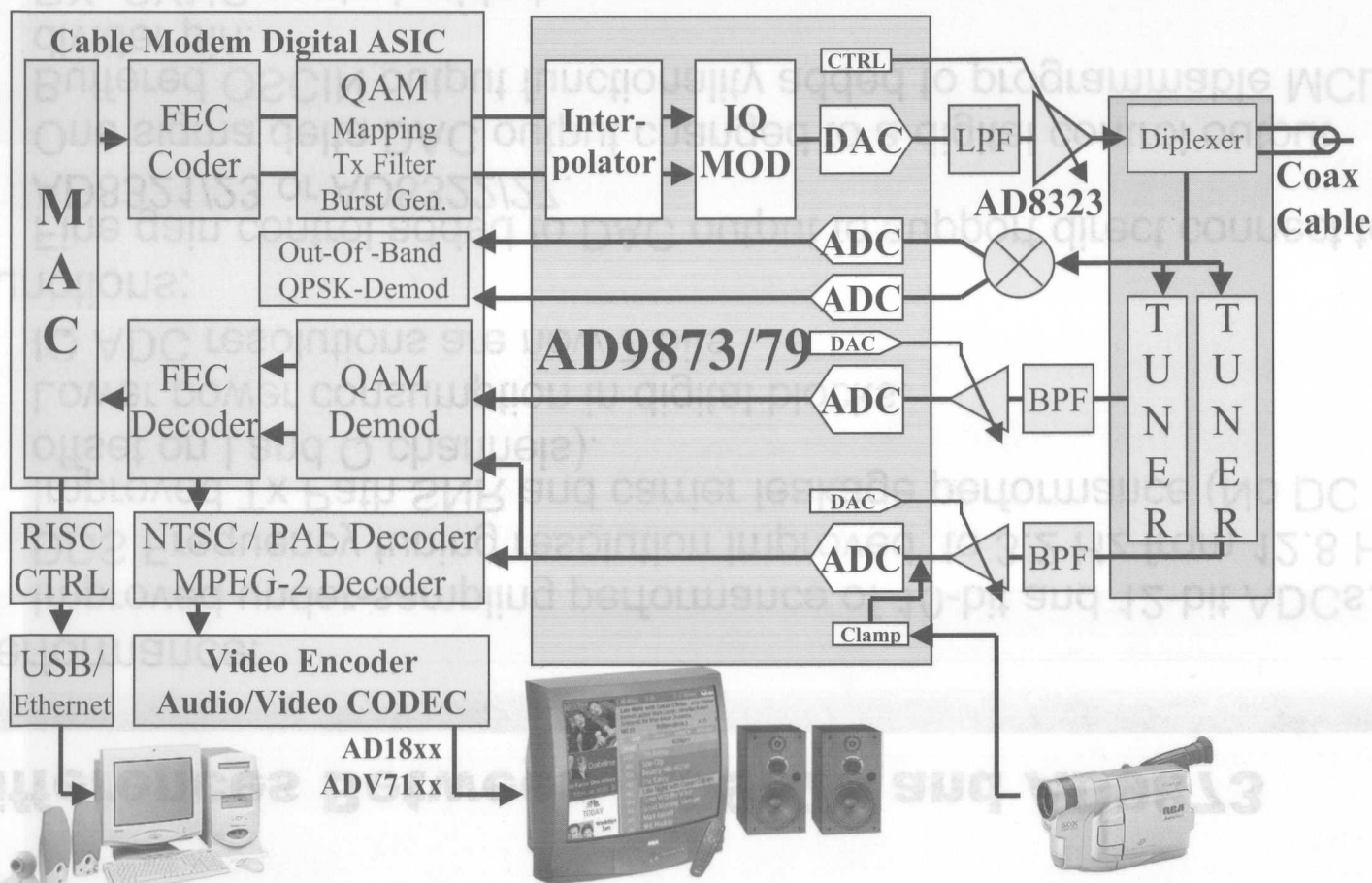
AD9879 Mixed Signal Front End Set Top Box & Cable Modem



AD9879 Mixed Signal Front End Set Top Box & Cable Modem

- Low Cost 3.3 V MxFE™ for DOCSIS, EURO-DOCSIS, DVB, DAVIC Compliant Set Top Box & Cable Modem Applications
- 232 MHz Quadrature Digital Upconverter
 - 12-Bit Direct IF DAC (TxDAC+™)
 - Up to 65 MHz Carrier Frequency DDS
 - Programmable Sampling Clock Rates
 - 16x Upsampling Interpolation LPF
 - Single Tone Frequency Synthesis
 - Analog Tx Output Level Adjust
 - Direct Cable Amp Interface
- 12-Bit, 33 MSPS Direct IF ADC with Optional Video Clamping Input
- 10-Bit, 33 MSPS Direct IF ADC
- Dual 7-Bit, 16.5 MSPS Sampling I/Q ADC
- 12-Bit Sigma Delta Auxiliary DAC

AD9873/79 Cable Modem - Set-Top Box



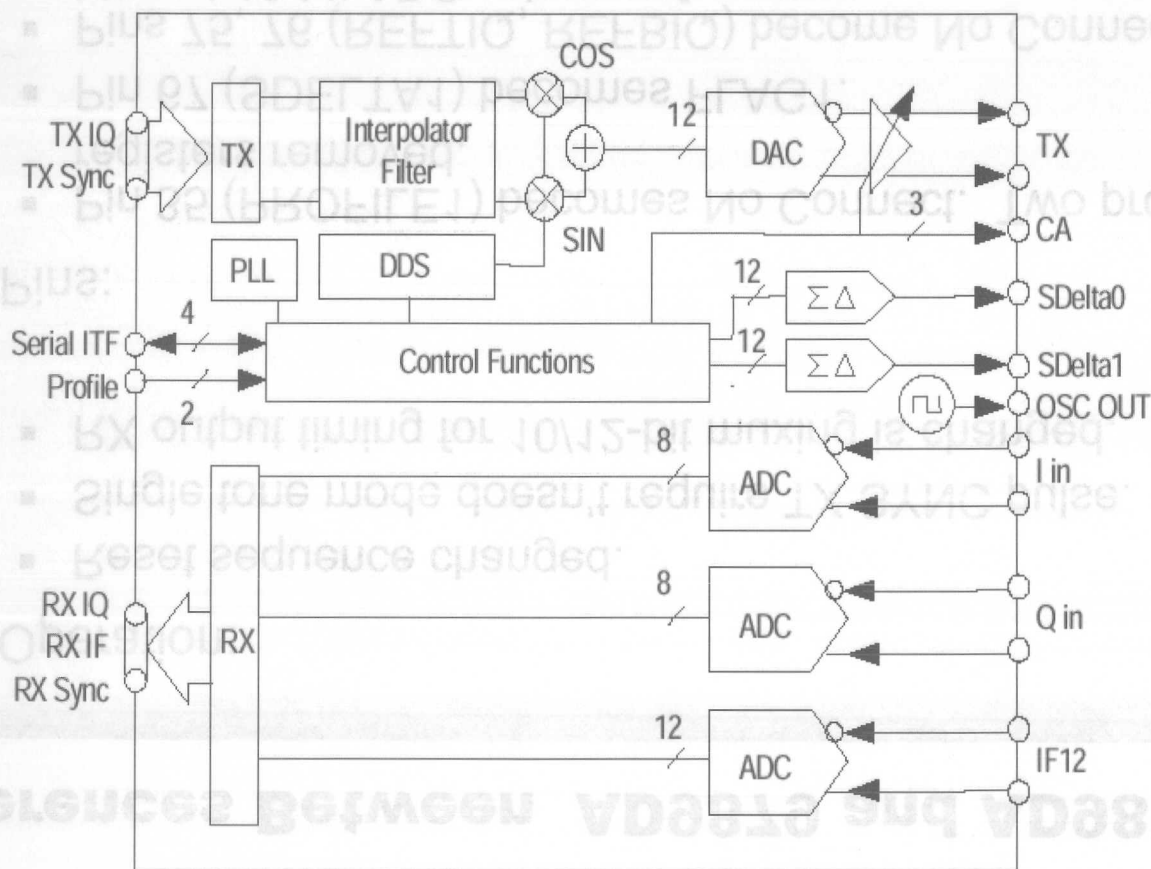
Differences Between AD9879 and AD9873

- Performance:
 - Improved under-sampling performance of 10-bit and 12-bit ADCs.
 - DDS Frequency tuning resolution improved to 3.2 Hz from 12.8 Hz.
 - Improved Tx Path SNR and carrier leakage performance (No DC offset on I and Q channels).
 - Lower power consumption in digital blocks.
 - IQ ADC resolutions are now 7 bits
- Functions:
 - Fine gain control added to DAC output to support direct connect to AD8321/23 or AD8322/27.
 - One sigma delta DAC output changed to a digital control output
 - Buffered OSCIN output functionality added to programmable MCLK divider pin.
 - RX_SYNC control added.
 - Programmable Output Edge Rate on Rx port.
 - 12x Interpolation mode (N=3) no longer supported
 - Number of Profile registers reduced from 4 to 2.

Differences Between AD9879 and AD9873

- Operation:
 - Reset sequence changed.
 - Single tone mode doesn't require TX SYNC pulse.
 - RX output timing for 10/12-bit muxing is changed.
- Pins:
 - Pin 35 (PROFILE1) becomes No Connect. Two profile registers removed.
 - Pin 67 (SDELTA1) becomes FLAG1.
 - Pins 75, 76 (REFTIQ, REFBIQ) become No Connects. 6-bit and 10-bit ADCs share reference.
 - Pin1 (AVDD) becomes No Connect.
 - Pins 77 & 80 (AGND IQ) become No Connects.

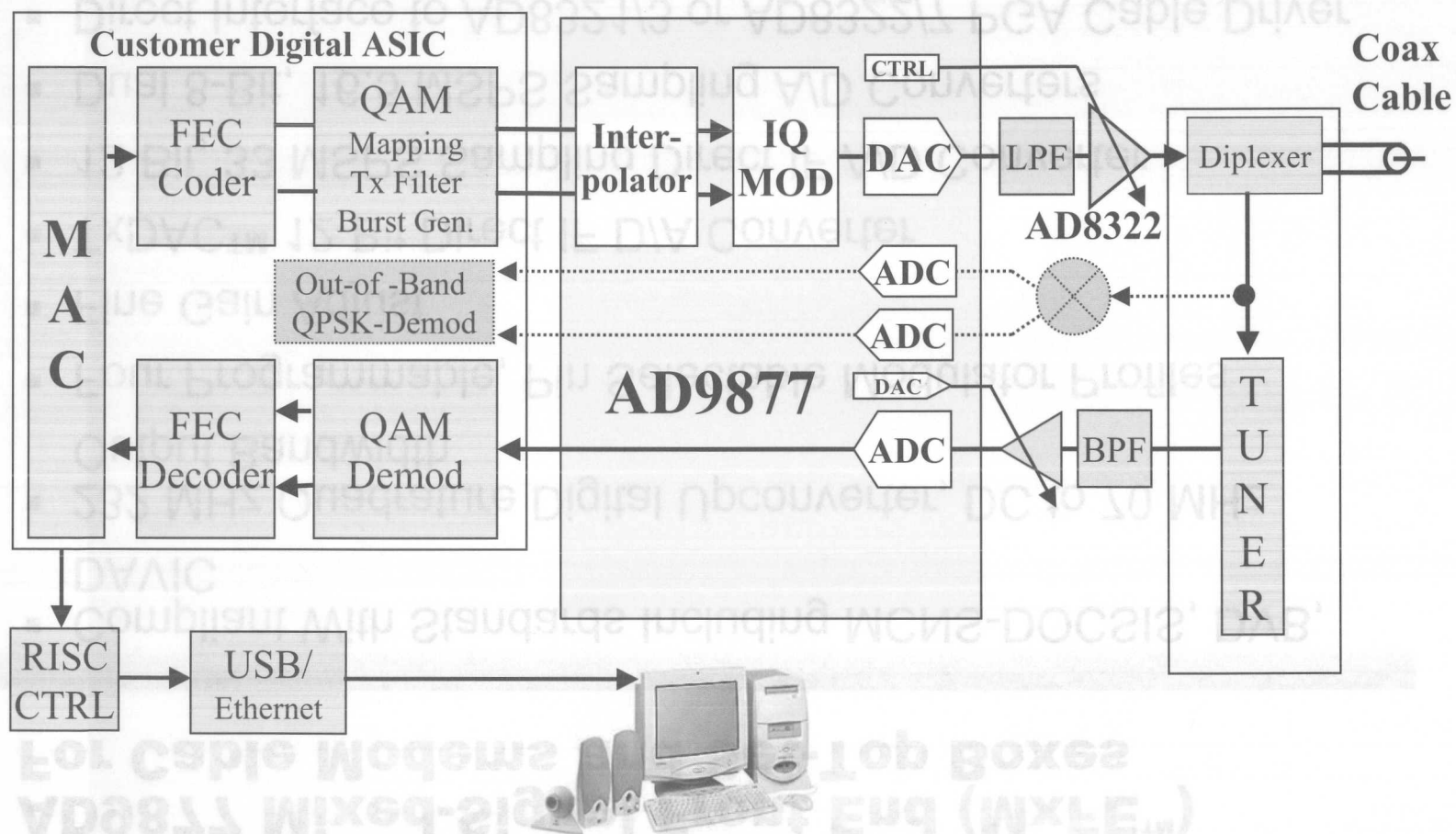
AD9877 Mixed-Signal Front End (MxFE™) For Cable Modems and Set-Top Boxes



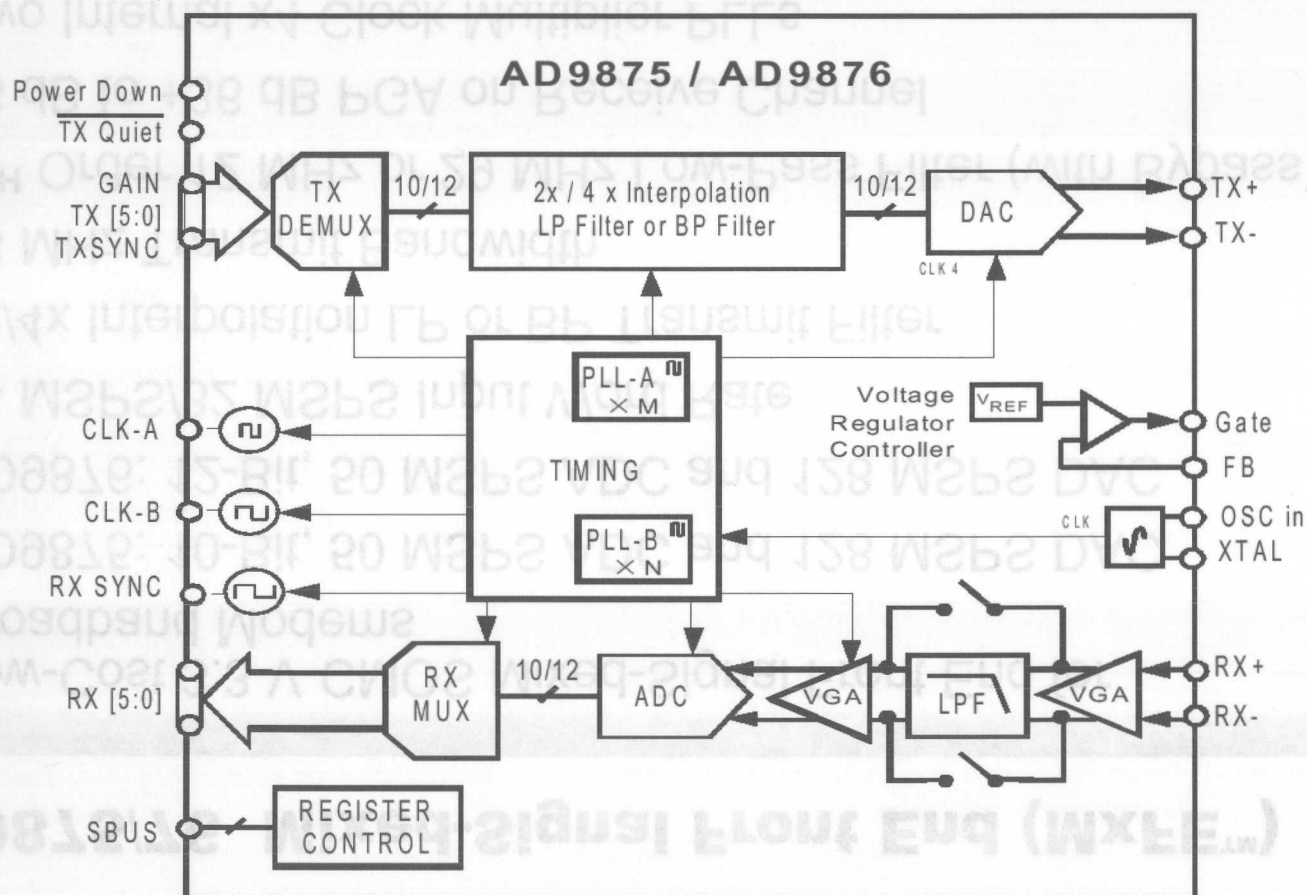
AD9877 Mixed-Signal Front End (MxFE™) For Cable Modems and Set-Top Boxes

- Compliant With Standards Including MCNS-DOCSIS, DVB, DAVIC
- 232 MHz Quadrature Digital Upconverter, DC to 70 MHz Output Bandwidth
- Four Programmable, Pin Selectable Modulator Profiles
- Fine Gain Adjust
- TxDAC™ 12-Bit Direct IF D/A Converter
- 12-Bit, 33 MSPS Sampling Direct IF A/D Converter
- Dual 8-Bit, 16.5 MSPS Sampling A/D Converters
- Direct Interface to AD8321/3 or AD8322/7 PGA Cable Driver
- Programmable Frequency Output
- Power-Down Modes

AD9877 Cable Modem Application



AD9875/76 Mixed-Signal Front End (MxFE™)



AD9875/76 Mixed-Signal Front End (MxFE™)

- Low-Cost 3.3 V-CMOS Mixed-Signal Front End for Broadband Modems
- AD9875: 10-Bit, 50 MSPS ADC and 128 MSPS DAC
- AD9876: 12-Bit, 50 MSPS ADC and 128 MSPS DAC
- 64 MSPS/32 MSPS Input Word Rate
- 2x/4x Interpolation LP or BP Transmit Filter
- 26 MHz Transmit Bandwidth
- 4TH Order 12 MHz or 29 MHz Low-Pass Filter (with Bypass)
- -6 dB to +36 dB PGA on Receive Channel
- Two Internal x4 Clock Multiplier PLLs
- Power-Down Mode
- 48-Lead LQFP Package

Home Networking and Wired BBA

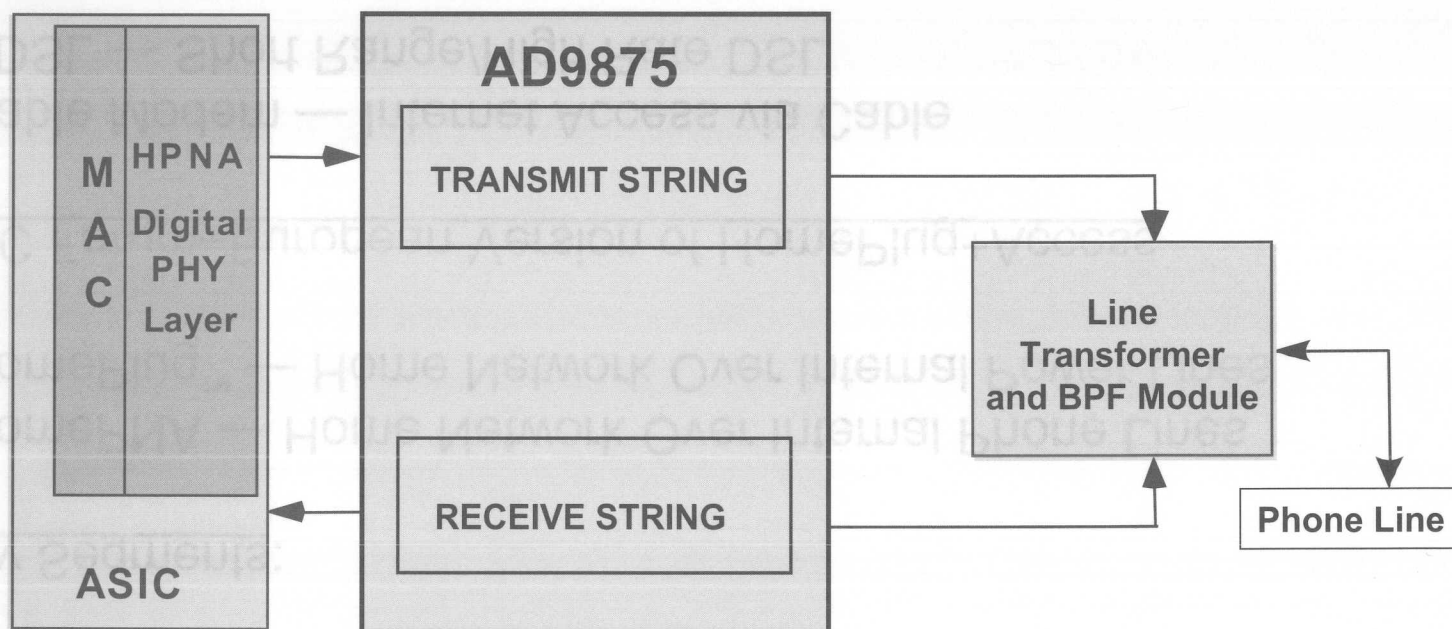
Key Segments:

- HomePNA — Home Network Over Internal Phone Lines
- HomePlug™ — Home Network Over Internal Power Lines

PLC Forum—European Version of HomePlug+Access

- Cable Modem — Internet Access via Cable
- VDSL — Short Range/High Rate DSL

HomePNA Modem Application



Home
Phoneline
Network
CERTIFIED™

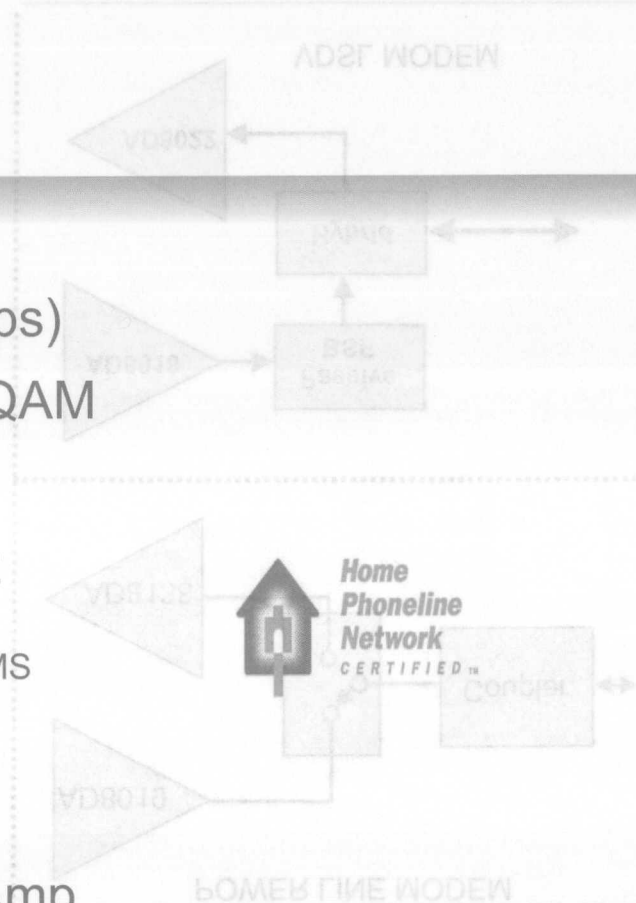
HomePNA Key Points

Technology:

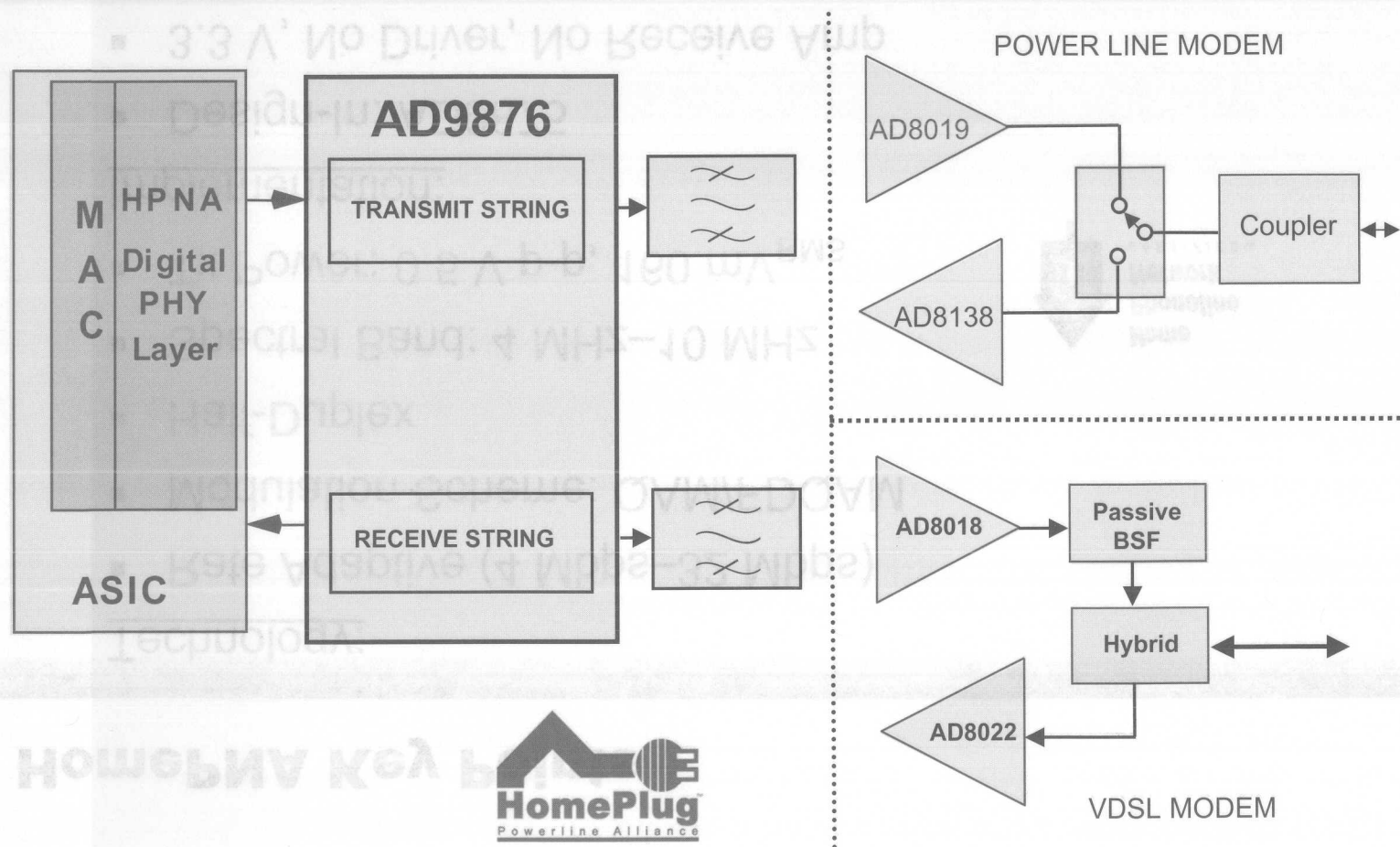
- Rate Adaptive (4 Mbps–32 Mbps)
- Modulation Scheme: QAM/FDQAM
- Half-Duplex
- Spectral Band: 4 MHz–10 MHz
- Tx Power: 0.5 V p-p, 160 mV_{RMS}

Implementation:

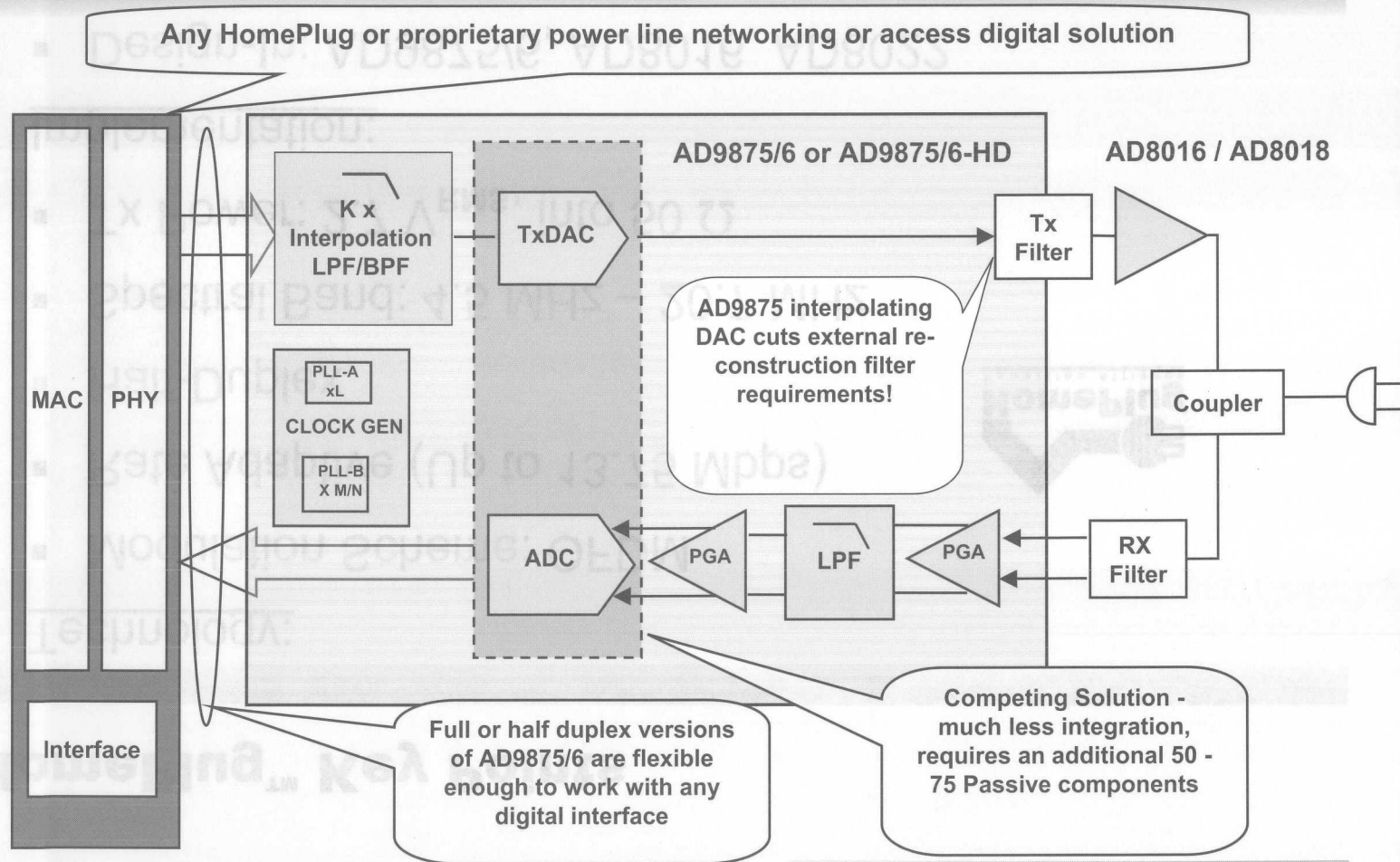
- Design-In: AD9875
- 3.3 V, No Driver, No Receive Amp
- Cheap, Small, Low Component Count



AD9876 Power Line Modem/VDSL Application



AD9875/6 Power Line Networking / Access



HomePlug™ Key Points

Technology:

- Modulation Scheme: OFDM
- Rate Adaptive (Up to 13.75 Mbps)
- Half-Duplex
- Spectral Band: 4.5 MHz – 20.7 MHz
- Tx Power: 2.7 V_{RMS}, into 50 Ω

Implementation:

- Design-In: AD9875/6, AD8016, AD8022
- 12 V, Needs Driver, Might Need Receive Amp



VDSL Key Points

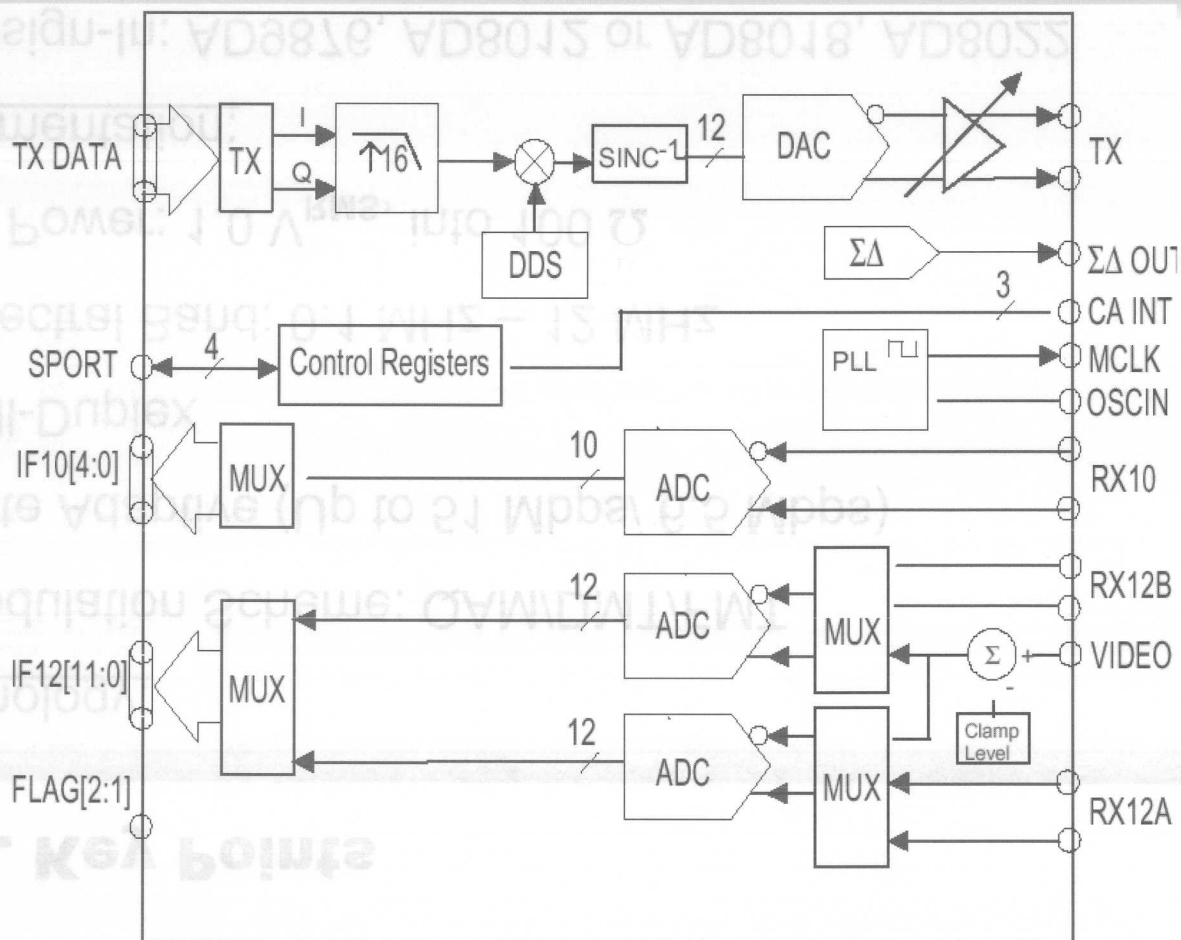
Technology:

- Modulation Scheme: QAM/DMT/FMT
- Rate Adaptive (Up to 51 Mbps/ 6.5 Mbps)
- Full-Duplex
- Spectral Band: 0.1 MHz – 12 MHz
- Tx Power: 1.0 V_{RMS}, into 100 Ω

Implementation:

- Design-In: AD9876, AD8012 or AD8018, AD8022
- 5 V, Low Power

AD9878 Mixed-Signal Front End (MxFE) for Set-Top Box, Cable Modem



AD9878 Mixed-Signal Front End (MxFE) for Set-Top Box, Cable Modem

- Low Cost 3.3 V-CMOS MxFE for DOCSIS, EURO-DOCSIS, DVB, DAVIC Compliant Set-Top Box and Cable Modem Applications
- 232 MHz Quadrature Digital Upconverter
 - 12-Bit Direct IF D/A Converter (TxDAC+[®])
 - Up to 65 MHz Carrier Frequency DDS
 - Programmable Sampling Clock Rates
 - Selectable Interpolation Filter
 - Analog Tx Output Level Adjust
- Dual 12-Bit, 29 MSPS Direct IF ADCs w/ Video Clamp I
- 10-Bit, 29 MSPS Sampling ADC
- 8-Bit Σ - Δ Auxiliary DAC
- Direct Interface to AD8321/23 or AD8322/27 PGA Cable Driver

Dual-Loop Laser Diode Drivers



ADN2841 AnyRate to OC-48/SDH-16 Dual-Loop Laser Diode Drivers

- 50 Mbps to 2.7 Gbps Operation
- 80 pS Rise and Fall Times (Typ)
- Modulation Current Range 5 mA to 80 mA
- Closed-Loop Control of Power and Extinction Ratio
 - Maintains optimal laser diode performance over temperature, lifetime, diode process variations, and diode supplier
 - Reduces diode tuning time required at assembly
- Full Current Parameter Monitoring
- Laser Fail and Laser Degrade Alarms
- Automatic Laser Shutdown, ALS
- Dual MPD Functionality for DWDM
- Optional Clocked Data
- Available in Two Package Sizes:
 - 32-Lead CSP — 5 mm x 5 mm
 - 48-Lead CSP — 7 mm x 7 mm

$$\text{Extinction Ratio} = \frac{P_0}{P_1}$$

$$\text{Average Power} = \frac{P_0 + P_1}{2}$$

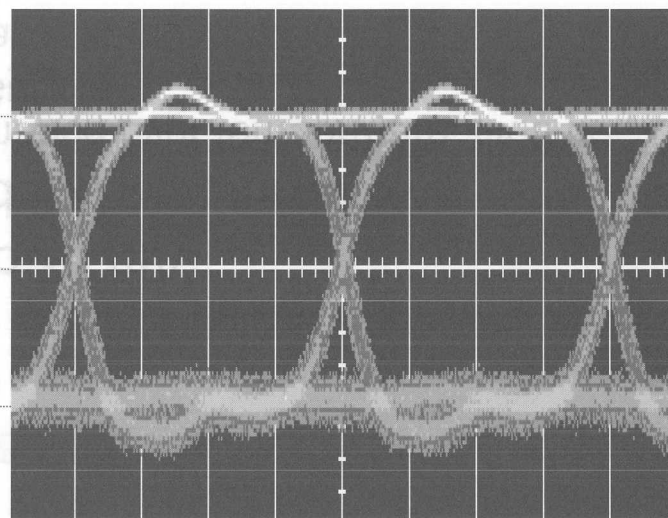
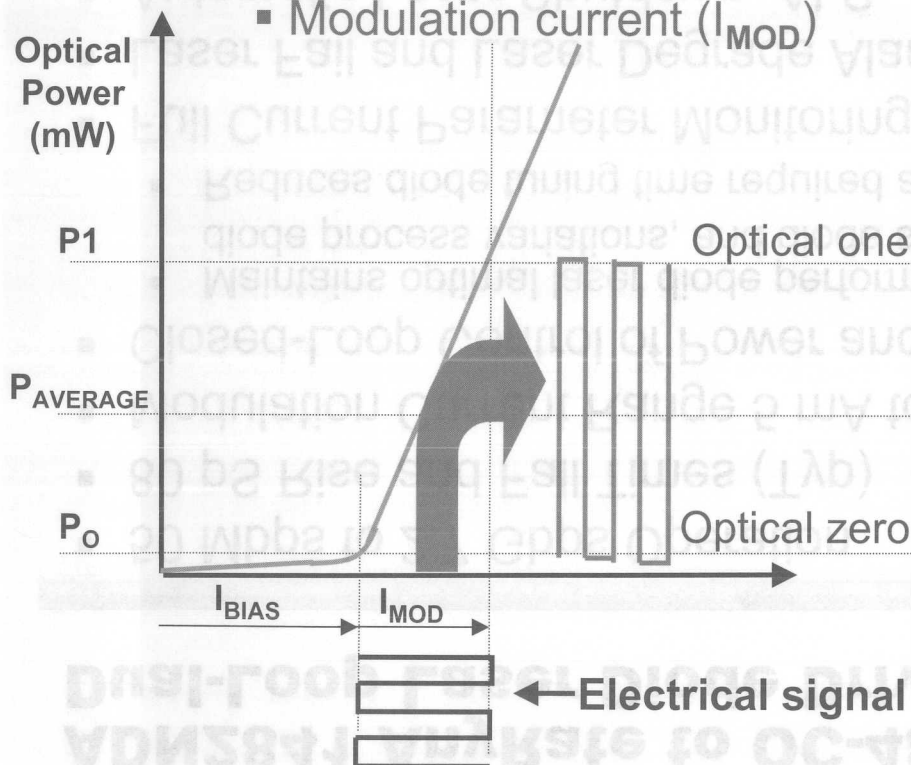
Dual-Loop Control Quick Tutorial: Understanding Laser Diode Transfer Function

- A Laser Diode is Driven with Two Currents:

- Bias current (I_{BIAS})
- Modulation current (I_{MOD})

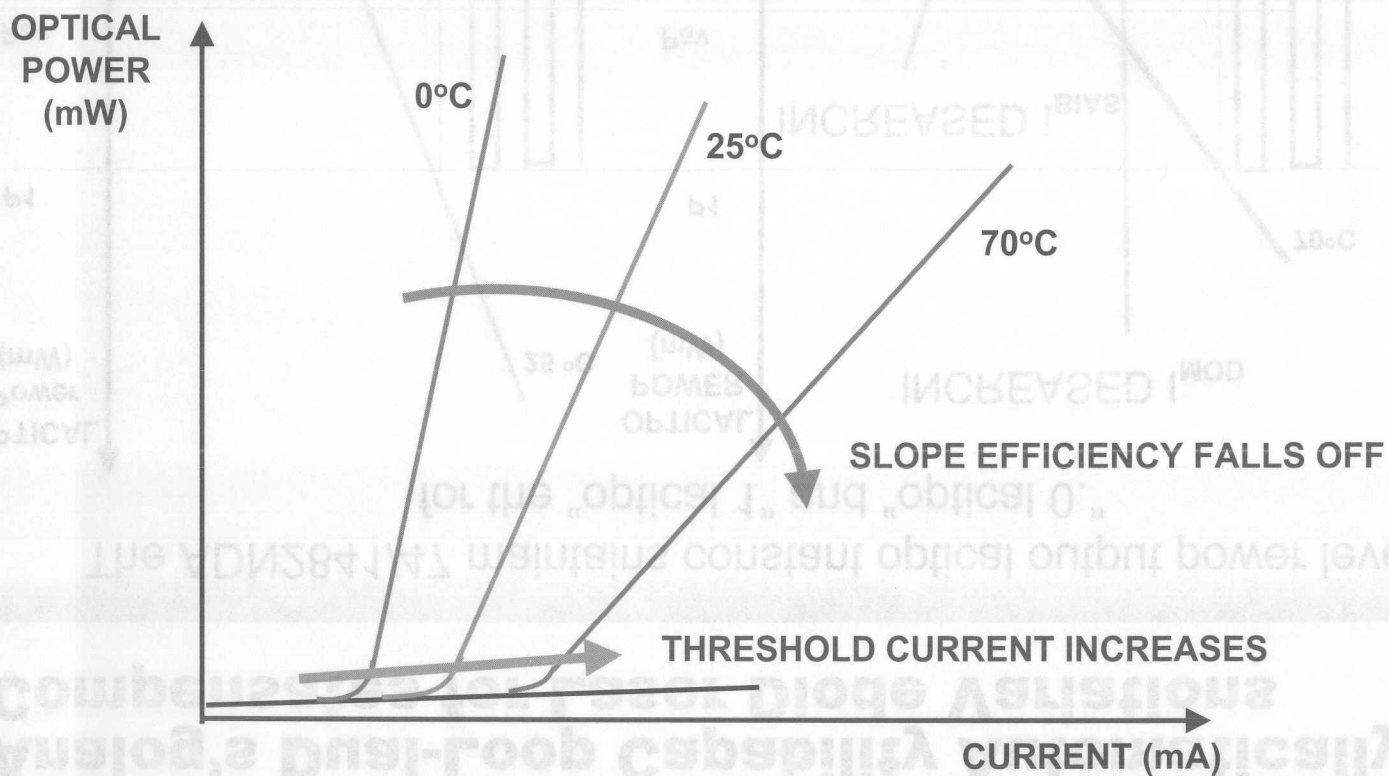
$$\text{Average Power} = \frac{P_1 + P_0}{2}$$

$$\text{Extinction Ratio} = \frac{P_1}{P_0}$$



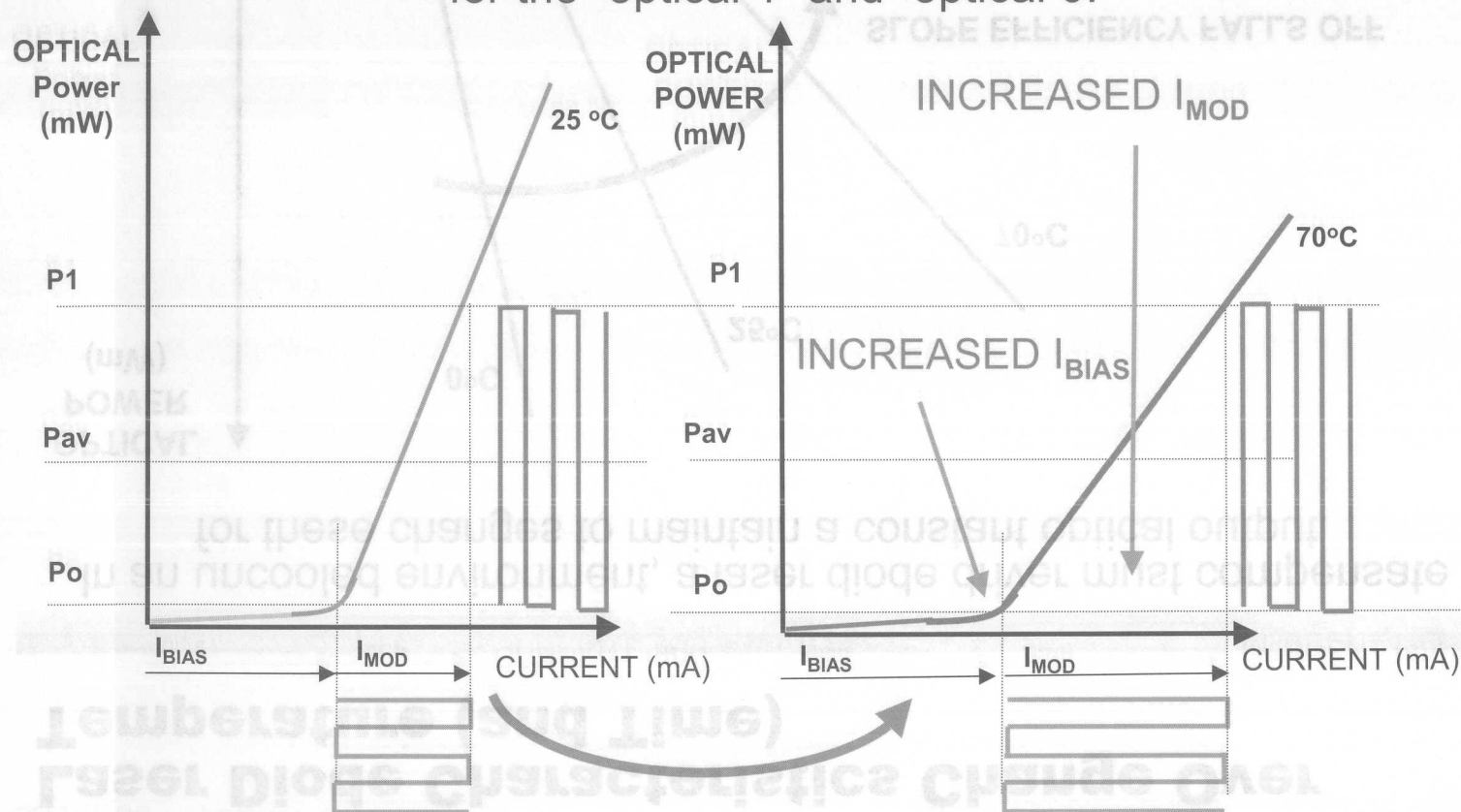
Laser Diode Characteristics Change Over Temperature (and Time)

In an uncooled environment, a laser diode driver must compensate for these changes to maintain a constant optical output.



Analog's Dual-Loop Capability Automatically Compensates for Laser Diode Variations

The ADN2841/47 maintains constant optical output power levels for the "optical 1" and "optical 0."



Extinction Ratio and Average Optical Power Continuously Maintained Over a Wide Temperature Range

- ADN2841 Optical Performance

Temperature (°C)	Extinction Ratio (dB)	Average Optical Power (dBm)
-10	9.86	-3.59
0	9.84	-3.44
25	9.64	-3.06
40	9.55	-3.03
70	10.16	-3.35

Extinction Ratio Range = 0.61 dB

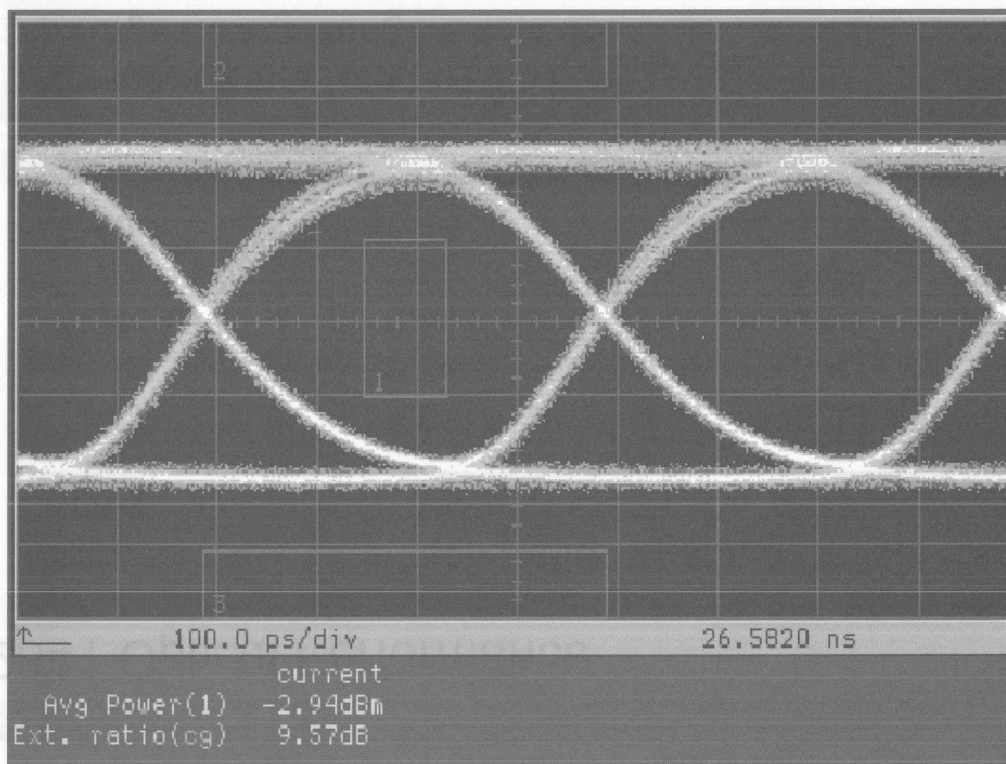
Average Power Range = 0.56 dB

Notes

Laser used = Mitsubishi FU-445, (typical tracking error = 0.5 dB).

Measurement taken from ADN2841 Optical Demo Board Rev C.

ADN2841 Optical Eye Diagram — 5 V Operation



2.5 Gbps filtered optical eye at 25°C, Mitsubishi FU-445 laser diode and ADN2841

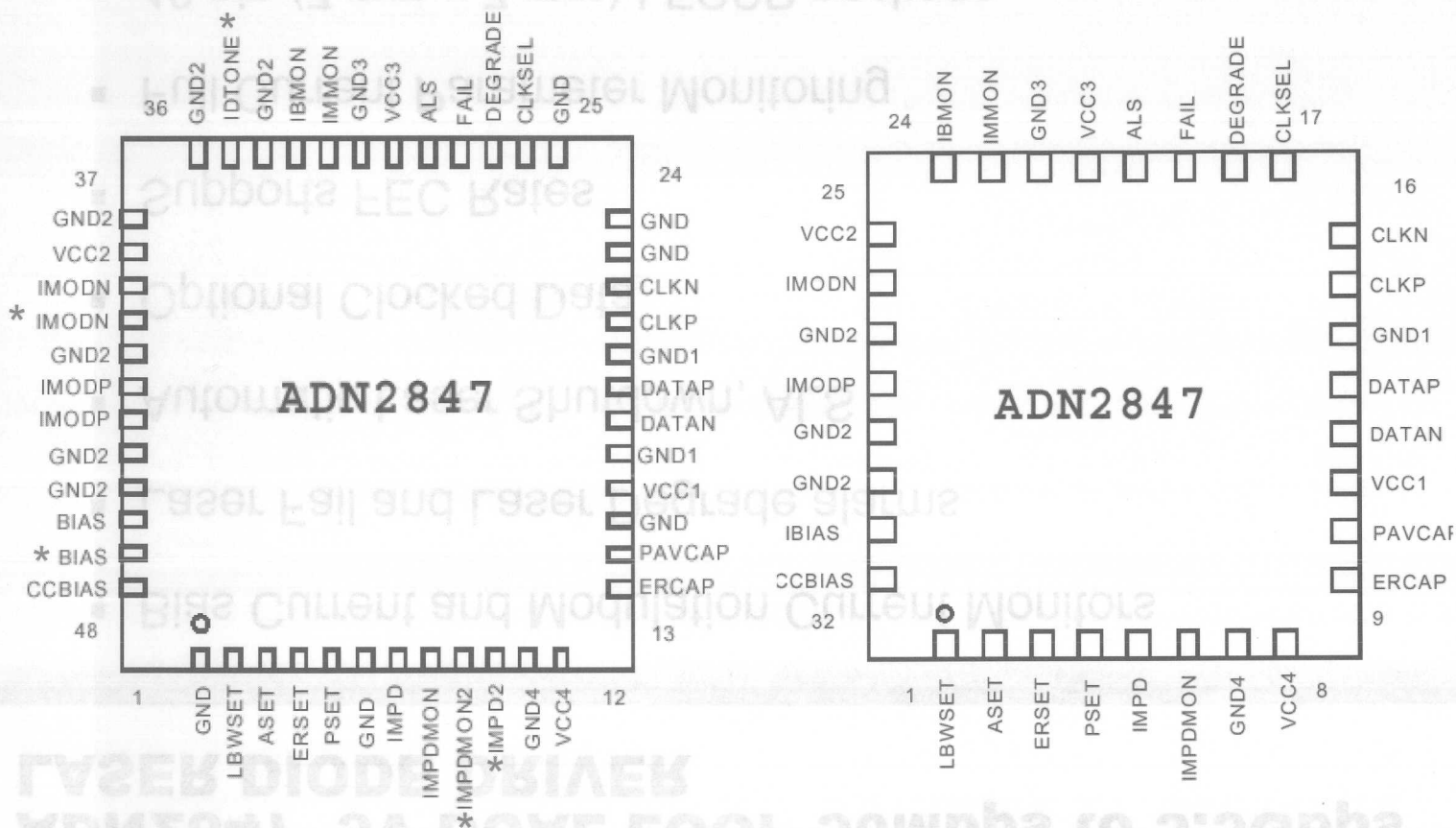
ADN2847 3V DUAL LOOP 50 Mbps to 3.3 Gbps LASER DIODE DRIVER

- Closed loop control of Power and Extinction Ratio
- 50 Mbps to 3.3 Gbps Operation
- Single 3.3 V operation
- Typical rise/fall time 80 ps
- Bias Current range 2 to 100 mA
- Modulation Current range 5 to 80 mA
- Monitor Photo Diode current 50 to 1100 μ A
- Dual MPD functionality for DWDM
- 55 mA Supply Current at +3.3 V

ADN2847 3V DUAL LOOP 50Mbps to 3.3Gbps LASER DIODE DRIVER

- Bias Current and Modulation Current Monitors
- Laser Fail and Laser Degrade alarms
- Automatic Laser Shutdown, ALS
- Optional Clocked Data
- Supports FEC Rates
- Full Current Parameter Monitoring
- 48 pin (7 mm x 7 mm) LFCSP package
- 32 pin (5 mm x 5 mm) LFCSP package
 - (reduced functionality)

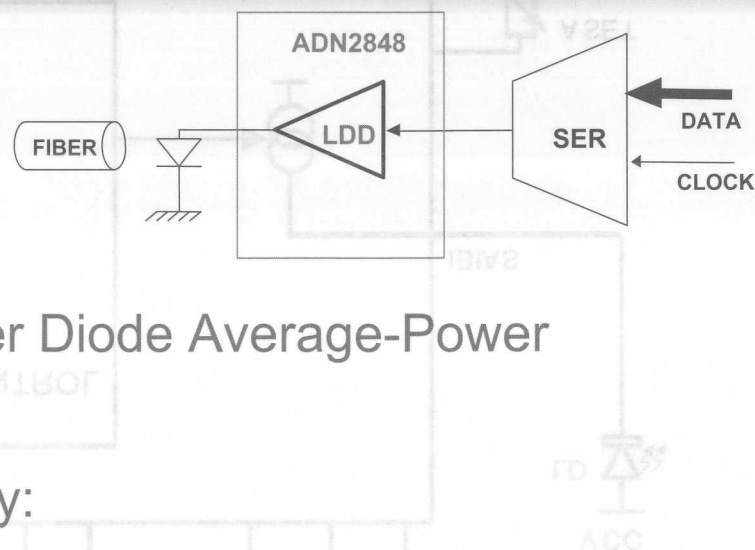
ADN2847 3V DUAL LOOP 50Mbps to 3.3Gbps LASER DIODE DRIVER



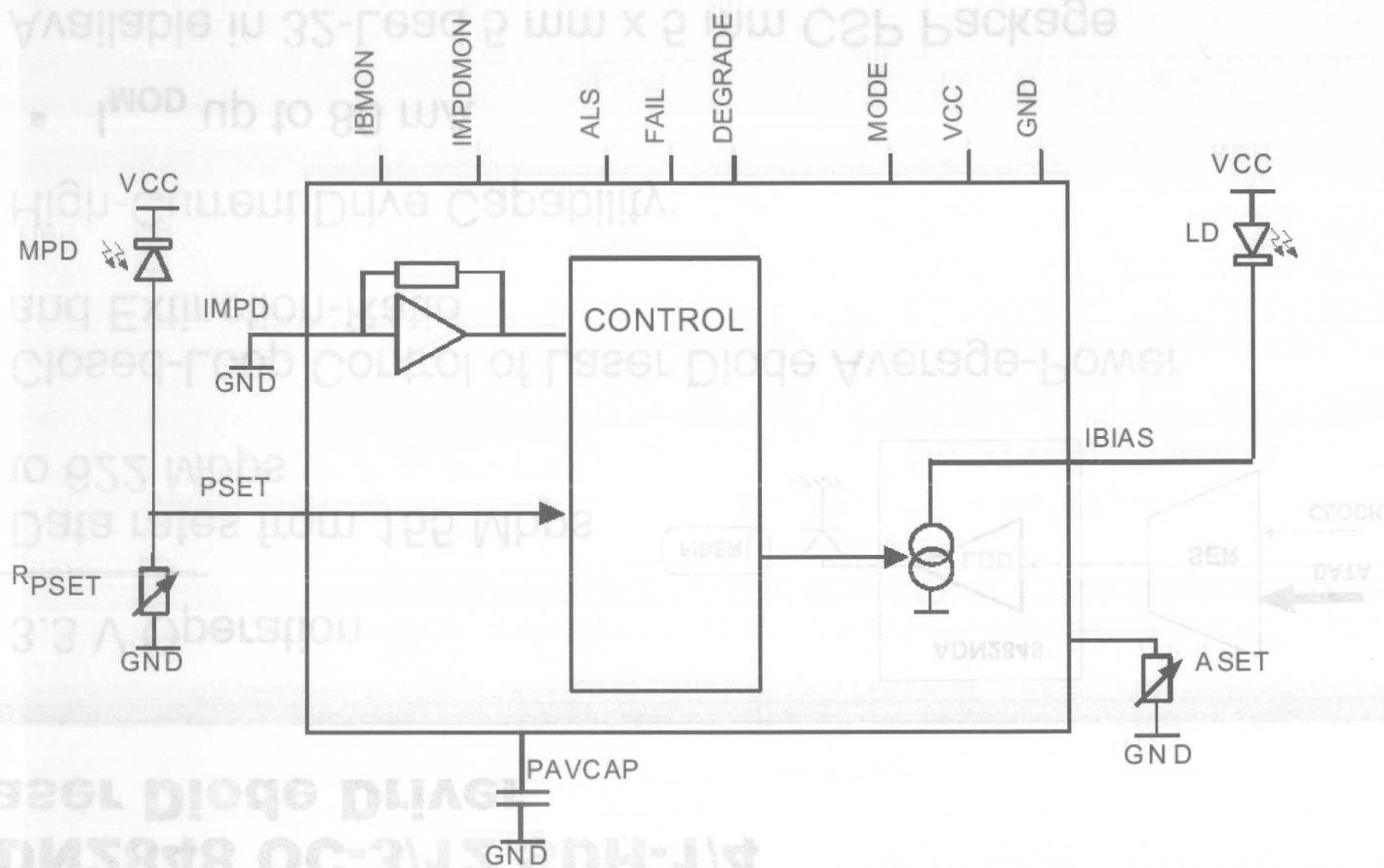
* NOT ON LOW PIN COUNT PACKAGE

ADN2848 OC-3/12 SDH-1/4 Laser Diode Driver

- 3.3 V Operation
- Data rates from 155 Mbps to 622 Mbps
- Closed-Loop Control of Laser Diode Average-Power and Extinction-Ratio
- High-Current Drive Capability:
 - I_{MOD} up to 80 mA
- Available in 32-Lead 5 mm x 5 mm CSP Package



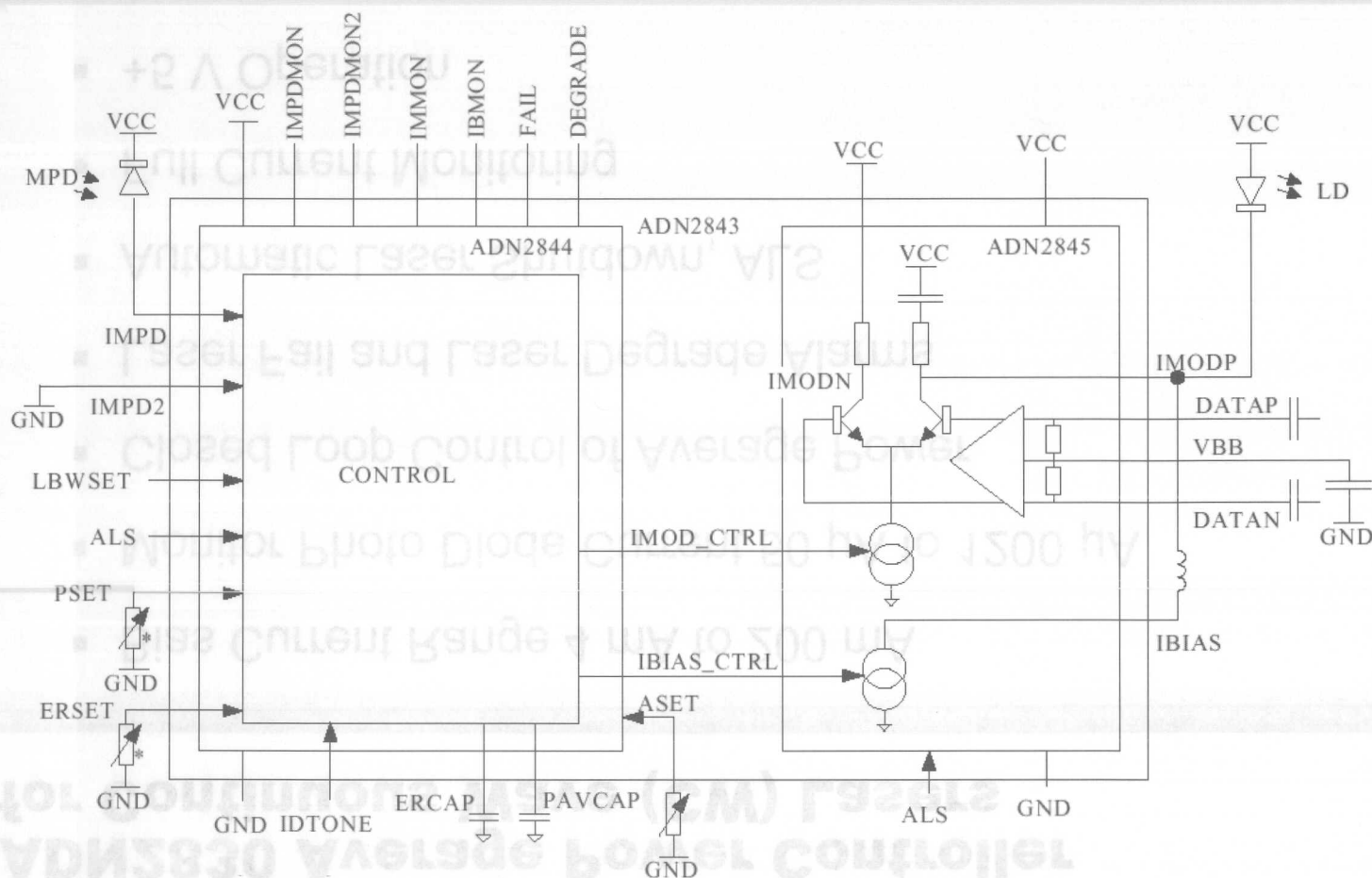
ADN2830 Average Power Controller for Continuous Wave (CW) Lasers



ADN2830 Average Power Controller for Continuous Wave (CW) Lasers

- Bias Current Range 4 mA to 200 mA
- Monitor Photo Diode Current 50 μ A to 1200 μ A
- Closed Loop Control of Average Power
- Laser Fail and Laser Degrade Alarms
- Automatic Laser Shutdown, ALS
- Full Current Monitoring
- +5 V Operation
- -40° C to 85° C Temperature Operation
- 5 mm x 5 mm 32 pin LFCSP Package

ADN2843 10.709 Gb/s Laser Diode Driver Chipset



ADN2843 10.709 Gb/s Laser Diode Driver Chipset

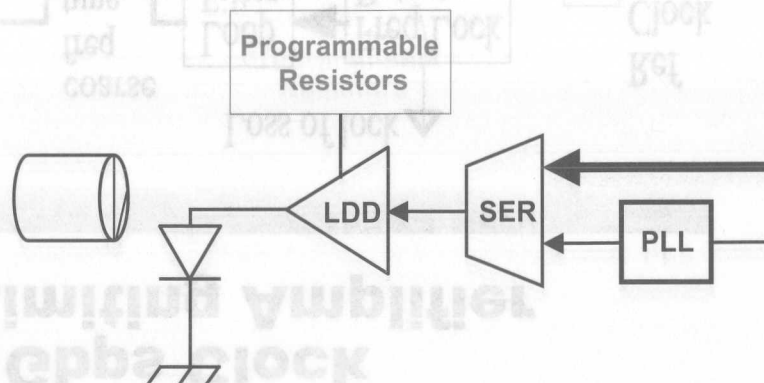
- Data Rates from 50 Mb/s to 10.709 Gb/s
- Typical Rise/ Fall Time 30 ps
- Bias Current Range 3 mA to 80 mA
- Modulation Current Range 5 mA to 80 mA
- Monitor Photo Diode Range 50 mA to 1100 mA
- Closed Loop Control of both Average Optical Power and Extinction Ratio
- Programmable Loop BW for Both Loops
- Laser Fail and Laser Degrade Alarms
- Automatic Laser Shutdown, ALS

ADN2843 10.709 Gb/s Laser Diode Driver Chipset

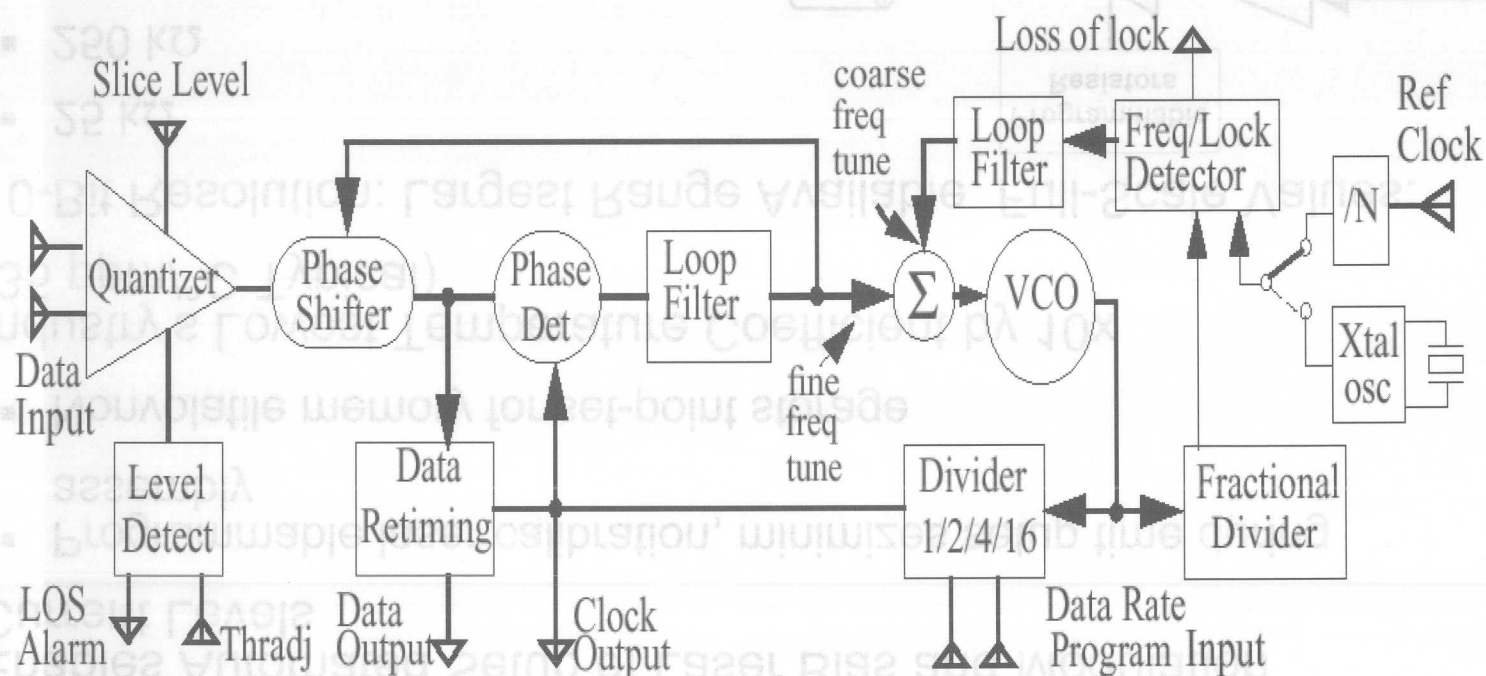
- Dual MPD functionality for wavelength control
- CML data inputs
- 50 Ω internal data terminations
- +3.3 V single supply operation
- Driver supplied in dice format.
 - ADN2844 Also Available in Packaged Form (5 mm x 5mm LFCSP)

ADN2850 Dual Programmable Resistors

- Enables Automated Setup of Laser Bias and Modulation Current Levels
 - Programmable laser calibration, minimizes setup time during assembly
 - Nonvolatile memory for set-point storage
- Industry's Lowest Temperature Coefficient by 10x (35 ppm/°C Typical)
- 10-Bit Resolution: Largest Range Available. Full-Scale Values:
 - 25 kΩ
 - 250 kΩ
- Available in Two Package Types:
 - LFCSP: 5 mm x 5 mm, 16-Lead
 - TSSOP: 5 mm x 6.5 mm, 16-Lead



ADN2819 Multirate to 2.7 Gbps Clock and Data Recovery with Limiting Amplifier



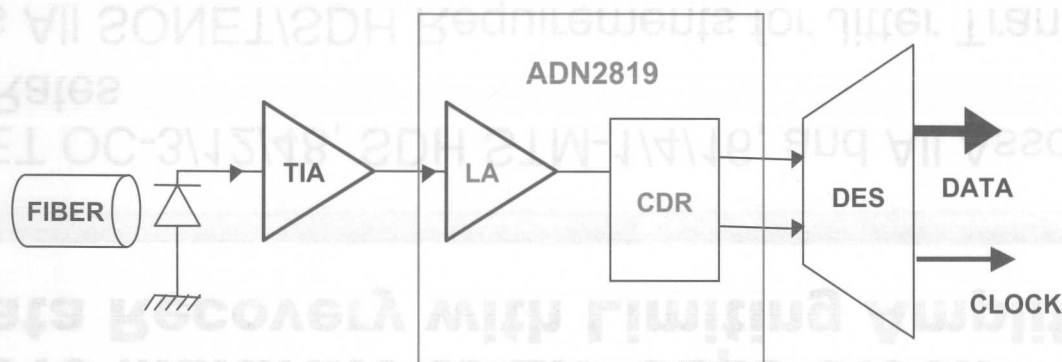
- Single Reference Clock Frequency for All Rates
- Internal MUX to Bypass CDR

ADN2819 Multirate to 2.7 Gbps Clock and Data Recovery with Limiting Amplifier

- SONET OC-3/12/48, SDH STM-1/4/16, and All Associated FEC Rates
- Meets All SONET/SDH Requirements for Jitter Transfer, Generation, and Tolerance
- Integrated Limiting Amplifier with User-Programmable Threshold (Slice) Adjust
 - Limiting amplifier sensitivity: 4 mV typical
 - Adjustable slice level: ± 100 mV
- One Supply $+3.3\text{ V} \pm 10\%$
- Low Power: 540 mW Typical
- Small Footprint: 48-Lead LFCSP Package (7 x 7 mm Overall)

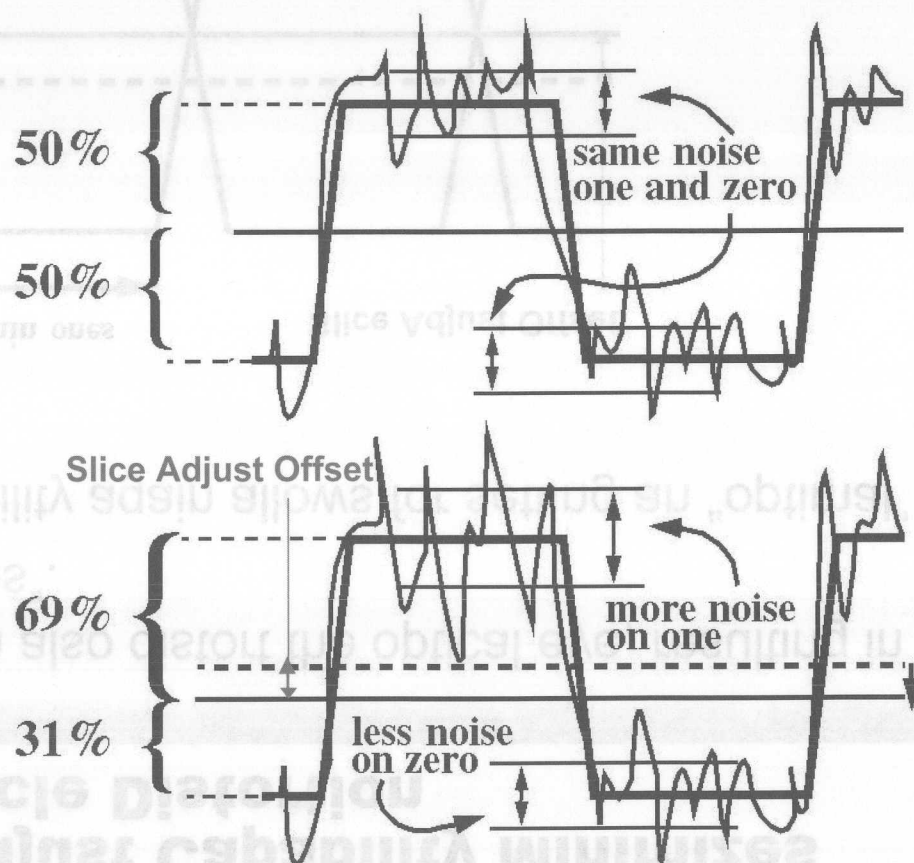
ADN2819 Multirate to 2.7 Gbps Clock and Data Recovery with Limiting Amplifier

- Loss of Lock Indicator
- Loop-back Mode for High-Speed Test Data
- Squelch and Bypass Features
- Single-Supply Operation: 3.3 V
- Patented Clock Recovery Architecture



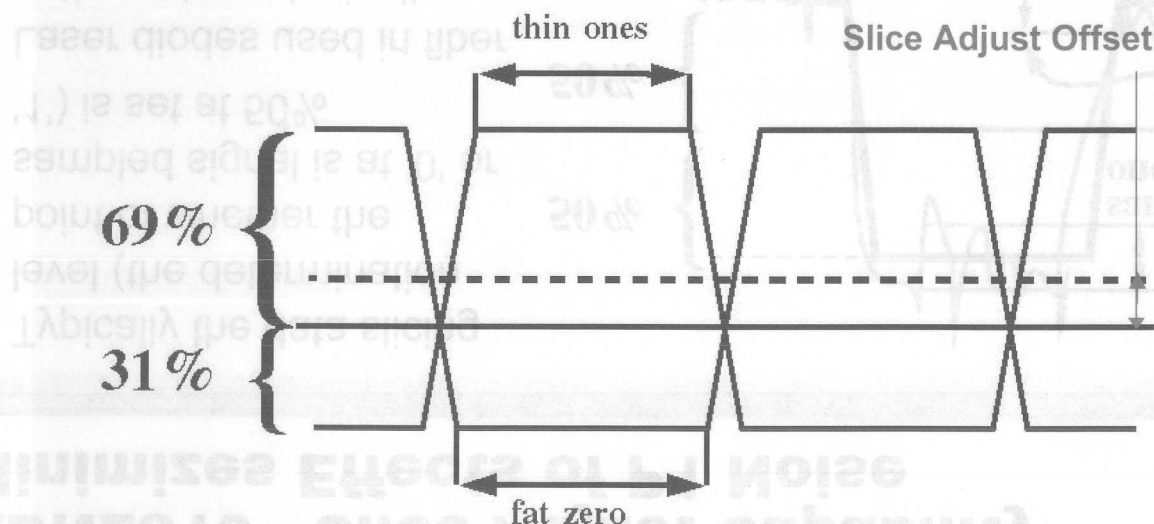
ADN2819 Slice Adjust Capability Minimizes Effects of P1 Noise

- Typically the data slicing level (the determination point of whether the sampled signal is at '0' or '1') is set at 50%
- Laser diodes used in fiber optic systems typically induce more noise on the optical '1' signal level than on the '0'
- In such systems the "optimal" slice level is below 50% in order to avoid false detects generated by excessive noise

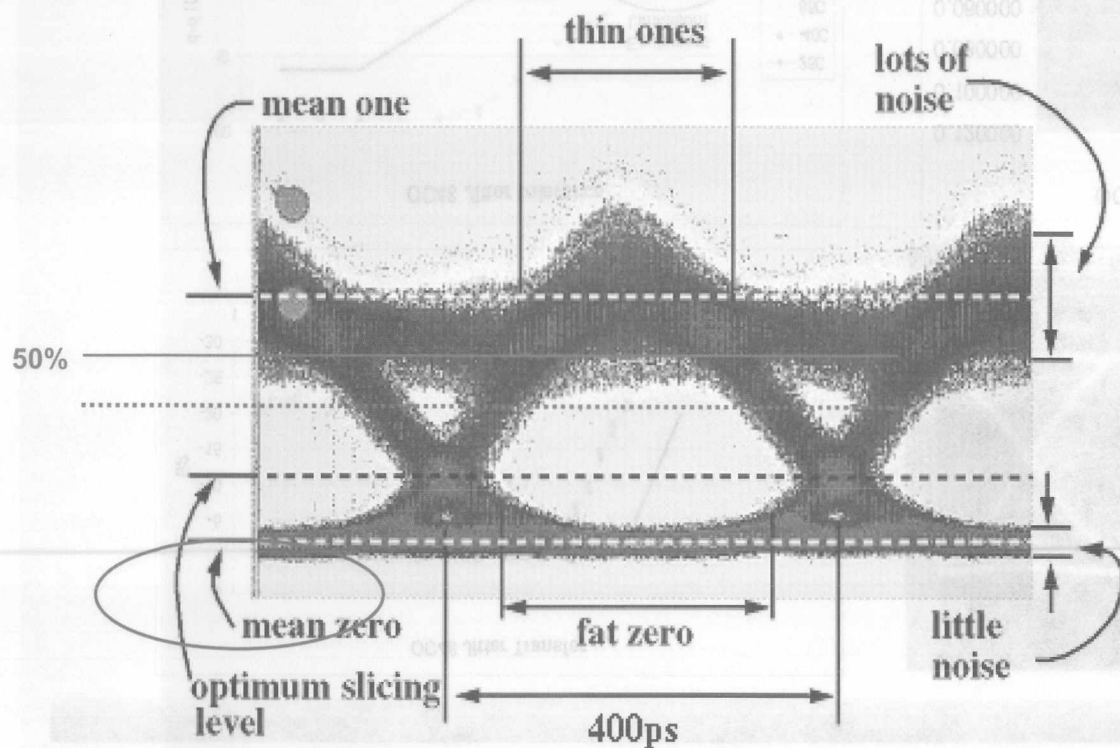


ADN2819 Slice Adjust Capability Minimizes Effects of Duty Cycle Distortion

- Optical transmission can also distort the optical eye, resulting in “fat zero’s” and “thin ones”.
- Again slice adjust capability again allows for setting an “optimal” slice level

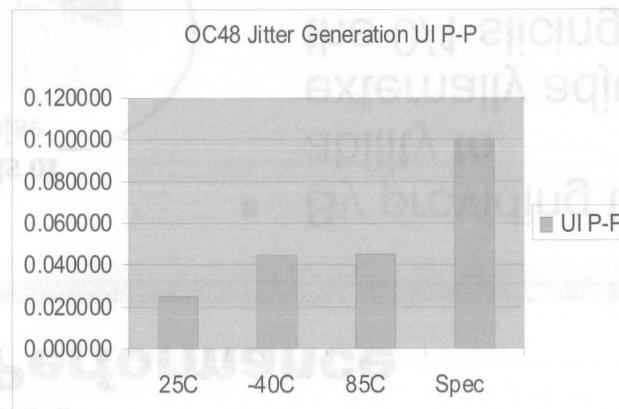
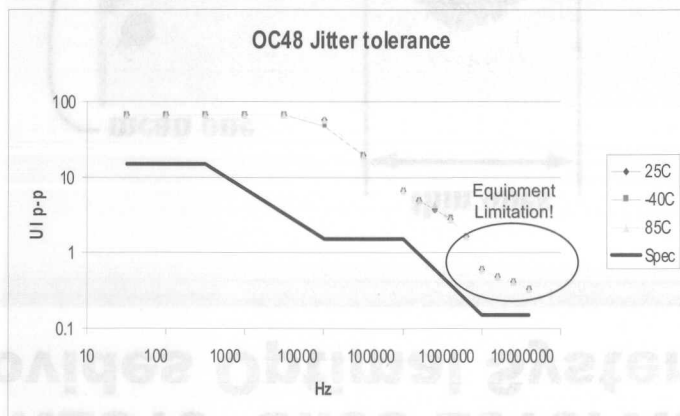
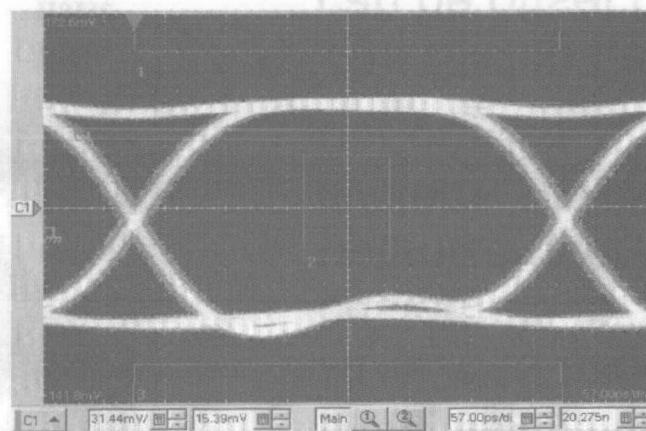
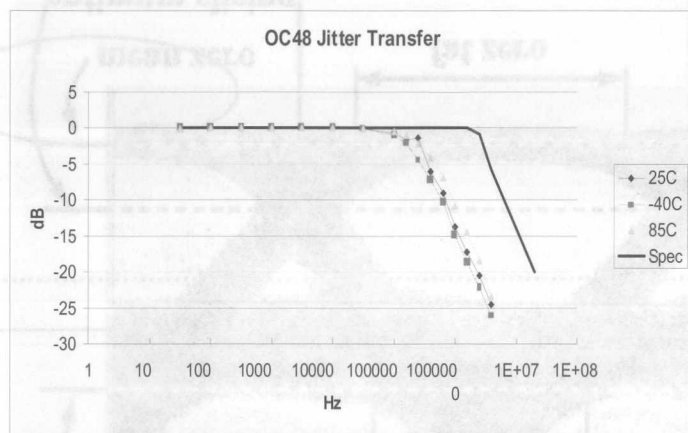


ADN2819 Slice Level Adjust Provides Optimal System Performance

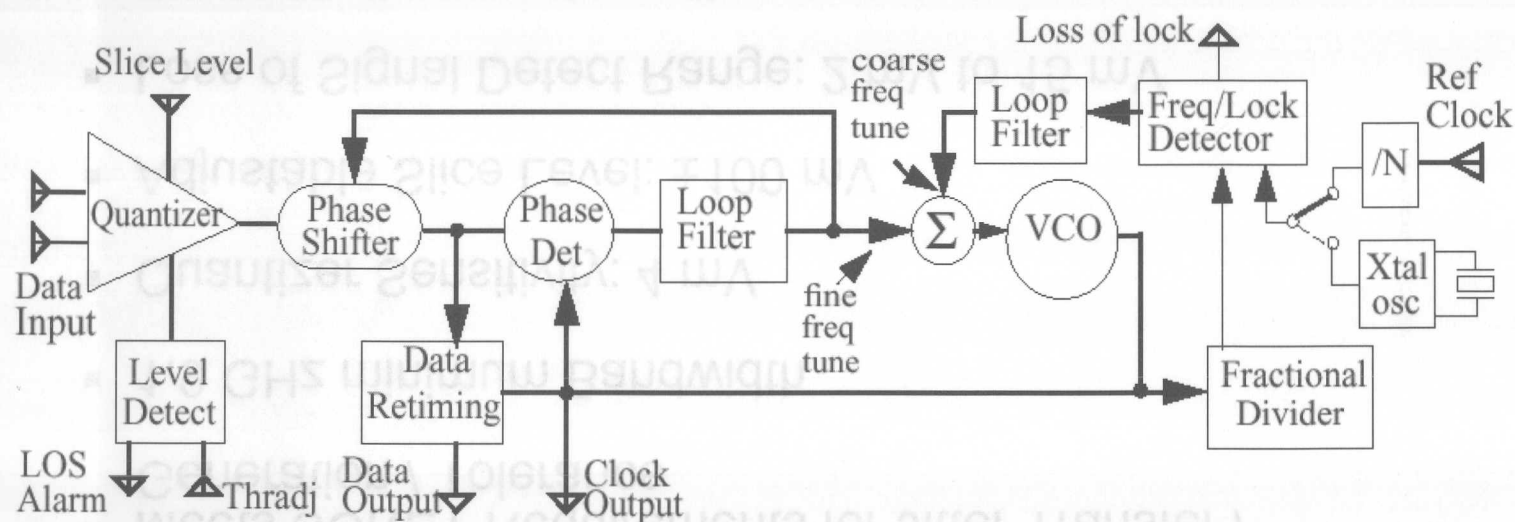


- By providing the ability to externally adjust the 0/1 slicing level, the ADN2819 allows customers to optimize overall system performance
- The Slicing Level can be offset by $\pm 100\text{mV}$ for enhanced flexibility

ADN2819 Measured Performance



ADN2811 OC-48 (FEC) CDR for WDM Transponders



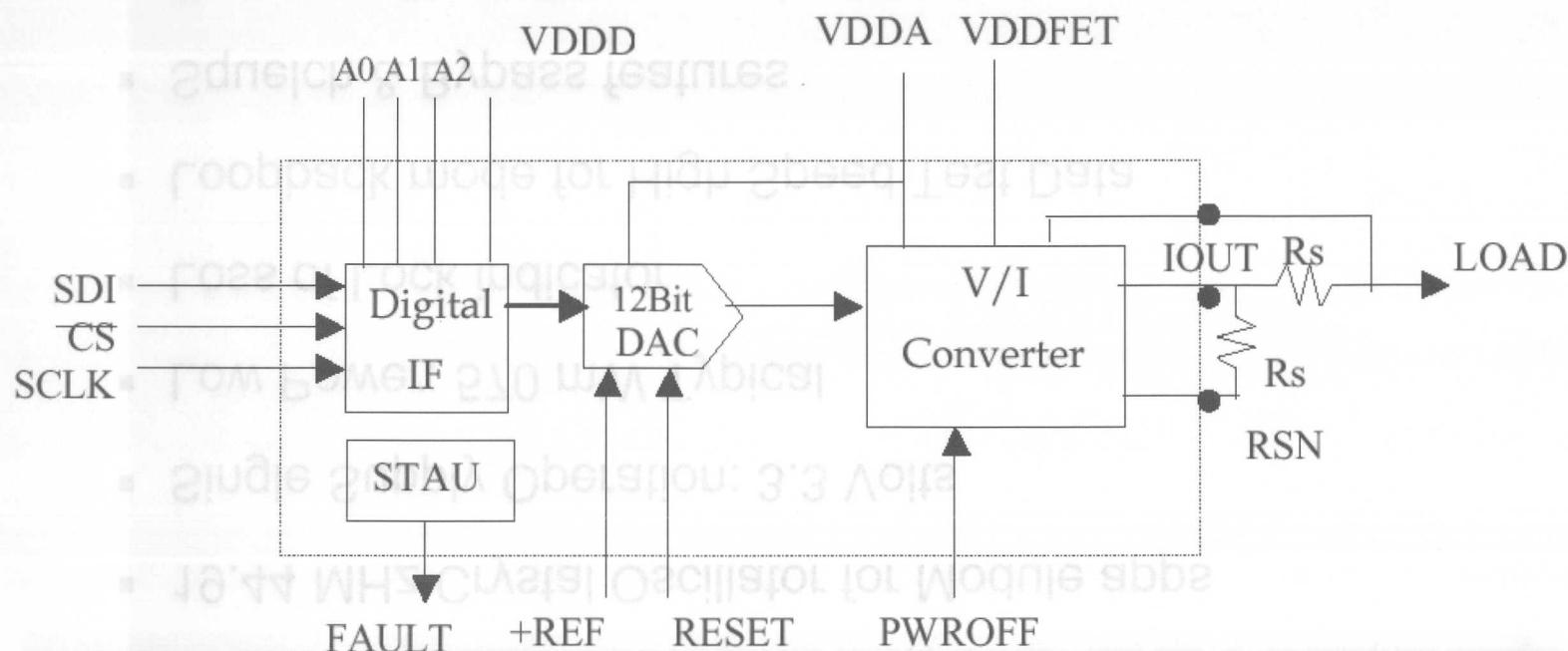
ADN2811 OC-48 (FEC) CDR for WDM Transponders

- Meets SONET Requirements for Jitter Transfer / Generation / Tolerance
- 1.9 GHz minimum Bandwidth
- Quantizer Sensitivity: 4 mV
- Adjustable Slice Level: ± 100 mV
- Loss of Signal Detect Range: 2 mV to 15 mV
- Single Reference Clock Frequency for both rates Including 15/14 (7 %) Wrapper Rate
 - Choice of 19.44, 38.88, 77.76 or 155.52 MHz
- LVPECL / LVDS / LVCMOS compatible inputs

ADN2811 OC-48 (FEC) CDR for WDM Transponders

- 19.44 MHz Crystal Oscillator for Module apps
- Single Supply Operation: 3.3 Volts
- Low Power: 570 mW Typical
- Loss of Lock indicator
- Loopback mode for High Speed Test Data
- Squelch & Bypass features
- Patented Clock Recovery Architecture
- 7 x 7 mm 48 pin LFCSP Package

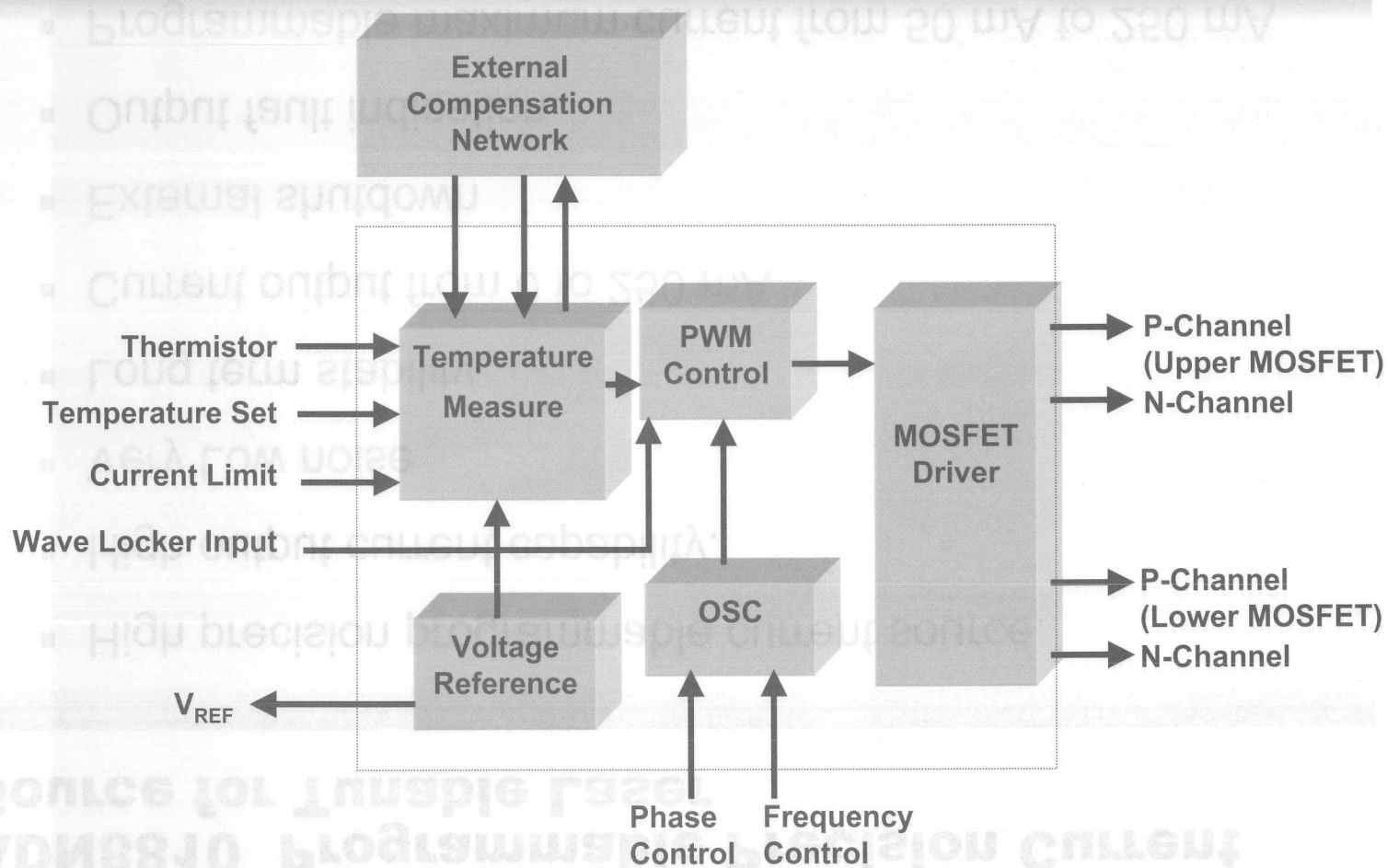
ADN8810 Programmable Precision Current Source for Tunable Laser



ADN8810 Programmable Precision Current Source for Tunable Laser

- High precision programmable current source.
- High output current capability.
- Very Low noise
- Long term stability
- Current output from 0 to 250 mA
- External shutdown
- Output fault indication
- Programmable maximum current from 50 mA to 250 mA
- Lead Frame Chip Scale Package (LFCSP) (4 mm x 4 mm)

ADN8830 Thermoelectric Cooler Controller

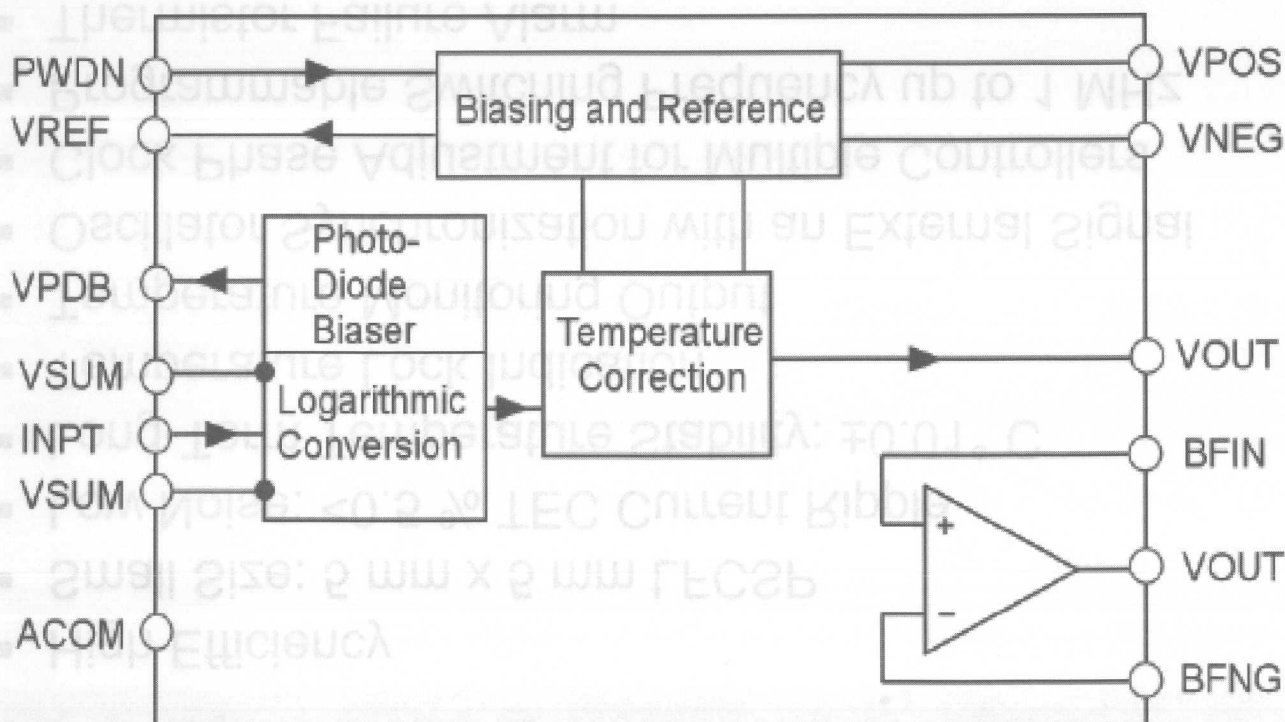


ADN8830 Thermoelectric Cooler Controller

- High Efficiency
- Small Size: 5 mm x 5 mm LFCSP
- Low Noise: <0.5 % TEC Current Ripple
- Long-Term Temperature Stability: $\pm 0.01^{\circ}\text{C}$
- Temperature Lock Indication
- Temperature Monitoring Output
- Oscillator Synchronization with an External Signal
- Clock Phase Adjustment for Multiple Controllers
- Programmable Switching Frequency up to 1 MHz
- Thermistor Failure Alarm
- Maximum TEC Voltage Programmability



AD8304 160 dB Range Logarithmic Converter

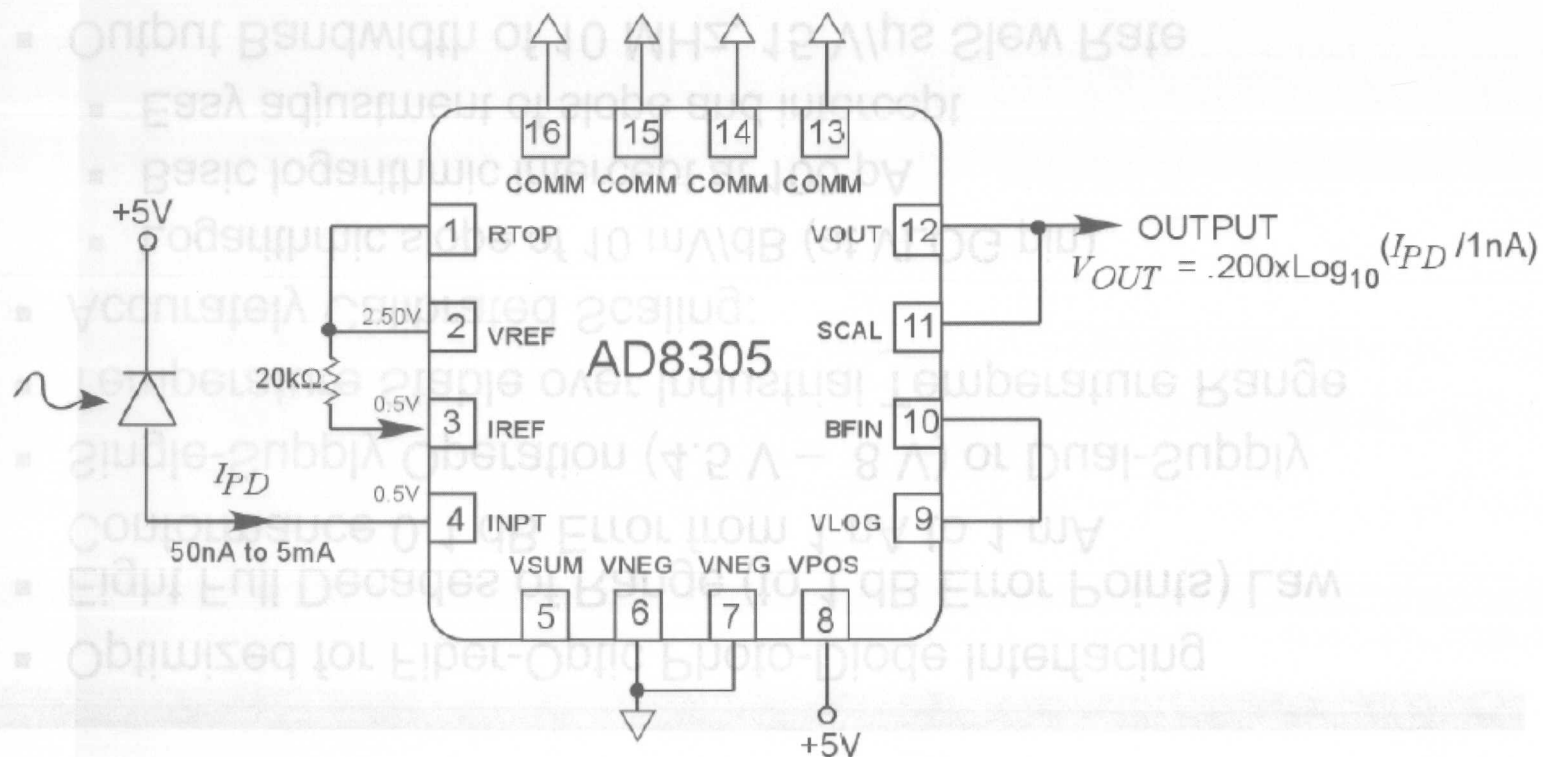


Optimized for photo-diode interfacing

AD8304 160 dB Range Logarithmic Converter

- Optimized for Fiber-Optic Photo-Diode Interfacing
- Eight Full Decades of Range (to 1 dB Error Points) Law Conformance 0.1 dB Error from 1 nA to 1 mA
- Single-Supply Operation (4.5 V – 8 V) or Dual-Supply
- Temperature Stable over Industrial Temperature Range
- Accurately Calibrated Scaling:
 - Logarithmic slope of 10 mV/dB (at VLOG pin)
 - Basic logarithmic intercept at 100 pA
 - Easy adjustment of slope and intercept
- Output Bandwidth of 10 MHz, 15 V/μs Slew Rate
- 1-, 2-, or 3-Pole Low Pass Filtering at Output
- Miniature 14-Lead Package (TSSOP)
- Low Power: ~3 mA Quiescent Current (Enabled)

AD8305 100dB-range (50nA-5mA) Logarithmic Converter



AD8305 100dB-range (50nA-5mA) Logarithmic Converter

- Optimized for Fiber-Optic Photodiode Interfacing Over Five Decades of Range
- Law Conformance 0.3 dB from 50 nA to 5 mA
- Single Supply Operation (2.7 V – 5.5 V)
- Complete and Temperature Stable
- Nominal slope of 10 mV/dB (200 mV/decade)
- Nominal Intercept of 1 nA set by external resistor
- Optional Adjustment of Slope and Intercept
- Minimal Response Time at all Current Levels
- Miniature 16 pin Chip Scale Package (LFCSP 3 x 3 mm)
- Low Power: ~4 mA Quiescent Current

(Am2-An02) agnab-Bb00r 208DA 18302 logarithmic Converter

revO gnicsatretal ebolboto19 citqO-1ed19 tot bezim19Q
 Five Decades of Range

- Am 2 of An 02 mont Bb 3.0 econsmofnoC law
- (V 2.2 – V T.S) noitaragO y1qu2 elgn12
- eld122 erut1reqmet bna etelqmcO
- (ebacabV/m 002) BbV/m 01 to eq12 la1n1m01
- tot121er la1n0t2x2 yd 122 An 1 to 1q20t2r1n1 la1n1m01
- 1q20t2r1n1 bna eq12 to 1n2mt2ulpA la1n0t1qO
- el212 1n2mt2U 1la 122 em1T 22n0q2221 la1n1m1m
- (1m1 2 x 2 120 12) 22gn022 1 21222 q1n0 1nq 01 212121m1m
- 1n2mt2U 1n22221uO Am 4 – 12w029 w02

SECTION 11

Digital Signal Processors

**16-Bit
32-Bit
Tools
Solutions**

16-Bit Processors

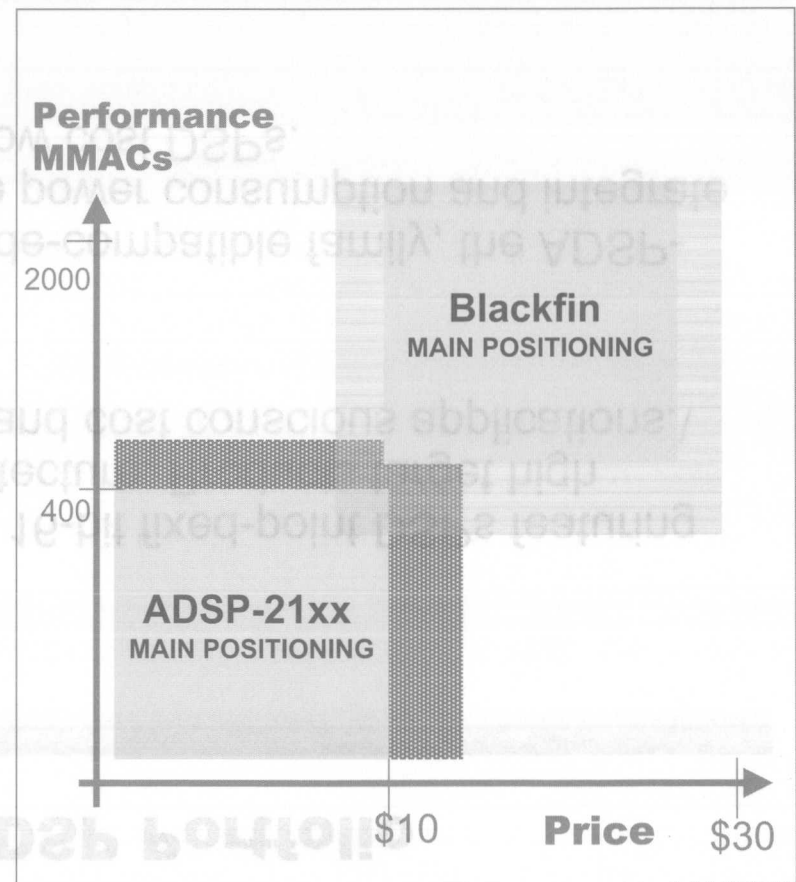
ADSP-21xx DSP Family
Blackfin™ DSP Family

16-Bit General-Purpose DSP Portfolio

- Blackfin™ DSP
 - High performance, dual-MAC, 16-bit fixed-point DSPs featuring the ADI/Intel microsignal architecture. Products target high performance, power efficient, and cost conscious applications.
- ADSP-21xx DSP
 - Continuing the ADSP-21xx code-compatible family, the ADSP-218xn and ADSP-219x reduce power consumption and integrate system-level peripherals into low cost DSPs.

16-Bit General-Purpose DSP Portfolio

- Blackfin DSPs Focus on
Moderate to High Performance,
Low Power Applications
 - Consumer Video, Audio
 - Internet, Networking Appliances
 - Automotive Telematics
- ADSP-21xx DSPs Focus on
Lower Cost, Moderate
Performance Applications
 - Wired/Wireless Voice
 - VoIP/VoN
 - Industrial Control
 - Automotive Control



Blackfin DSP Core Values

Wireless Connectivity

- Bluetooth
- GSM
- Third Generation

Wired Connectivity

- USB
- TCP/IP
- VoIP

■ RTOS

- Operating Systems
- Applications Software

Digital
Signal
Processing

BLACKfin™
DSP

Micro-
Processing

Image
Processing

Human Interface

- Speech Recognition
- Handwriting
- Audio

Image and Video

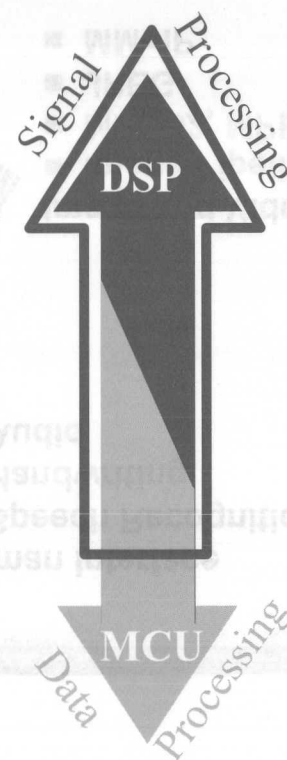
- Image Pipeline
- MPEG2, MPEG4, WMT
- JPEG
- MMoIP

■ Low Power

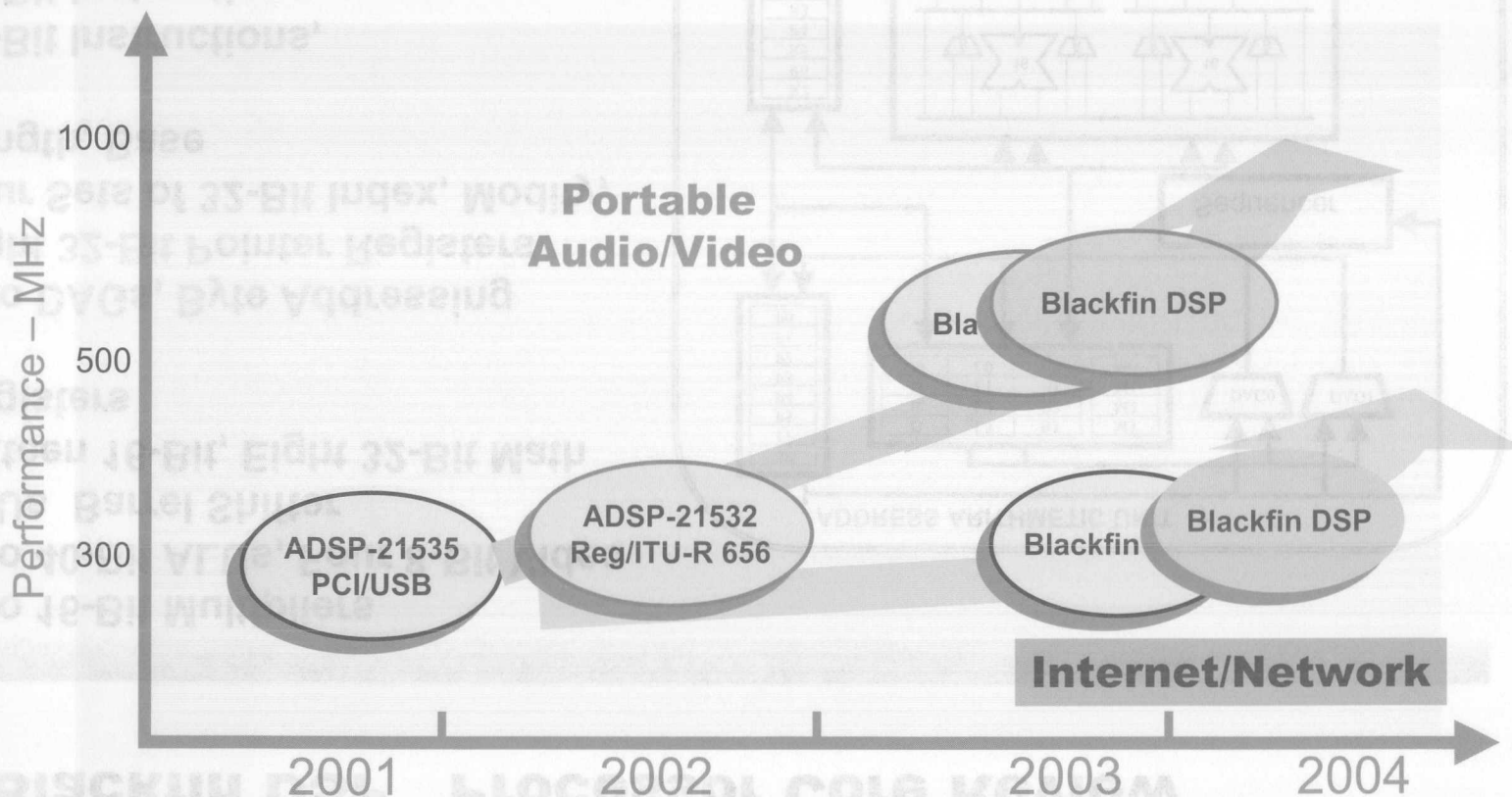
- Dynamic Power Management

Blackfin DSP Architectural Benefits

- Simplifying Real-Time Hardware and Software Design
 - High Performance Architecture with support for Video Processing
 - Single Processor supports DSP and Control Functions
 - Dynamic Power Management through Optimized Companion Products and integration



Blackfin DSP Roadmap to Performance and Integration



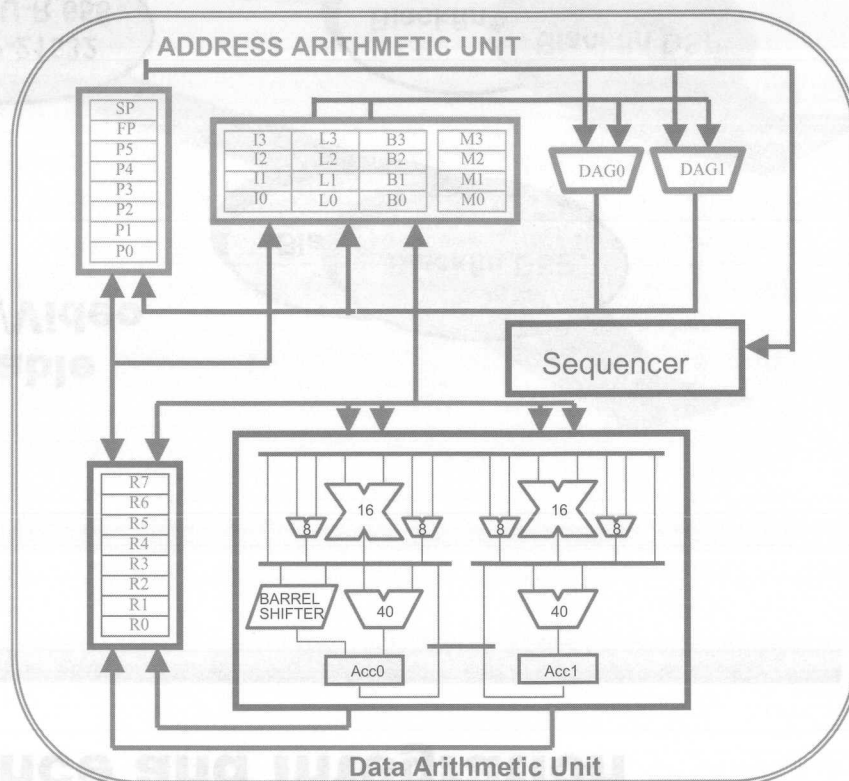
Blackfin DSP Processor Core Review

Two 16-Bit Multipliers
Two 40-Bit ALUs, Four 8-Bit Video
ALUs Barrel Shifter
Sixteen 16-Bit, Eight 32-Bit Math
Registers

Two DAGs, Byte Addressing
Eight 32-Bit Pointer Registers
Four Sets of 32-Bit Index, Modify,
Length, Base

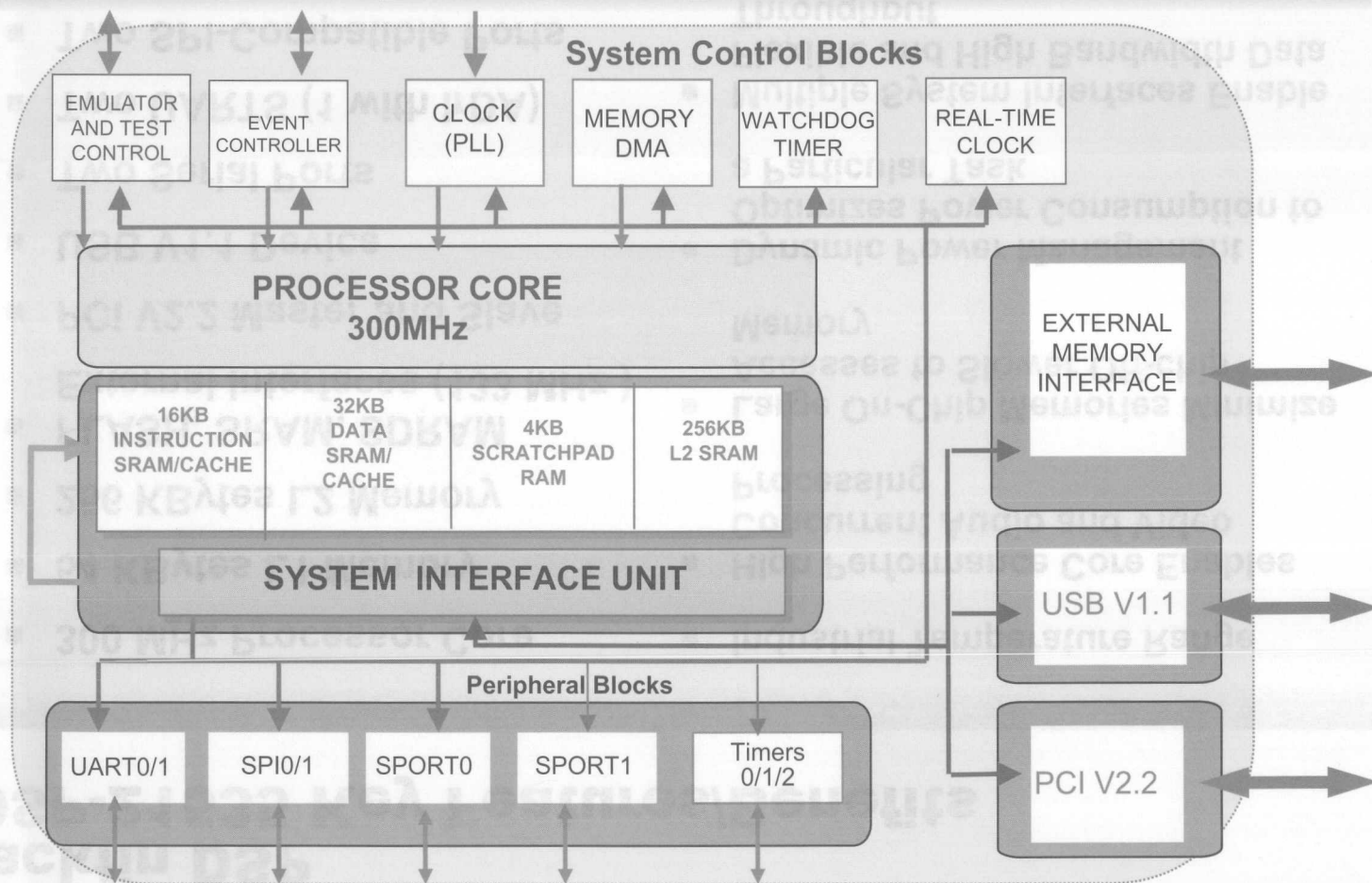
16-Bit Instructions,
32-Bit Instructions
Multi-Issue, 64-Bit Instructions

Interlocked Pipeline Micro Signal
Architecture, Developed with Intel



Blackfin DSP

ADSP-21535: Architecture Overview



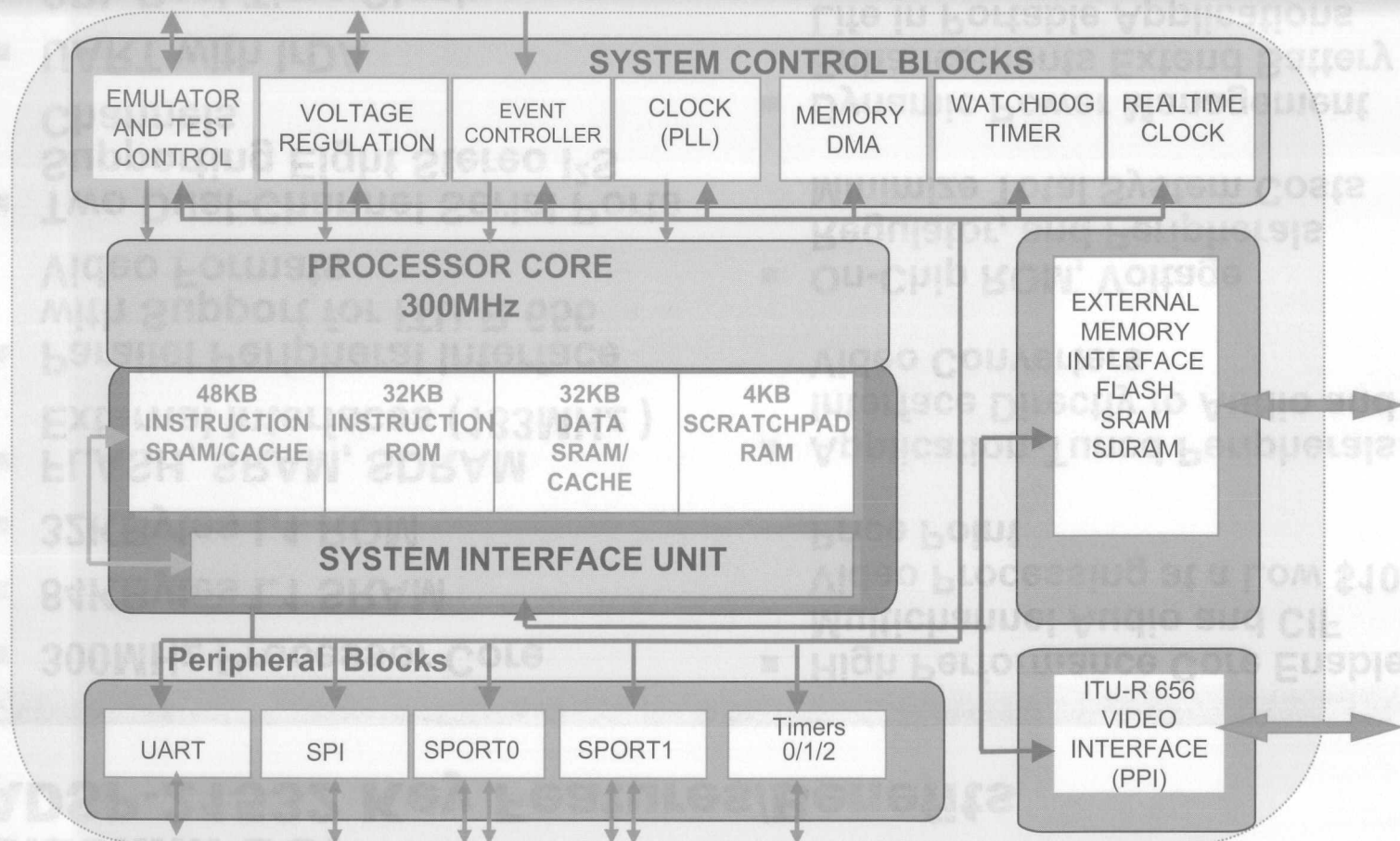
Blackfin DSP

ADSP-21535 Key Features/Benefits

- 300 MHz Processor Core
- 54 KBytes L1 Memory
- 256 KBytes L2 Memory
- FLASH, SRAM, SDRAM External Interfaces (133 MHz)
- PCI V2.2 Master and Slave
- USB V1.1 Device
- Two Serial Ports
- Two UARTS (1 with IrDA)
- Two SPI-Compatible Ports
- Real-Time Clock
- Watchdog Timer
- Industrial Temperature Range
- High Performance Core Enables Concurrent Audio and Video Processing
- Large On-Chip Memories Minimize Accesses to Slower Off-chip Memory
- Dynamic Power Management Optimizes Power Consumption to a Particular Task
- Multiple System Interfaces Enable Flexible and High Bandwidth Data Throughput
- Highly Integrated Peripheral Set Minimizes System BOM Costs.

Blackfin DSP

ADSP-21532: Architecture Overview



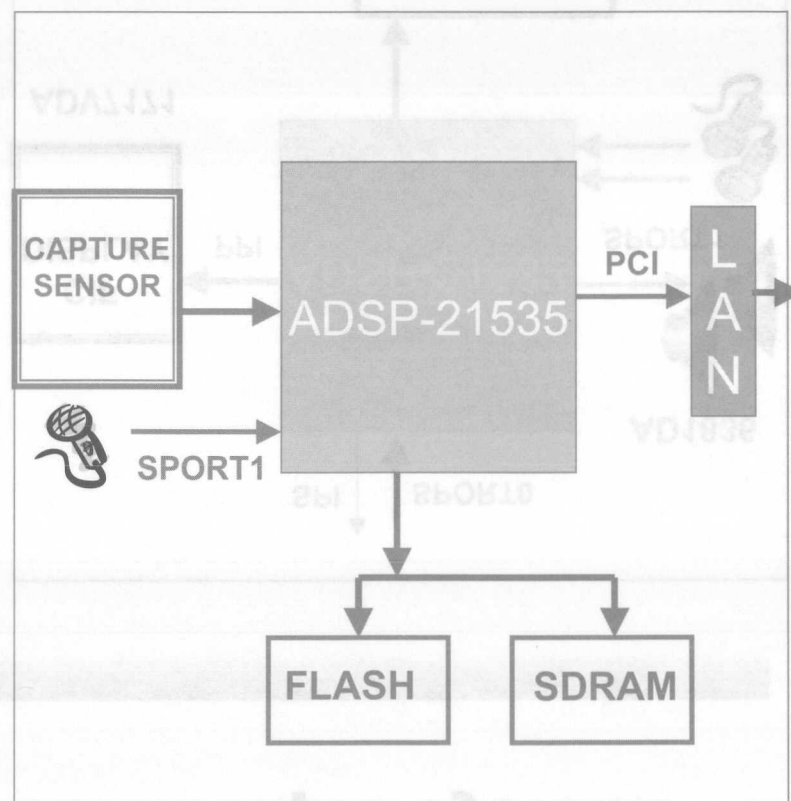
Blackfin DSP

ADSP-21532 Key Features/Benefits

- 300MHz Processor Core
- 84KBytes L1 SRAM
- 32KBytes L1 ROM
- FLASH, SRAM, SDRAM External Interfaces (133MHz)
- Parallel Peripheral Interface with Support for ITU-R 656 Video Formats
- Two Dual-Channel Serial Ports Supporting Eight Stereo I²S Channels
- UART with IrDA
- SPI, Real-Time Clock, Watchdog Timer
- On-chip Core Coltage Regulator
- High Performance Core Enables Multichannel Audio and CIF Video Processing at a Low \$10 Price Point
- Application-Tuned Peripherals Interface Directly to Audio and Video Converters
- On-Chip ROM, Voltage Regulator, and Peripherals Minimize Total System Costs
- Dynamic Power Management Enhancements Extend Battery Life in Portable Applications
- Industrial Temperature Range

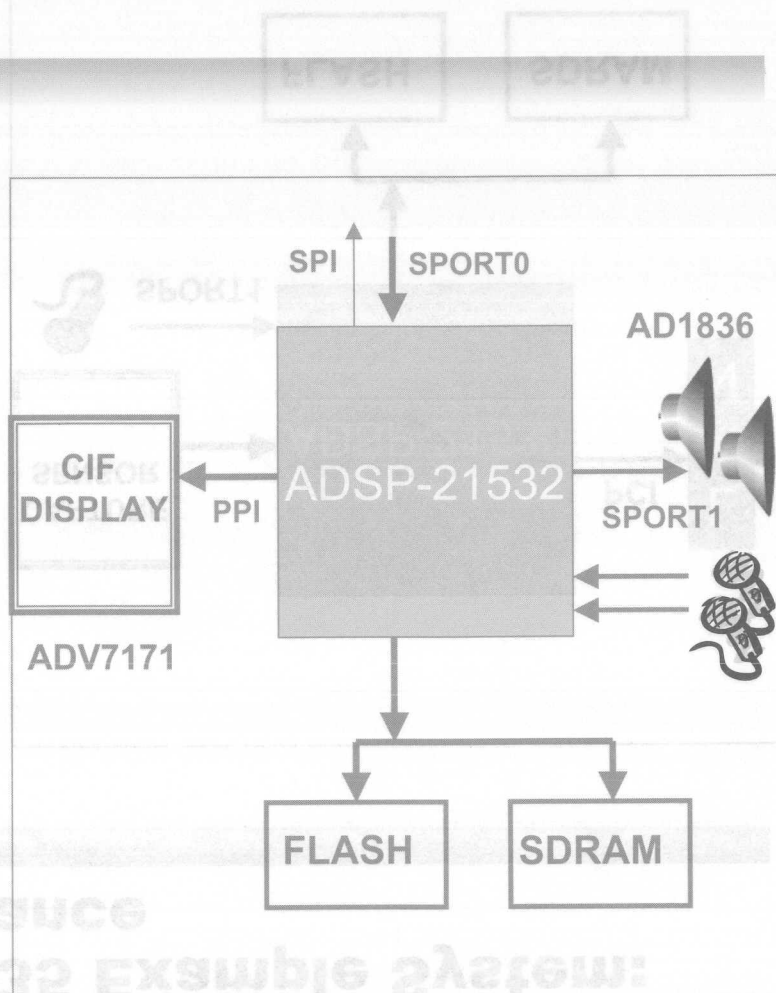
Blackfin DSP ADSP-21535 Example System: Low Cost Video Surveillance

- Single Chip Video Encoder for Surveillance Systems
 - Video capture – example Omnivision integrated lens/sensor
 - SPORT1 connects microphone
 - MPEG4 CIF video encoding
 - MPEG4 audio encoding optional
 - Video transport over Ethernet



Blackfin DSP ADSP-21532 Example System: Video Display system

- Single Chip Audio and Video Decoder for Entertainment System
 - Video transport over local bus, connected through SPORT0 and SPI control
 - SPORT1 connects to stereo speakers and microphones
 - MPEG2 Video Decoding
 - MPEG2 Audio Decoding
 - Speech Recognition command and control with noise canceling array microphone input
 - Reduced existing BOM by 50%



Blackfin DSP Competitive Comparison: Low Cost Products

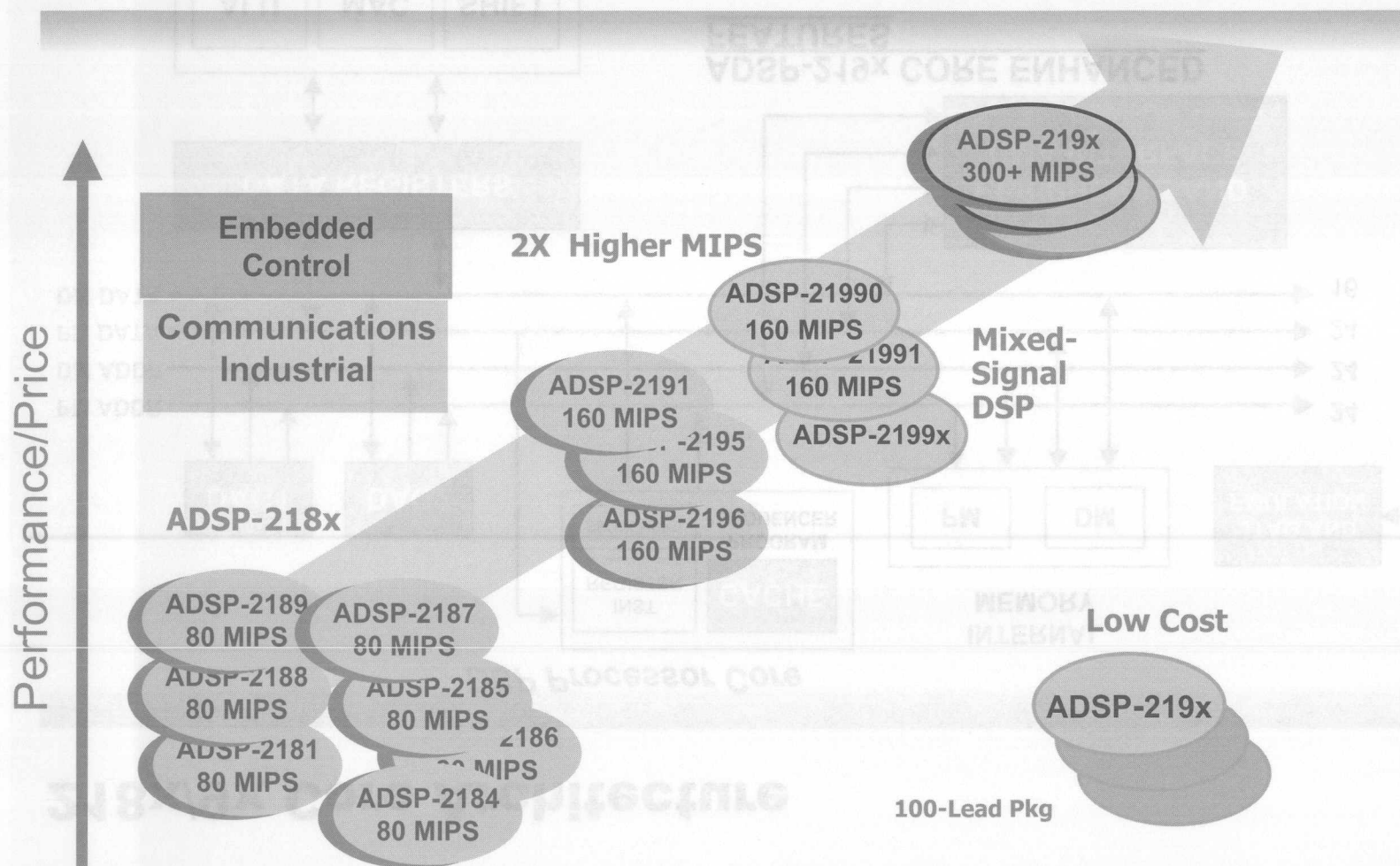
- ADSP—21532 Announced in September 2001 for Samples in Summer 2002
- C5502 Announced in July 2001 for Samples in 1Q02
- ADSP-21532 Positioned at Same Price as C5502
 - With on-chip regulator, further reducing system cost
 - I²S and Video ITU-R 656 interfaces
- ADSP-21532 Positioned at > 50% Higher Performance than C5502

	ADSP-21532	320C5502
Speed	300 MHz, 600 MMAC	200 MHz, 400 MMAC
SRAM	84 KB	64 KB
Ext. Memory Interface	16-Bit	32-Bit
Serial Ports, Watchdog, RTC	Y	Y
UART/Timer	ITU-R 656	Host Port
Core Voltage	2.25V–3.6 V Regulated	1.5 V
10K _u Price	\$9.95	\$9.95

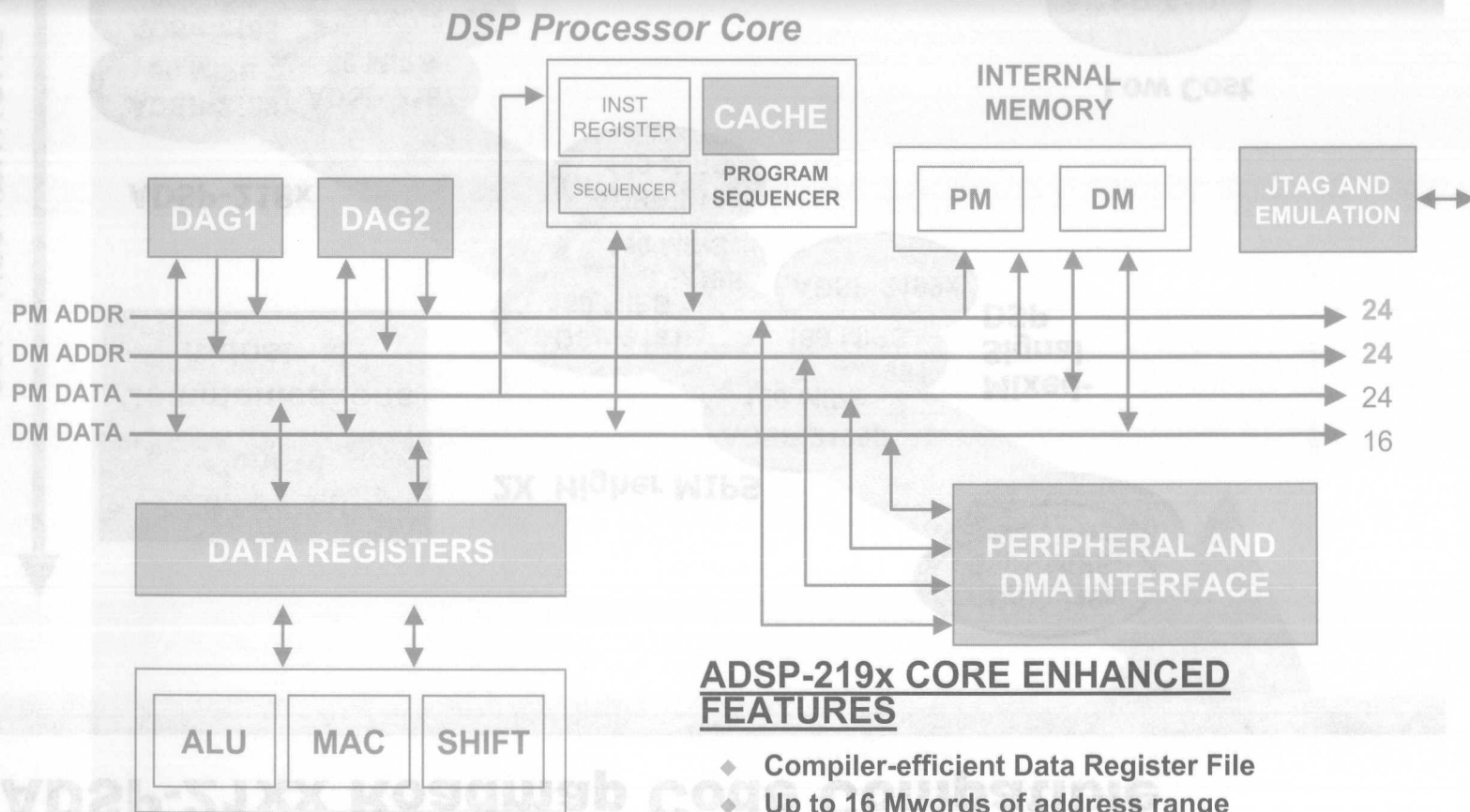
ADSP-21xx Overview

- ADSP-218xN DSPs Released at 80 MHz, Commercial and Industrial Temperature Ranges
 - ADSP-2184, ADSP-2186, ADSP-2185, ADSP-2187, ADSP-2189, ADSP-2188 pin-pin compatible
- ADSP-219x Family Introduced with Three Members at 160 MHz
 - ADSP-2196, ADSP-2195, ADSP-2191 pin-pin compatible
- ADSP-2196 Achieves 160 MIPS for under \$10
- ADSP-2195, ADSP-2196 On-Chip ROM Reduces System Cost in High Volume Applications
 - Low Risk development path, with full RAM ADSP-2191

ADSP-21xx Roadmap Code Compatible



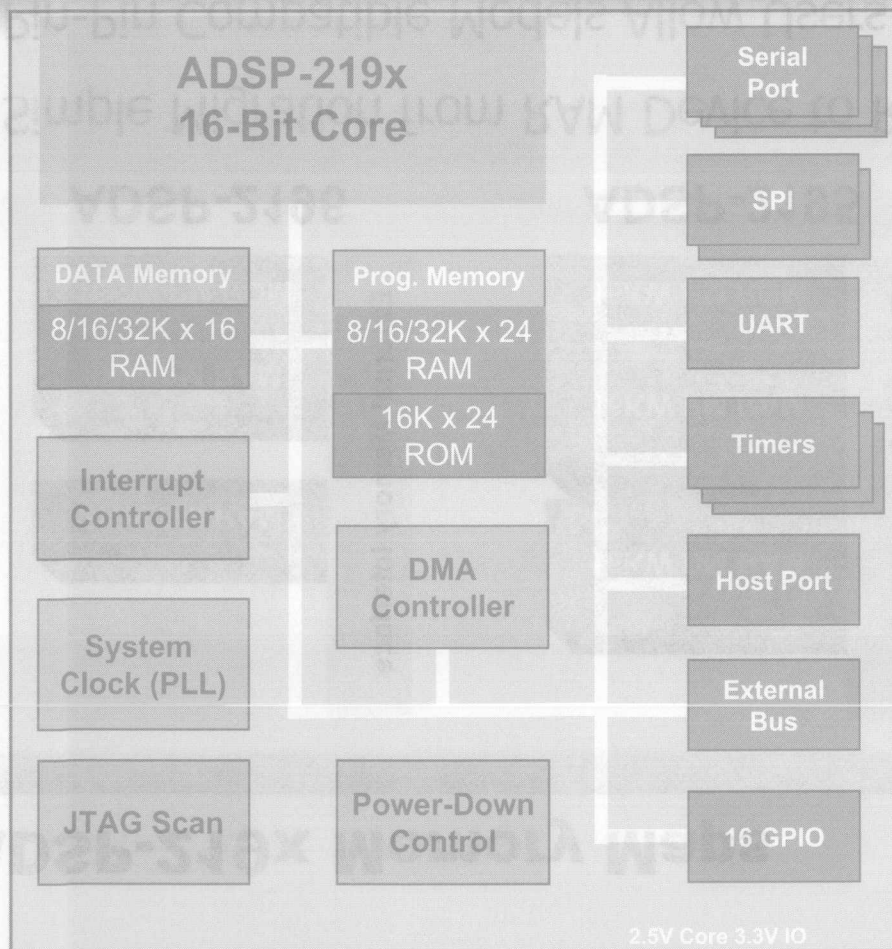
218x/9x Core Architecture



ADSP-219x CORE ENHANCED FEATURES

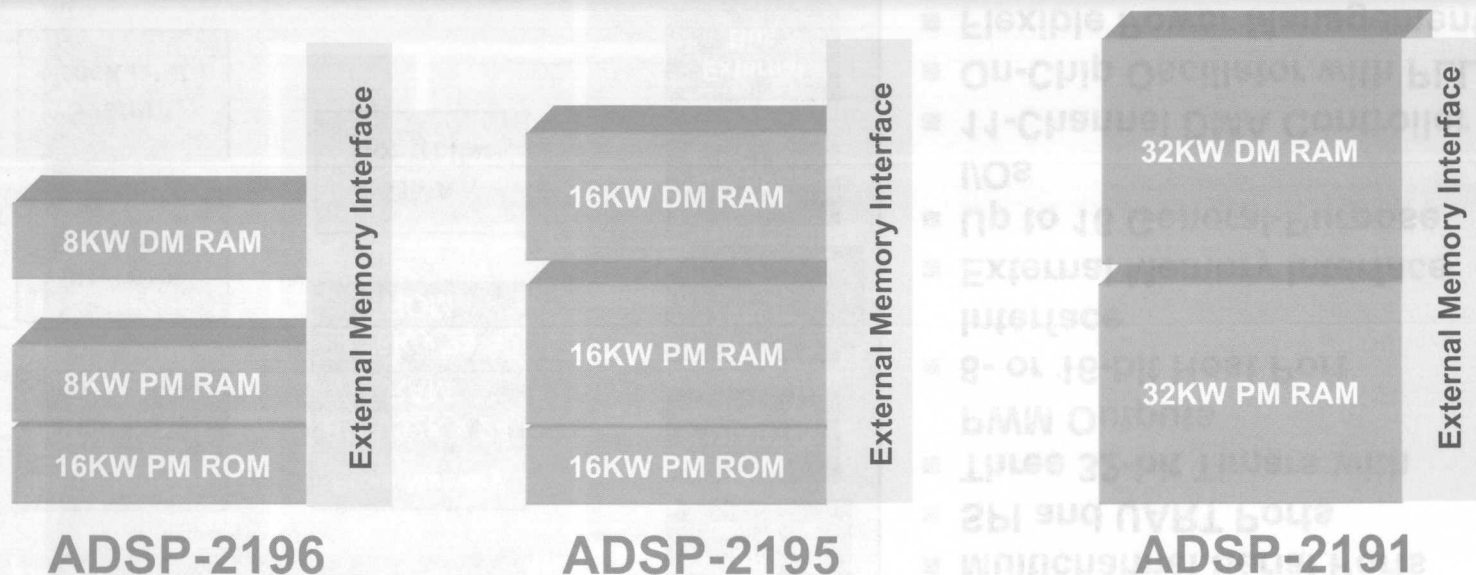
- ◆ Compiler-efficient Data Register File
- ◆ Up to 16 Mwords of address range
- ◆ Unified memory space
- ◆ Instruction Cache

ADSP-219x Product Features



- 160 MIPS
- Up to 64 KWords RAM
- Boot ROM
- Multichannel Serial Ports
- SPI and UART Ports
- Three 32-bit Timers with PWM Outputs
- 8- or 16-bit Host Port Interface
- External Memory Interface
- Up to 16 General-Purpose I/Os
- 11-Channel DMA Controller
- On-Chip Oscillator with PLL
- Flexible Power Management
- JTAG Port for System Test and Debug
- Industrial Grade
- 144 BGA and QFP Packages

ADSP-219x Memory Maps



- Simple Migration from RAM Device to ROM Production Device
- Pin-Pin Compatible Models Allow Users to:
 - migrate to smaller memory to reduce system costs or
 - move to larger memory models to increase end-product functionality

Telephony Algorithms

- Off-the-Shelf Voice and Data Algorithms Available Now for Complete Telephony System Solutions
- Algorithms are Optimized for Maximum Channel Capacity per DSP
- Customer Specific Algorithms Available on Request

Vocoders	Description	Peak MIPS
Voice Coders – (Choice of speech compression algorithms)	G.729AB	13.5
	G.723.1A	21.7
	G.728	29
	G.726	9.7
	G.722	12.9
	G.711	0.2
Auxiliary		
Jitter Buffer Tone Detection System Echo Cancellation VAD	Adaptive	1
	Voice/Fax/Data	2.5
	G.168 (16 ms)	5.4
	G.168 (32 ms)	8.5
	Voice Activity Detection	CS
Signalling Detection and Generation	Call Progress	CS
	Caller ID	CS
	DTMF	<1
	E&M Signalling	<0.5

ADSP-ADI 219x Competitive Advantages

- High Level of System Integration Lowers System Cost
- Efficient C/C++ Compiler Maximizes Code Density and Reduces Development Time
- Code-compatible Roadmap beyond 300 MIPS

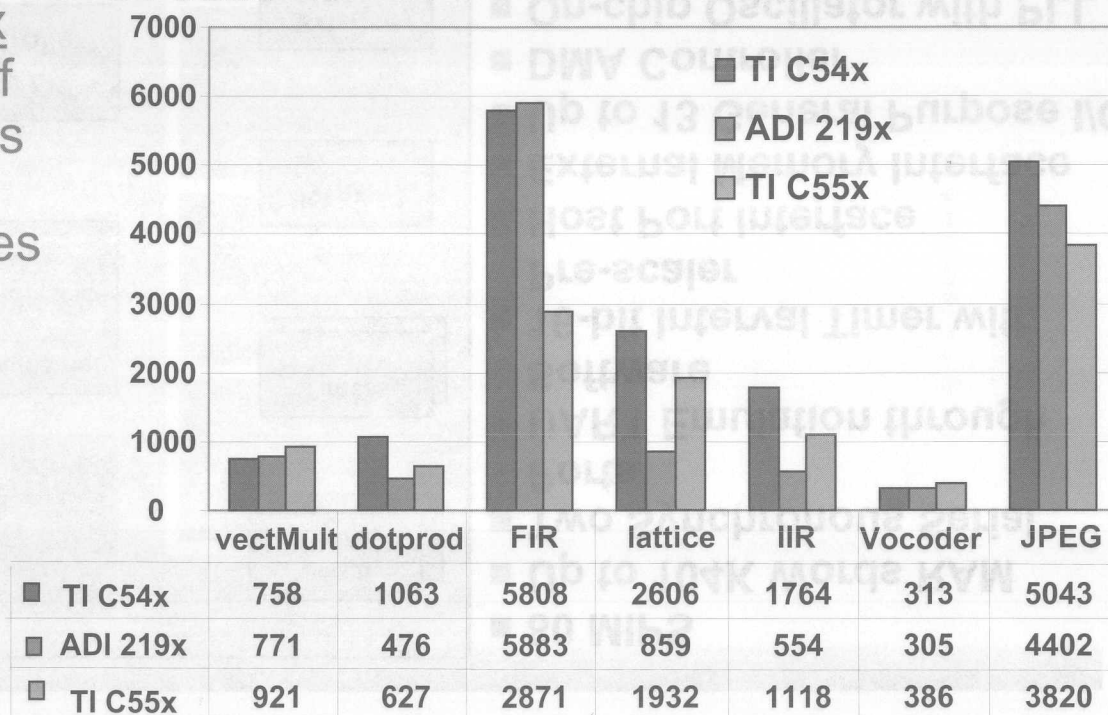
	ADI 219x	TI C54x	MOT 52000
MHz	160	160	15.18
MIPS	160	160	15.18
DMA Channels	11	6	6
External Address Space	16M Word	8M Word	16M Word
UART	1	0	0
Timers	Three 32-bit	One 16-bit	Three 4-bit
GPIO Pins	16	0	16
Compiled Code Size	0.7	1	-

ADSP-219x vs. C54x/C55x Compiler Benchmarks

- 219x Compiler Outperforms C54x and C55x in five of seven Benchmarks
- Fewer Clock Cycles Per DSP Function Reduces Code Size and System Power Consumption

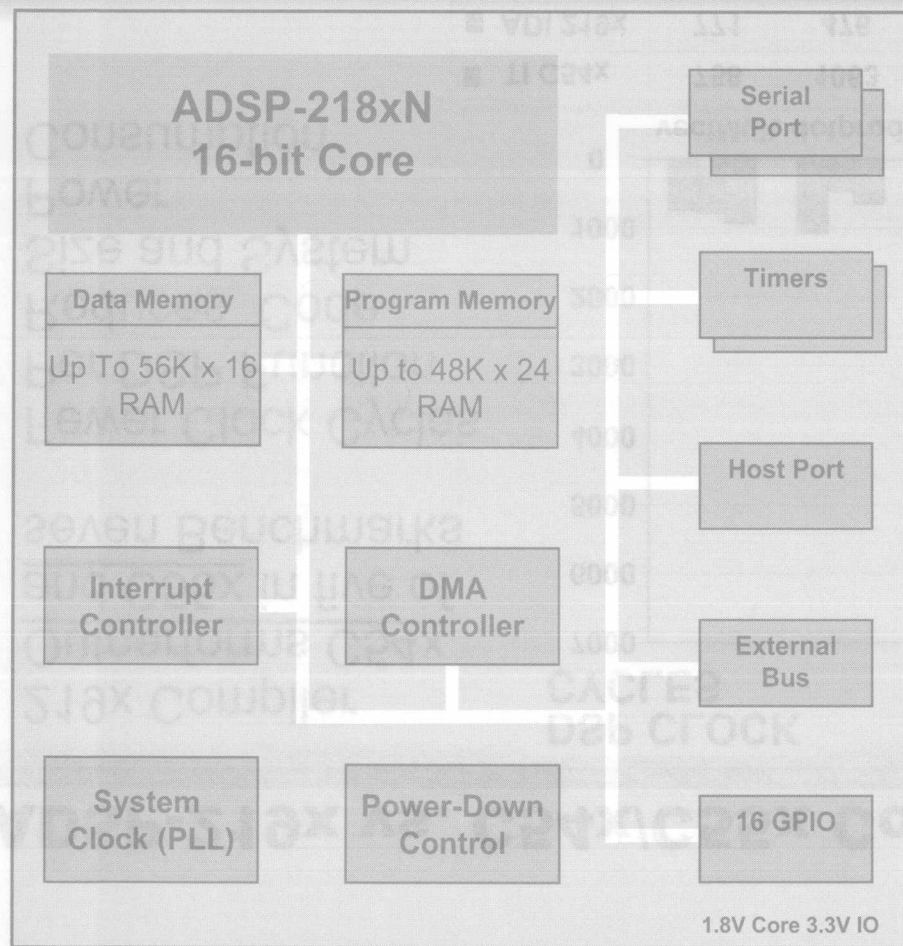
DSP CLOCK CYCLES

SMALLER IS BETTER



Source: Analog Devices

ADSP-218x Product Features



- 80 MIPS
- Up to 104K Words RAM
- Two Synchronous Serial Ports
- UART Emulation through Software
- 16-bit Interval Timer with Pre-scaler
- Host Port Interface
- External Memory Interface
- Up to 13 General Purpose I/O
- DMA Controller
- On-chip Oscillator with PLL
- Flexible Power Management
- EZ ICE Port for System Test and Debug
- Industrial Grade
- 144 BGA and QFP Packages

ADSP-218xN Series

■ All Models

- Operate at 80 MHz/MIPS and down to 1.8 V for low power applications
- Are power efficient — as low as 0.31 mA/MIPS for the series
- Are pin-compatible with memory sizes from 40 Kbytes to 256 Kbytes
- Integrate dual serial ports, byte-wide DMA, and 16-bit-wide host DMA

ADSP-218xN Series Memory Options

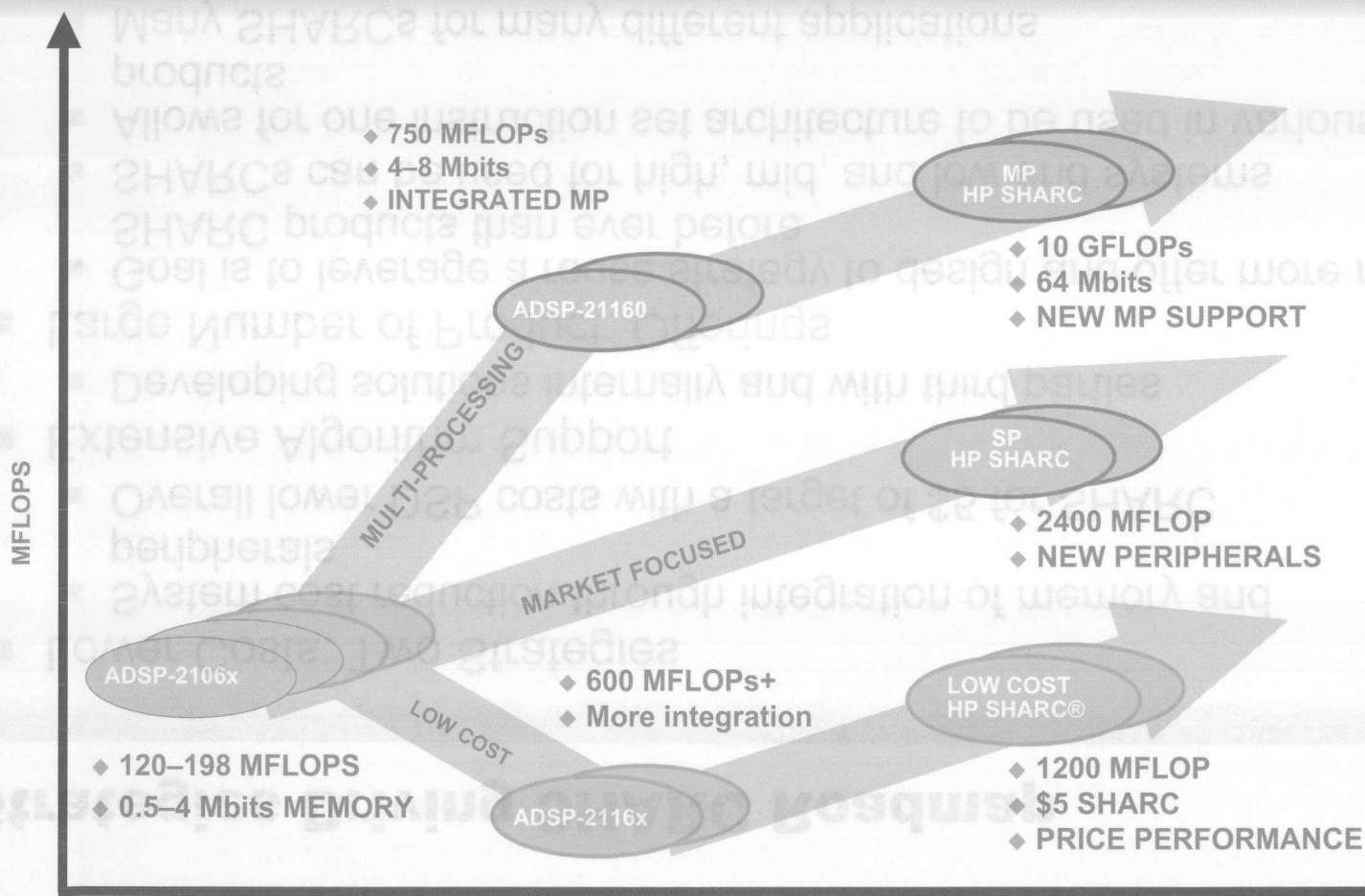
Models	Program RAM	Data RAM
ADSP-2184N	4K	4K
ADSP-2186N	8K	8K
ADSP-2185N	16K	16K
ADSP-2187N	32K	32K
ADSP-2189N	32K	48K
ADSP-2188N	48K	56K

Features and Benefits

Features	Benefits	219x	218x
Large on-chip RAM	Reduces system cost, allows DSP to sustain a higher performance	X	X
Glueless 8- or 16-bit Host Port Interface	Allows an external host device to boot the DSP and access the DSP's on-chip memory space	X	X
Multichannel synchronous serial ports	Supports T1/E1/H.100 standards with A-law and μ -law companding in hardware	X	
2 Serial Peripheral Interface (SPI) Ports	Compatible with low cost SPI devices	X	
UART Interface	Provides simplified serial communication to peripherals and host processors	X	
General-Purpose I/O pins	User programmable I/O pins for application specific requirements	X	X
Programmable PLL supports 1x to 32x frequency multiplication	Enables full speed operation from low speed input clocks	X	X
On-chip boot ROM with multiple boot strapping modes	Flexible boot methods: Boot from EEPROM, UART, SPI, or HPI 8/16 bit host ports or execute from Ext Mem	X	
144 BGA/LQFP Package	10mm x 10mm Small package option for space constrained applications	X	X

144 BGA QFP package	space constrained applications 10mm x 10mm small package option for	X	X
surface mount	boards or execute from Ext Mem		
On-chip boot ROM with multiple boot	EEPROM, UART, SPI, or I ² C serial ports	X	
32x frequency multiplication	flexible boot methods: boot from		
programmable PLL subblocks (x to	speed input clocks	X	X
General-purpose I/O pins	Enables full speed operation from low		
UART interfaces	application specific requirements	X	X
boards	User programmable I/O pins for		
3 serial peripheral interfaces (SPI)	to peripherals and user processors	X	
boards	Communication		
High-frequency synchronous serial	Compatible with low cost SPI devices	X	
interfaces	low and high combined in package		
clocks	subblocks (1, 2, 3, 4) for synchronous with A-	X	
large on-chip RAM	DSP and address bus (up to 8 on-chip		
features	DSP and address bus (up to 8 on-chip	X	
	ensuring a high performance		
	Reset		
	Resets	X	X
	Resets		

SHARC Roadmap— 10 Years of Code Compatibility



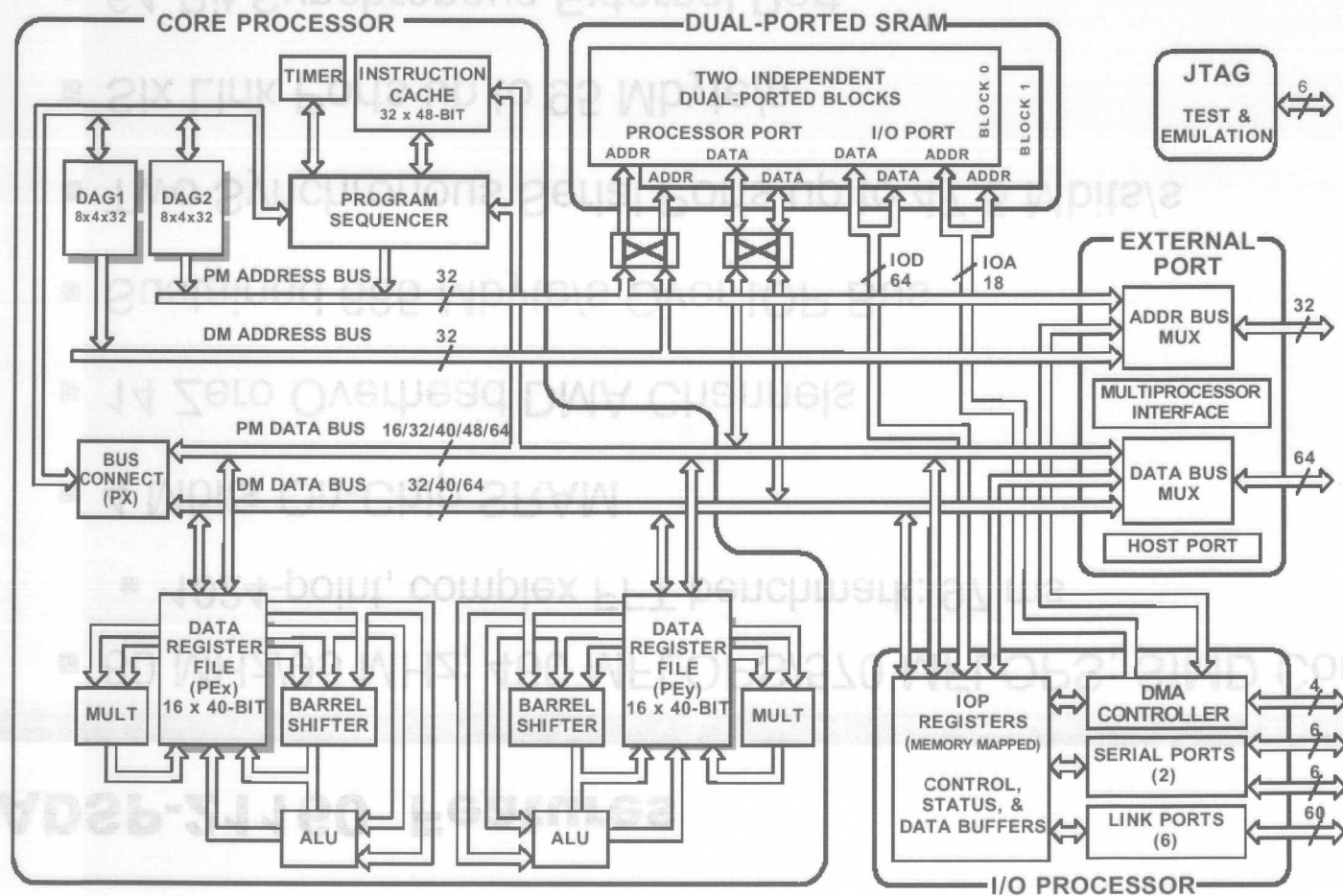
Strategies Driving SHARC Roadmap

- Lower Costs: Two Strategies
 - System cost reduction through integration of memory and peripherals
 - Overall lower DSP costs with a target of \$5 for SHARC
- Extensive Algorithm Support
 - Developing solutions internally and with third parties
- Large Number of Product Offerings
 - Goal is to leverage a reuse strategy to design and offer more new SHARC products than ever before
 - SHARCs can be used for high, mid, and low end systems
 - Allows for one instruction set architecture to be used in various products
 - Many SHARCs for many different applications
- Higher Performance
 - With the latest CMOS processes and improvements to the architecture, new performance levels will be achieved

ADSP-21160 Features

- 80 MHz/95 MHz; 480 MFLOPS/570 MFLOPS; SIMD Core
 - 1024-point, complex FFT benchmark: 97 ms
- 4 Mbits On-Chip SRAM
- 14 Zero Overhead DMA Channels
- Sustained 665 Mbyte/s Over IOP Bus
- Two Synchronous Serial Ports up to 47.5 Mbits/s
- Six Link Ports up to 95 Mbyte/s
- 64-Bit Synchronous External Port
- Cluster Multiprocessing Support

ADSP-21160 Internal Architecture



ADSP-21160 Benchmarks

	ADSP-21060	ADSP-21160 SISD	ADSP-21160 SIMD (Multichannel)
Clock Cycle	40 MHz	95 MHz	95 MHz
Instruction Cycle Time	25 ns	10.4 ns	10.4 ns
MFLOPS Sustained	80 MFLOPS	190 MFLOPS	380 MFLOPS
MFLOPS Peak	120 MFLOPS	285 MFLOPS	570 MFLOPS
1024 Point Complex FFT (Radix 4, with Bit Reversal)	460 μ s	460 μ s	460 μ s
FIR Filter (per Tap)	25 ns	10.4 ns	5.2 ns
IIR Filter (per Biquad)	100 ns	42 ns	21 ns
Matrix Multiply (Pipelined) [3 x 3] x [3 x 1] [4 x 4] x [4 x 1]	225 ns 400 ns	94 ns 166 ns	47 ns 83 ns
Divide (y/x)	150 ns	62 ns	31 ns
Inverse Square Root	225 ns	94 ns	47 ns

ADSP-2116x Family

- Start of a New Generation of SHARCs
- Code-Compatible with ADSP-2106x SHARC
- Increased Performance with:
 - Higher clock rate
 - SIMD architecture
 - Higher data bus bandwidth
- ADSP-21160 was First Family Member
- ADSP-21161 Extends SHARC Performance and Value

ADSP-2116x SHARC Core

- SIMD Core Provides Significant Performance Increases on Key Signal Processing Benchmarks
- Designed and Optimized for Signal Processing
- Code-Compatible with First-Generation SHARC

Optimized for Signal Processing
SIMD Architecture

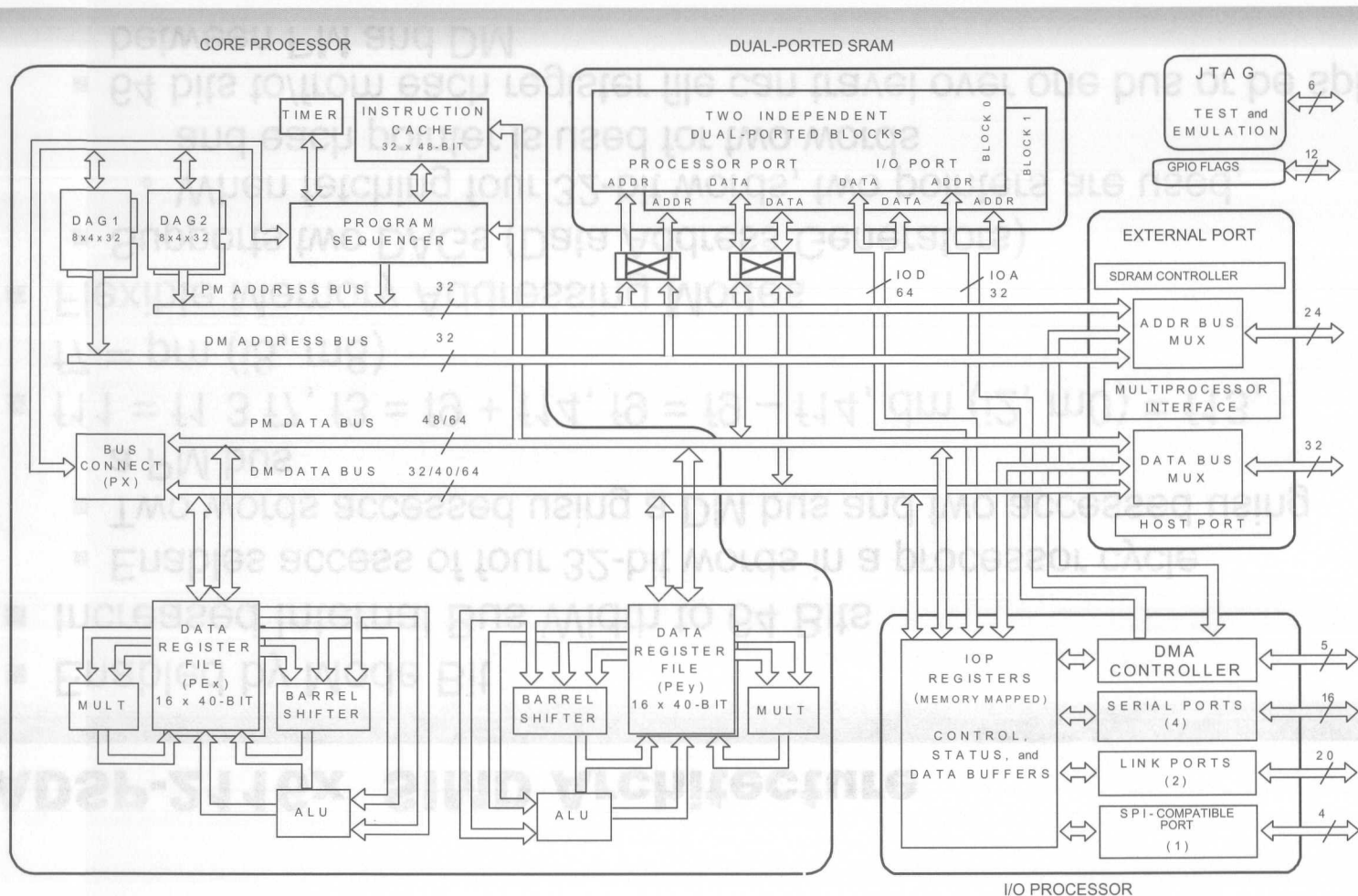
SIMD Architecture Optimized for Signal Processing

- Doubles Processor Performance while Minimizing Code Size and Power Consumption
 - One instruction now does twice the work
- Adds Second Set of Computational Units
 - Two ALUs, two multipliers, two shifters, two register files
- Two Sets of Computational Units Operate in Parallel to Decrease Benchmark Times Up to 2x
 - A 50 TAP FIR filter in a non-SIMD machine takes 50 processor cycles
 - A 50 TAP FIR filter in a SIMD machine takes 25 cycles

ADSP-2116x SIMD Architecture

- Enabled by Mode Bit
- Increased Internal Bus Width to 64 Bits
 - Enables access of four 32-bit words in a processor cycle
 - Two words accessed using a DM bus and two accessed using a PM bus
- $f_{11} = f_1 \oplus f_7$, $f_3 = f_9 + f_{14}$, $f_9 = f_9 - f_{14}$, $dm(i_2, m_0) = f_{13}$, $f_7 = pm(i_8, m_8)$
- Flexible Memory Addressing Modes
 - Supports two DAGs (Data Address Generators)
 - ◆ When fetching four 32-bit words, two pointers are used, and each pointer is used for two words
 - 64 bits to/from each register file can travel over one bus or be split between PM and DM

The ADSP-21161 Architecture Block Diagram



ADSP-21161 Features and Benefits

FEATURE	BENEFIT
600 MFLOP Core	Enables the fast execution of highly complex signal processing algorithms
1 Mbit Dual-Ported SRAM	Dual-ported nature increases data bandwidth and processing speed
14 Channels of Zero Overhead DMA	No cycles stolen from the core to move data on and off chip
Two 100Mbyte/second Link Ports	Simplifies connection and communication in multiprocessing systems
Cluster Multiprocessing Support	Enables universally addressable multiprocessing memory system
Host Interface through SPI and Parallel Bus	Allows for low and high bandwidth host processor communications
SDRAM Controller	Mechanism for controlling large banks of fast, inexpensive SDRAM
Four Serial Ports	Allows for 16 channels of data to be transferred in and out of the DSP

ADSP-21161N Features

- ADSP-2116x SHARC SIMD Core 3.3 V External/1.8 V Internal
- SPORT Pins: 5 V Tolerant I/O
- 100 MIPs, 600 MFLOPs Peak
- 1 MB On-Chip SRAM
- 14 Zero-Overhead DMA Channels
- SDRAM Controller for Glueless Interface to Low Cost Memory
- External Instruction Cache Mode
- SPI-Compatible Port for Host and Peripheral Control
- Two Link Ports, 12 General-Purpose I/O Lines, Four IRQ lines, One Timer
- Four SPORTs Supporting 128-Channel TDM and I²S

ADSP-21161 Performance Benchmarks

	ADSP-21060	AD21161 SISD	AD21161 SIMD (MultiChannel)
Clock Cycle	40 MHz	100 MHz	100 MHz
Instruction Cycle Time	25 ns	10 ns	10 ns
MFLOPS Sustained	80 MFLOPS	200 MFLOPS	400 MFLOPS
MFLOPS Peak	120 MFLOPS	300 MFLOPS	600 MFLOPS
1024 Point Complex FFT (Radix 4, with Bit Reversal)	92 μ s	92 μ s	92 μ s
FIR Filter (per Tap)	25 ns	10 ns	5 ns
IIR Filter (per Biquad)	100 ns	40 ns	20 ns
Matrix Multiply (Pipelined) [3 x 3] x [3 x 1] [4 x 4] x [4 x 1]	225 ns 400 ns	90 ns 160 ns	45 ns 80 ns
Divide (y/x)	150 ns	60 ns	30 ns
Inverse Square Root	225 ns	90 ns	45 ns

TigerSHARC® Static Superscalar Architecture: Blend of Proven Architectures

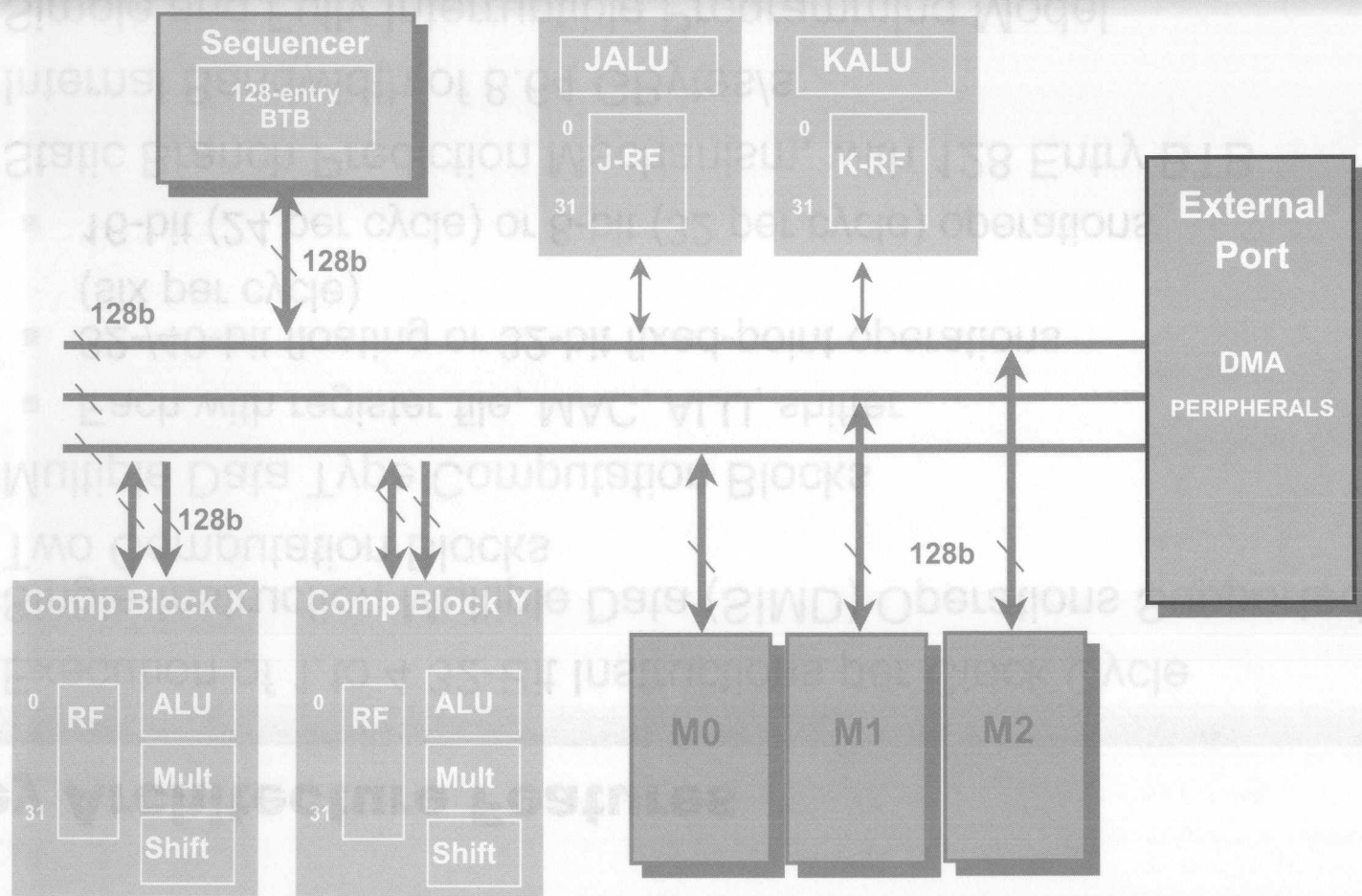
- Load/store architecture
- Deeply pipelined for high clock rates
- Branch prediction
- Large interlocked register file
- Compiler friendly



- Instruction level parallelism determined prior to run time in multi-instruction lines
- Code efficiency

- Determinism and real-time execution
- Fast and responsive interrupt system
- I/O and internal memory capable of sustaining core rates
- Fast multiply accumulates, HW support for circular buffers
- Bit reverse, zero overhead looping

TigerSHARC Block Diagram

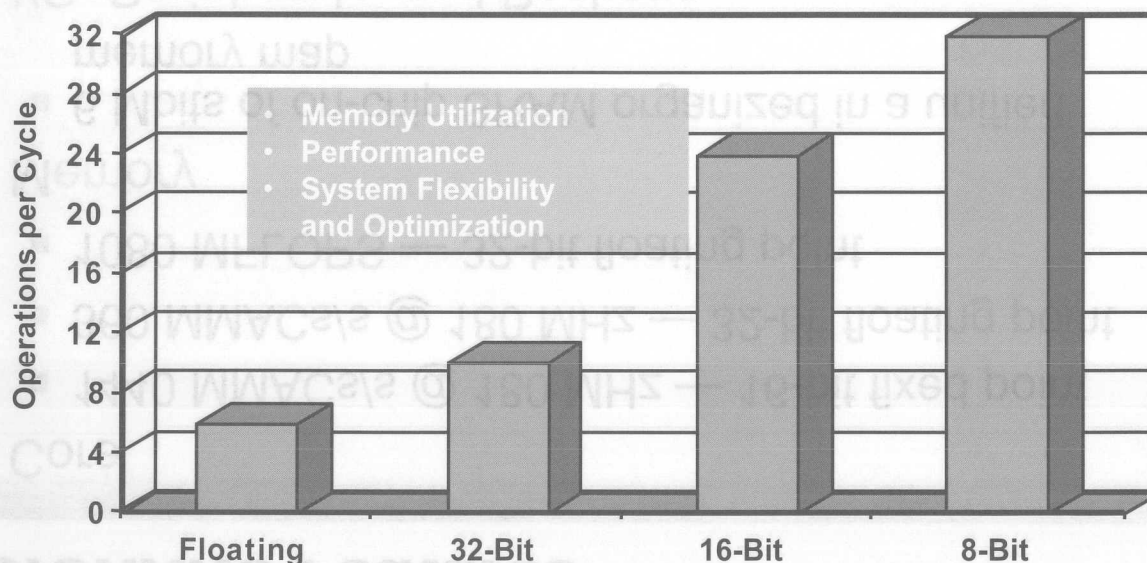


Key Architecture Features

- Execution of 1 to 4 32-Bit Instructions per Clock Cycle
- Single-Instruction Multiple Data (SIMD) Operations Supported by Two Computation Blocks
- Multiple Data Type Computation Blocks
 - Each with register file, MAC, ALU, shifter
 - 32-/40-bit floating or 32-bit fixed-point operations (six per cycle)
 - 16-bit (24 per cycle) or 8-bit (32 per cycle) operations
- Static Branch Prediction Mechanism, with 128 Entry BTB
- Internal Bandwidth of 8.64 GBytes/s
- Simple and Fully Interruptible Programming Model

TigerSHARC: First DSP to Support Multiple Data Types on One Chip

- The TigerSHARC Natively Supports Multiple Data Types
 - 8-bit, 16-bit, 32-bit fixed-point and floating-point
 - Native support scales performance to the task



Note: Up to 256 bits of data can be transferred to and from internal memory in the same cycle

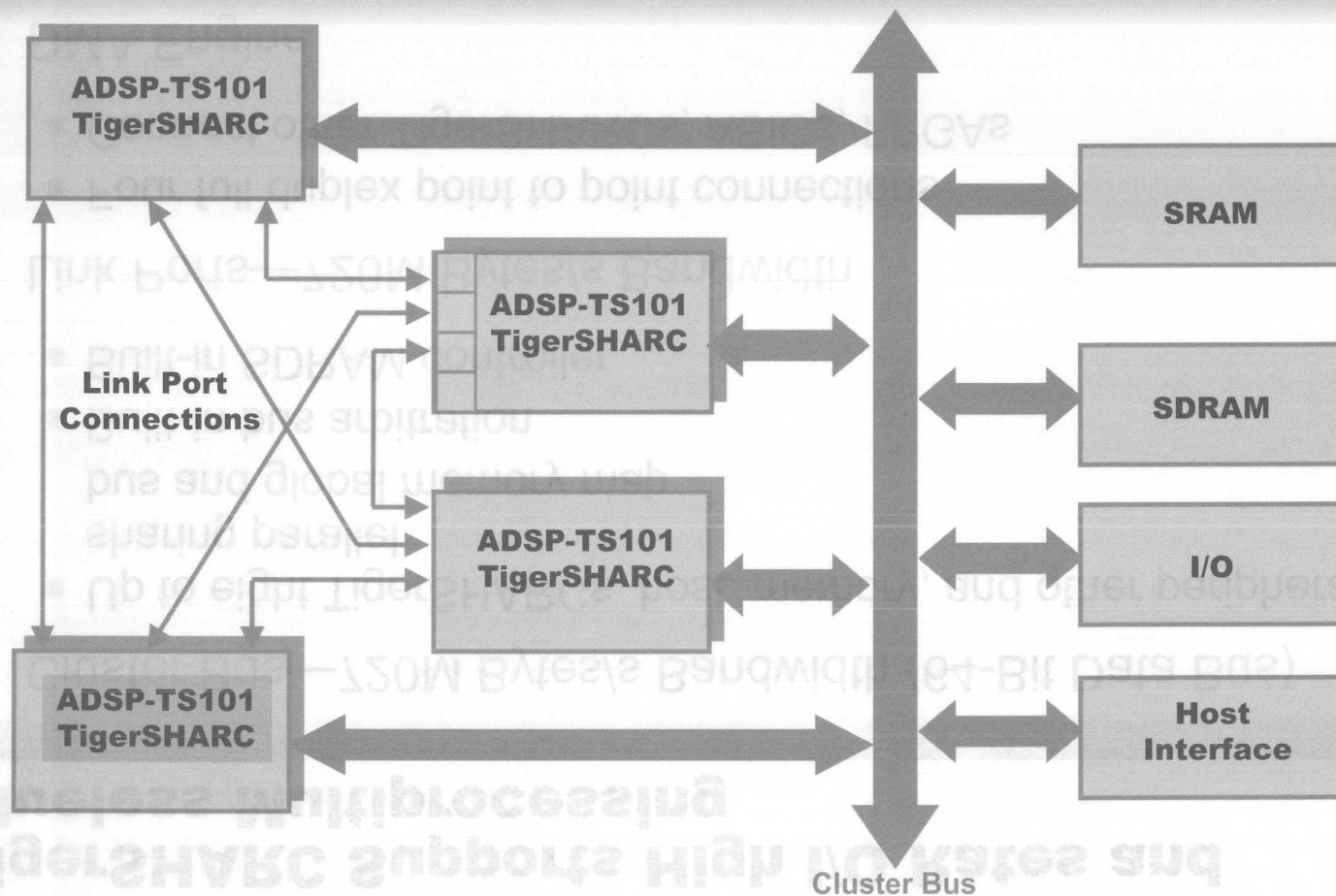
TigerSHARC Features

- Core
 - 1440 MMACs/s @ 180 MHz — 16-bit fixed point
 - 360 MMACs/s @ 180 MHz — 32-bit floating point
 - 1080 MFLOPS — 32-bit floating point
- Memory
 - 6 Mbits of on-chip SRAM organized in a unified memory map
- I/O, Peripherals, and Package
 - 720 Mbytes/s transfer rate through external bus.
 - 720 Mbytes/s aggregate transfer rate through four link ports
 - Glueless MP cluster support for up to eight TigerSHARCs
 - SDRAM controller
 - 19 mm x 19 mm, 484-Ball, PBGA, ADSP-TS101SKB1180x
 - 27 mm x 27 mm, PBGA package, ADSP-TS101SKB2180x

TigerSHARC Supports High I/O Rates and Glueless Multiprocessing

- Cluster Bus—720M Bytes/s Bandwidth (64-Bit Data Bus)
 - Up to eight TigerSHARCs, host, memory, and other peripherals sharing parallel bus and global memory map
 - Built-in bus arbitration
 - Built-in SDRAM controller
- Link Ports—720M Bytes/s Bandwidth
 - Four full duplex point to point connections
 - Connect other TigerSHARCs, ASICs, FPGAs
- DMA Engine
 - 14 channels
 - Zero overhead DMA

Multiprocessing Communication via Link Ports and Cluster Bus



TigerSHARC Benchmarks @ 180 MHz

- 16-Bit Performance — 1440 MMACs/s Peak Performance

Algorithm	Execution Time	Cycle to Execute
256-Point Complex FFT (Radix 2)	6.1 μ s	1100
50 Tap FIR on 1024 inputs	40 μ s	7200
Single FIR MAC	0.78 ns	0.14
Single Complex FIR MAC	3.17 ns	0.57
Single FFT Butterfly	5.6 ns	1.0

TigerSHARC Benchmarks @ 180 MHz

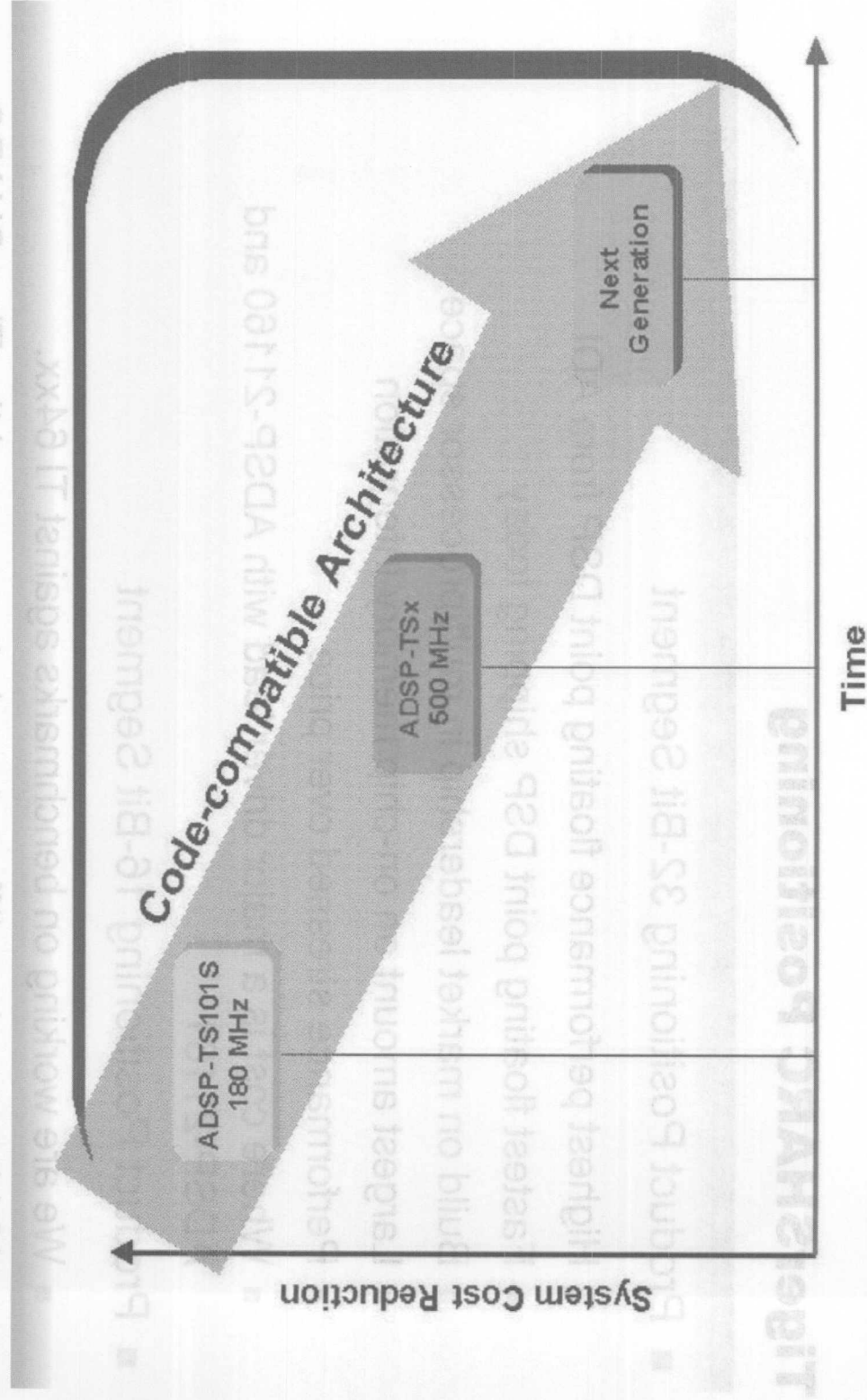
- 32-Bit Performance — 360M MACs/s Peak Performance

Algorithm	Execution Time	Cycle to Execute
1024-Point Complex FFT (Radix 2)	68 μ s	12300
50 Tap FIR on 1024 Input	153 μ s	27500
Single FIR MAC	3.1 ns	0.55
Single FFT Butterfly	11.1 ns	2.0
Single Complex FIR MAC	11.1 ns	2.0
Divide	16.7 ns	3.0
Square Root	27.8 ns	5.0
Viterbi Decode (per Add/Compare/Select)	2.8 ns	0.5

TigerSHARC Positioning

- Product Positioning 32-Bit Segment
 - Highest performance floating point DSP from ADI
 - Fastest floating point DSP shipping today
 - Build on market leadership in multiprocessor space
 - Largest amount on on-chip memory integration
 - Performance stressed over price
 - Where cost is a major driver lead with ADSP-21160 and ADSP-21161
- Product Positioning 16-Bit Segment
 - We are working on benchmarks against TI 64xx.
 - 16-bit space is a different market space and the TigerSHARC will be priced to compete here.

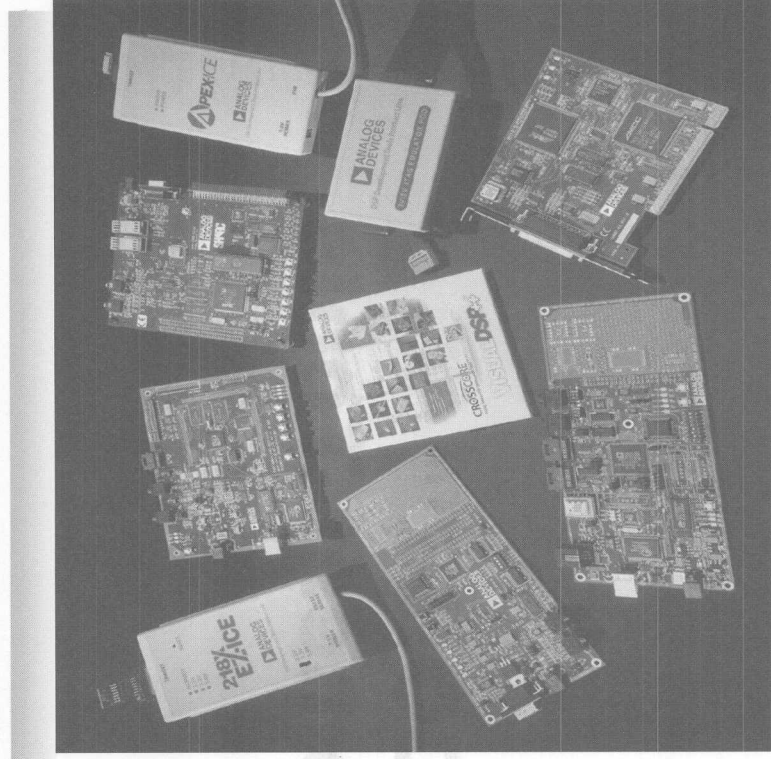
TigerSHARC Roadmap



CROSSCORE™ DSP Development Tools

C

- C
 - W
 - Emulators
 - ◆ USB
 - ◆ PCI
 - Evaluation Boards
 - ◆ EZ-KIT Lites
 - ◆ At least one for all platforms



What is VisualDSP++™

- VisualDSP++ is an integrated development environment that delivers efficient project management so programmers can easily move between editing, building, and debugging.
 - Key Features Include:
 - The VisualDSP++ Kernel (VDK)
 - C++ compiler
 - Advanced plotting tools enabling programmers to visually measure software performance
 - Statistical profiling to easily identify programming bottlenecks
- VisualDSP++ offers programmers a powerful programming tool with flexibility that significantly decreases the time required to port software code to a DSP, reducing time to market.

Features of VisualDSP++

VisualDSP++ 3.0

- Expert Linker
- VisualDSP Component Software Engineering (VCSE)
- Cache and Pipeline Viewer
- VisualDSP++ RTOS/Kernel/Scheduler (VDK)
- High Level Language Including C++
- Rich Debug Ability Including MP Support
- Advanced Plotting and Profiling Features
- Interfacing to VisualDSP++
- Easy to Test and Verify Applications with TCL Scripts
- Easy to Learn with Online Help

Expert Linker

- Graphical Alternative to Linker Definition File (LDF) Text Format
 - Though powerful, the LDF format is intimidating to new users, especially those with limited experience in embedded programming
- Graphical Tools to Create a Memory Map, Place Objects, Create Overlays, etc.
 - LDF autogenerated for linker consumption
 - “Round tripping” possible (GUI will consume existing LDF)
 - Will support pre-link visualization

“VCSE” VisualDSP++ Component Software Engineering

- Component-based Algorithm/Device Driver Development Approach with Tool's Support
 - Widely used in PC application development, now emerging in embedded development
- VisualDSP++ GUI Support for Component Creation, Browsing, and Utilization

Cache Visualization (Blackfin DSP)

- Statistics Gathered by PC Address/Source Line and Cache Line/set
 - Total cache accesses
 - Cache hits
 - Cache misses
 - Compulsory
 - Conflict
 - Capacity
- Visualization within VisualDSP++ at Run-Time
 - Histogram by source, cache line display, summary

VisualDSP++ Kernel (VDK)

- Faster Time to Market, No Need to Develop or Maintain Homemade Kernel
- Efficient Debugging of Applications with Kernel Analysis Tools
- Reduce Cost of Software Maintenance with Code Reuse and Standardized Software
- Standardized Code Enables Rapid Migration Across All DSP Platforms
- Royalty and NRE Free (No Risk to Use)
- Embedded in the IDE (Nothing Else to Install)

High Level Language Compilation

- C/C++ support
 - High level languages (HLL) can shorten customers' time to market. HLLs are more common, allowing for a greater talent pool to take advantage of the real-time processing performance offered by DSPs.
 - "Don't just do it, do it well!" ADI purchased Edinburgh Portable Compilers for their expertise in DSP compilation technology. They are intimately aware of the DSP architectures and the target applications, which leads to optimized C and C++ compilers.
 - ADI's C++ is based on superset of Embedded C++ standard that adds the code reuse aspect of C++ without bloating the compiled code.
 - Object-oriented programming shortens time to market.

Debug Features and MP Support

- Debug Features
 - Setting breakpoints and watchpoints allows user to halt the processor on various conditions
 - **For instance, a watchpoint can be set on a location in memory, but if the memory location is written to or read from the processor will halt.**
- Multiprocessor Support Features
 - Supports memory sharing among processors
 - Simple visual feedback for focusing on particular processor
 - Processor Status windows
 - Ability to control groups of processor together

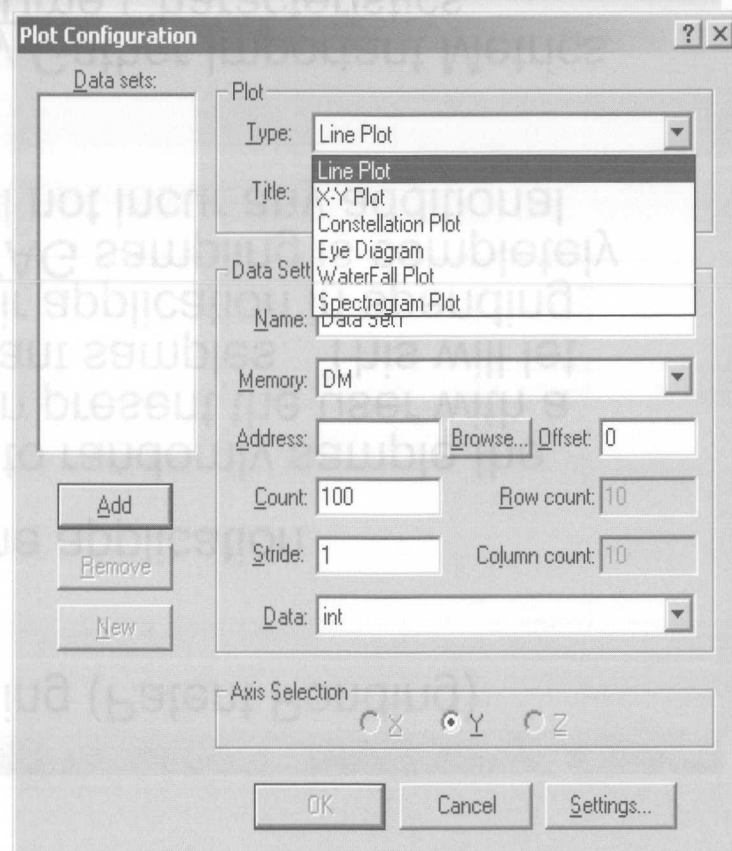
Statistical Profiling

- Non-Intrusive Statistical Profiling (Patent Pending)
 - Does not halt the DSP
 - No extra coded added to the application
- The Debugger has the ability to randomly sample the target processors PC and then present the user with a graphical display of the resultant samples. This will let the user easily see where their application is spending most of its time. Since the JTAG sampling is completely non-intrusive, this process will not incur any additional run-time overhead.
- Allows Developer to Passively Gather Important Metrics without Interrupting the Real-Time Characteristics
- Programmer Can Focus on Those Areas in the Program that Impact Performance and Take Corrective Action

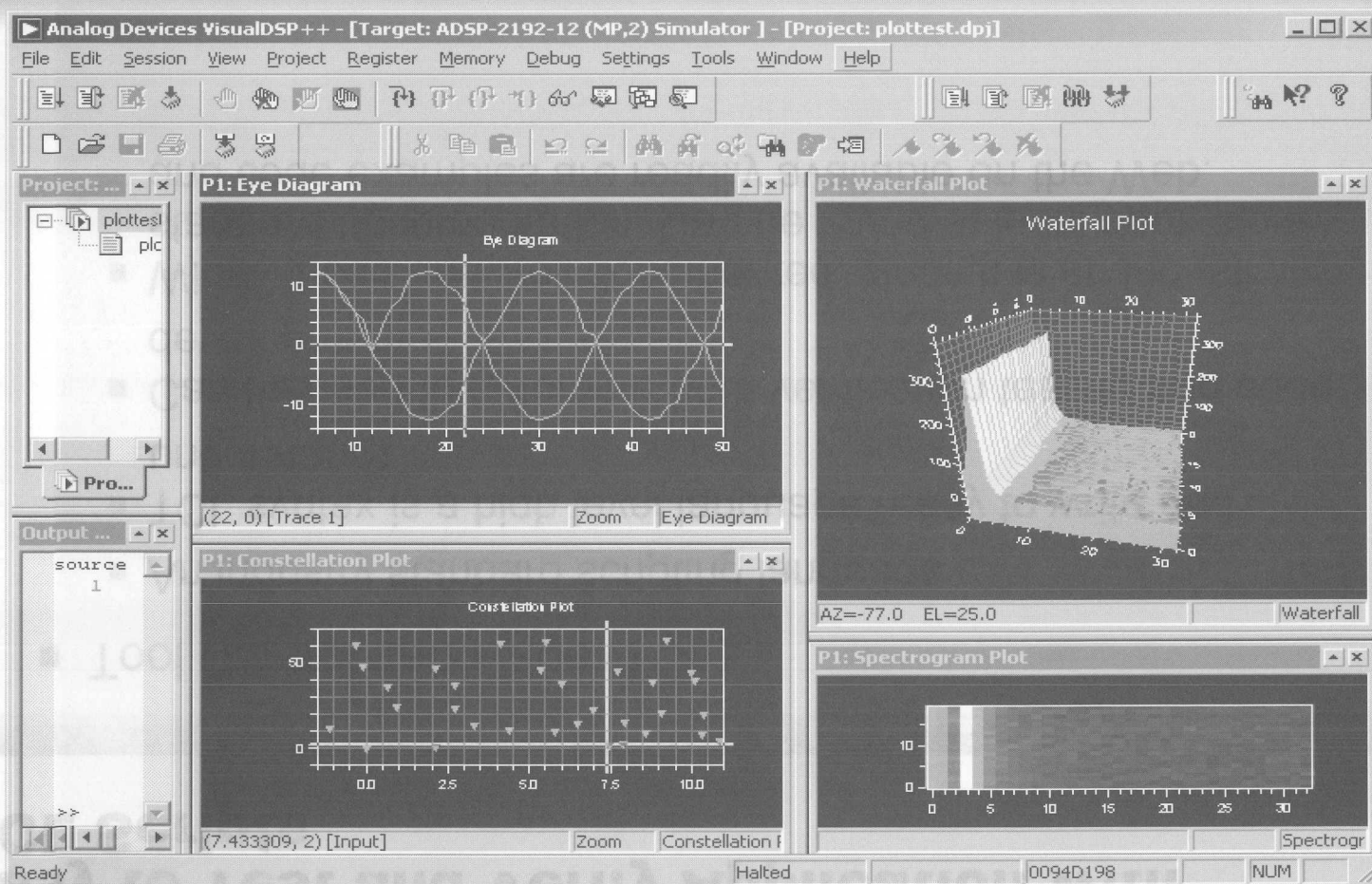
Advanced Plotting Capabilities

■ Visualize Application Results

- Plot various types of plots
- Includes special plot types for communications such as Constellation Plots and Eye Diagrams
- Settings for data processing on plot data. Convert to Db, FFT...



Advanced Plotting



Easy to Test and Verify Application with TCL Scripts

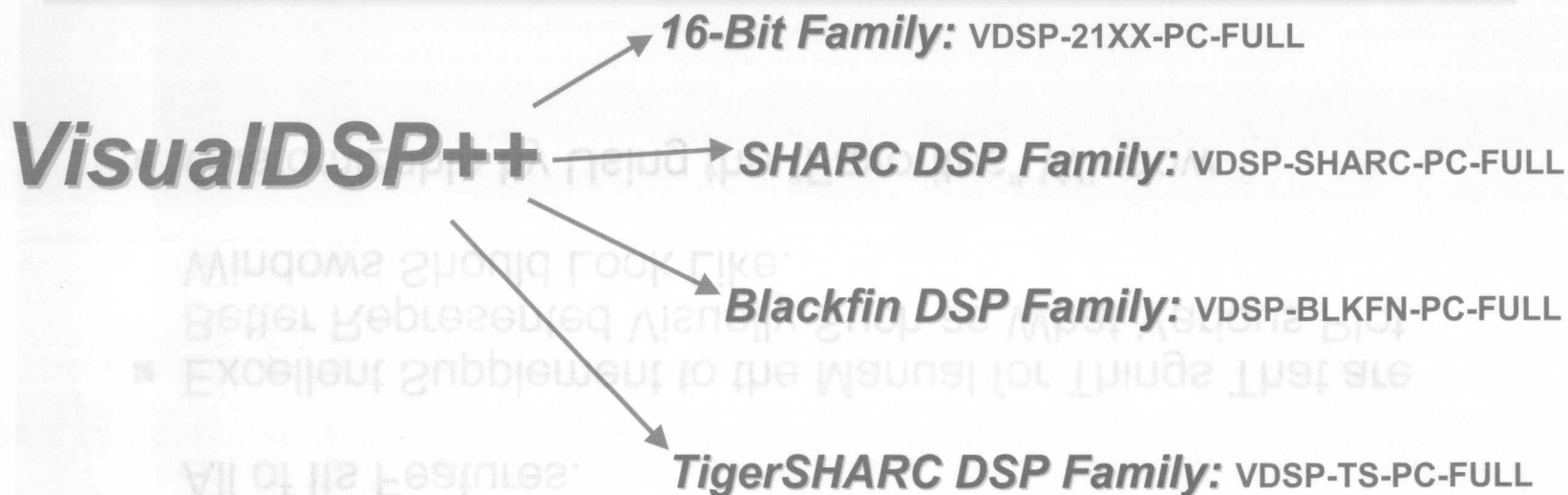
- Tool Control Language (TCL)
 - An industry standard scripting language
 - TCL syntax is a high level language (easy to write and understand)
 - Can be used to automate both verification testing and code development
 - Widely used and well documented, since it is an industry standard documentation. Can be found at local book stores and code examples are readily available on the Web.

Advanced Plotting

Easy to Learn with Online Help

- Fully Searchable and Indexed Online Help
- Includes Quick Overviews on Using VisualDSP++ and All of Its Features.
- Excellent Supplement to the Manual for Things That are Better Represented Visually Such as What Various Plot Windows Should Look Like.
- Customizable by Using the “Favorites” Window

Processors and Platforms Supported



Platforms Supported

- Windows 98, 2000
- Window NT

Packages Available for VisualDSP++

Product	Part Number	Price
VisualDSP++ Test Drive: 30-day free trial of VisualDSP++	VDSP-SHARC-PC-TEST VDSP-TS-PC-TEST VDSP-21XX-PC-TEST VDSP-BLKFN-PC-TEST	\$0.00
VisualDSP++: IDE, Debugger, C/C++ Compiler, Assembler, Linker, VDK, VCSE, with Emulation and Simulation Support	VDSP-SHARC-PC-FULL VDSP-TS-PC-FULL VDSP-21XX-PC-FULL VDSP-BLKFN-PC-FULL	\$3500.00
VisualDSP++ Floating License	VDSP-SHARC-PCFLOAT VDSP-TS-PCFLOAT VDSP-21XX-PCFLOAT VDSP-BLKFN-PCFLOAT	\$4250.00

VisualDSP++ Test Drive

- The Test Drive is a Free 30-day Trial of VisualDSP++. The Test Drive is a Full Version of VisualDSP++, No Limitations Other Than the Time Limit and contains PDFs of the VisualDSP++ Manuals.
- Test Drive CDs May Be Ordered from the Web Site or User May Download the Test Drives from the DSP Tools Web Site at: <http://www.analog.com/dsp/tools/>
- Test Drives Require Registration Online to Receive a Serial Number that Activates the Software:

http://forms.analog.com/Form_Pages/DSP/tools/visualDSPTestDrive.asp.

- The Test Drive Expires 30 Days from the Install.

Available Now for \$2992.00

Apex-ICE™ V2B Emulator

Separately, VisalD2B++

Software Sold

Windows 88, Windows 5000

Powered Externally

to Reach Targets

Meters in Length

Small Diameter Cable

Small Host

Portable Solution

DSPs

Emulator for Analog Devices JTAG

Universal Serial Bus (USB) Based

Emulators for Analog Devices DSPs

Apex-ICE™ V2B Emulator

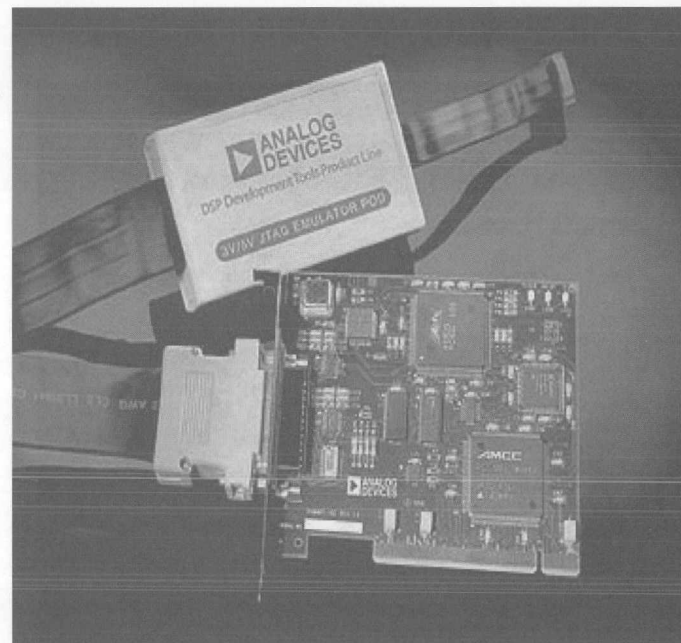
Apex-ICE™ USB Emulator

- Universal Serial Bus (USB)-Based Emulator for Analog Devices JTAG DSPs
- Portable Solution
- Small Hand-Held Unit
- Small Diameter Cable, 5 Meters in Length, for Hard to Reach Targets
- Powered Externally
- Windows 98, Windows 2000
- Software Sold Separately, VisualDSP++
- Part # ADDS-APEX-ICE Available Now for \$4995.00



Summit-ICE™ PCI Emulator

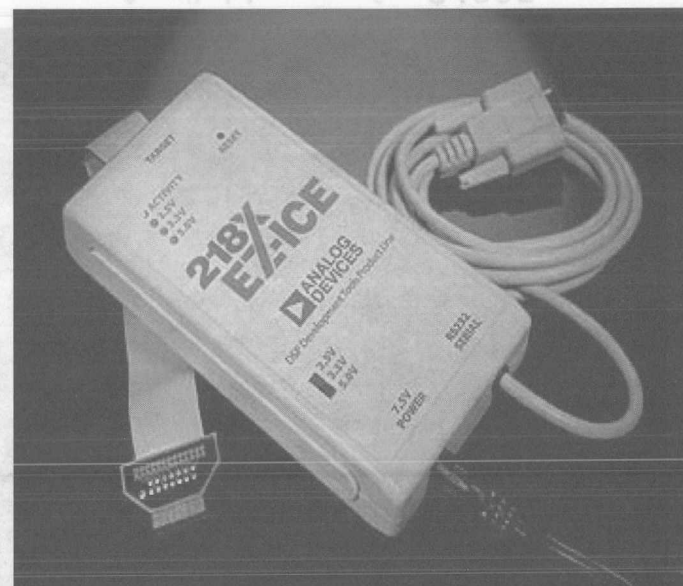
- 32-bit PCI interface Add-in Card
- Four-Inch, Flexible Shielded Target Board Cable for Easy Access to a 14-pin JTAG Header
- Embedded ICEPAC Technology Provides a Rugged and Reliable Solution
- Remote 3 V/5 V JTAG Pod with Extended, Shielded Cable (1.5 m)
- For Analog Devices JTAG DSPs
- Windows 98, Windows 2000
- Software sold Separately, VisualDSP++
- Part # ADDS-SUMMIT-ICE



Available now for \$4995

EZ-ICE® for the ADSP-218x DSP Family

- Serial Port Interface, Printed Circuit Board and 14-Pin Header
- Controls Equipment for Testing, Observing, and Debugging a Target System
- 6-Foot Cable
- Hardware Switch to Accommodate 2.5 V, 3.3 V, and 5 V
- Shielded Enclosure to Cover Bare Circuit Board
- Performance Increase via Faster Data Transfer
- Windows 9x, Windows 2000
- Software Sold Separately, VisualDSP++
- Part # ADDS-218X-ICE-2.5V



Available now for \$1,995

■ **694 # VDD2-51235-EZLITE**

AD2B-51232 EZ-KIT Lite Hardware

AD2B-51232 EZ-KIT Lite Hardware

- Evaluation suite of AD2B-51232: compiler, assembler, linker,

- Subsystem Win 98 or Win2000

■ **Software Features**

- Desktop standalone operation

- CE-compliant PCB and external power supply

■ **AD2B-51232 EZ-KIT LITES™**

for Analog Devices DSPs

- AD2B-51232 EZ-KIT Lite Hardware

- AD2B-51232 EZ-KIT Lite Hardware

- AD2B-51232 EZ-KIT Lite Hardware

- AD2B-51232 EZ-KIT Lite Hardware

- AD2B-51232 EZ-KIT Lite Hardware

AD2B-51232 EZ-KIT Lite™

ADSP-21535 EZ-KIT Lite™

- Hardware Features
 - ADSP-21535 DSP
 - 4 M x 32-bit SDRAM
 - 272 Kx16-bit FLASH memory
 - AD1885 48 kHz AC'97 SoundMax® codec
 - ADP3088 Analog Devices switching regulator for core power management
 - JTAG ICE 14-Pin header
 - CE-compliant PCB and external power supply
 - Desktop standalone operation
- Software Features
 - Supports Win 98 or Win2000
 - Evaluation suite of VisualDSP++: compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface.
VisualDSP++ limited to use with EZ-KIT Lite hardware.
- Part # ADDS-21532-EZLITE

ADSP-2191 EZ-KIT Lite™

■ Hardware Features

- Single ADSP-2191
- AD1885 48 kHz AC'97 SoundMAX® codec
- AD1803 low power modem codec
- AD3338 and AD3339 voltage regulators
- 4 Mbits of flash memory
- Jumper selectable line-in or mic-In 1/8" stereo jack and line-out 1/8" stereo jack
- USB version 1.1-compliant interface
- 14-pin emulator connector for JTAG interface

■ Software Features

- Support for Win98 and Win2000
- Evaluation suite of VisualDSP++: compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface. VisualDSP++ limited to use with EZ-KIT Lite hardware.

■ Part # ADDS-2191-EZLITE

ADSP-21990 EZ-KIT Lite

■ Hardware Features

- ADSP-21990 DSP
- 64K x 16-bit static RAM
- 4 Mbits of flash memory
- Analog input circuitry
- Two 4-channel 12-bit DACs (AD5327) on SPI Interface
- Encoder interface circuitry
- UART interface (RS-232)
- External CAN controller IC on SPI interface
- USB version 1.1-compliant interface
- 14-Pin emulator connector for JTAG interface

■ Software

- Support for Win98 and Win2000
- Evaluation suite of VisualDSP++: compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface.
VisualDSP++ limited to use with EZ-KIT Lite hardware.

■ Part# ADDS-21990-EZLITE

ADSP-TS101S EZ-KIT Lite™

- **Hardware Features**
 - Dual ADSP-TS101S DSP
 - 90MHz oscillator and buffer logic
 - ST Microelectronics DSM2150F5V combination FLASH (512K x 8) and programmable logic
 - MT4LSDT464A (4M x 64) 32 MB Synchronous Dynamic RAM (SDRAM)
 - DIMM expandable up to 128 MB
 - Three 90-pin connectors for analyzing and interfacing with the expansion port
 - USB version 1.1-compliant interface
 - JTAG ICE 14-pin header
- **Software Features**
 - Support for Win98 or Win2000
 - Evaluation suite of VisualDSP++ : compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface.
VisualDSP++ limited to use with EZ-KIT Lite hardware.
- Part# ADDS-TS101S-EZLITE

ADSP-21161N EZ-KIT Lite

■ Hardware Features

- ADSP-21161N SHARC DSP
- 48 Mbits of SDRAM
- AD1836 96 kHz audio codec
- AD1852 96 kHz auxiliary DAC
- 4 Mbits of flash memory
- USB version 1.1-compliant interface
- 14-pin emulator connector for JTAG interface

■ Software Features

- Support for Win98 or Win2000
- Evaluation suite of VisualDSP++: compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface. VisualDSP++ limited to use with EZ-KIT Lite hardware.

■ Part # ADDS-21161N-EZLITE

ADSP-21160M/N EZ-KIT Lite

■ Hardware Features

- ADSP-21160 DSP
- AD1881A SoundMAX audio codec
- USB debug interface with host PC
- 128K x 64-bits SBSRAM
- 512K x 8-bit flash memory
- JTAG ICE 14-pin header
- Two link port connectors

■ Software Features

- Support for Win98 or Win2000
- Evaluation suite of VisualDSP++ : compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface.
VisualDSP++ limited to use with EZ-KIT Lite hardware.

■ Part # ADDS-21160-EZLITE

- Part # ADDS-21160N-EZLITE, Available Fall 2002 for \$495

ADSP-21065L EZ-KIT Lite

- **Hardware Features**
 - ADSP-21065L SHARC DSP running at 60MHz
 - Full Duplex, 16-Bit audio codec
 - RS-232 interface with UART
 - JTAG emulation connector
 - EMAFE connector
 - SDRAM
 - Socketed EPROM
- **Software Features**
 - Support for Win9x, Win2000 and WinNT
 - Evaluation suite of VisualDSP++ : compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface. VisualDSP++ limited to use with EZ-KIT Lite hardware
 - Demonstrations: Fast Fourier Transform (FFT), Discrete Fourier Transform (DFT), Band Pass Filter, Pluck String Themes, Talk Through13
- **Part# ADDS-21065L-EZLITE**

ADSP-21061 EZ-KIT Lite

■ Hardware Features

- ADSP-21061 40 MHz SHARC DSP
- RS-232 interface with UART
- AD1847 SoundPort® 16-bit, full-duplex audio codec
- Line in and line out with stereo jacks
- MIC In (battery powered) with stereo jack
- Socketed EPROM, 128K x 8 (27C010) firmware includes a power-on self-test with audio report and an RS-232 based boot-strap loader
- Emulation header
- Power LED and 4 flag LEDs

■ Software Features

- Support for Win9x, Win2000 and WinNT
- Evaluation suite of VisualDSP++ : compiler, assembler, linker, prom splitter (loader), VisualDSP++ debugger interface.
VisualDSP++ limited to use with EZ-KIT Lite hardware

■ Part# ADDS-21061-EZLITE

ADSP-2189M EZ-KIT Lite

- Hardware Features
 - ADSP-2189M 75 MIPS processor
 - DSP-programmable CODEC gain
 - RS-232 interface port, and one PF/I/O
 - ADSP-218x EZ-ICE emulator port connector
 - Expansion connector includes all signal I/O plus 2.5 V, 3.3 V, and GND connections LED indicators for master power
 - CE certified
- Software Features
 - Windows 98 and Windows 2000
 - Evaluation suite of VisualDSP++: compiler, assembler, linker, prom splitter (loader), VisualDSP debugger interface, application size limited to 8k, VisualDSP++ limited to use with EZ-KIT Lite hardware
 - Application Examples: DTMF Generator, Echo Cancellation, FFT, etc. (similar to 2181 EZ-KIT Lite) Email Support
- Part # ADDS-2189M-EZLITE

ADSP-2181 EZ-KIT Lite™

- **Hardware Features**
 - ADSP-2181, 33 MIPS DSP
 - AD1847 stereo codec
 - RS-232 interface
 - Socketed EPROM
 - User push buttons
 - Power supply regulation
 - Expansion connectors
 - User configurable jumper
- **Software Features**
 - Windows 98 and Windows 2000
 - Evaluation suite of VisualDSP++: compiler, assembler, linker, prom splitter (loader), VisualDSP debugger interface, application size limited to 8K, VisualDSP++ limited to use with EZ-KIT Lite hardware
- **Part #: ADDS-2181-EZLITE**

DSP Tools Resources

- A complete DSP Tools Selection guide is found on the ADIDSP Tools Web site at:
www.analog.com/dsp/tools/selection.html
- DSP Connection: Yearly “mag-a-log” that contains information on all the DSP Tools Products, application notes, contact information, interviews with top DSP professionals in the industry, and third party information.
- For technical support please contact:
DSPtools.support@analog.com
- VisualDSP++ Demo available on the ADI DSP Tools Web site at:
http://www.analog.com/industry/dsp/tools/v_dsp_tutorial.html.
- For a free VisualDSP++ Test Drive please contact your local ADI Sales or Distributor or email DSPtools@analog.com with your complete mailing information and which ADI DSP architecture you would like to take your test drive with.

ADI Third Party Network: The DSP Collaborative™

- The DSP Collaborative is ADI's Third Party Network
 - Over 180 partners
 - Goal: Shorten customer time to market
 - Over 600 Products for ADI DSP Solutions
 - Algorithms
 - Real-time operating systems
 - Debuggers
 - MATLAB® DSP support
 - Focused Applications
 - Audio/Video
 - Cameras
 - Industrial inspection and control
 - Medical instrumentation/Imaging
 - Military/Aerospace
 - <http://www.analog.com/dsp/3rdparty>
- Emulators
Hardware development boards
Graphical S/W programs
Consulting services
- Motor/Motion Control
Radar/Sonar
Telecom/Telephony
Sound processing
Speech processing

Why the DSP Collaborative?

- To help shorten customer time to market through Third Party Products and Consulting Services
 - Real-time operating systems/Kernels
 - Algorithms
 - Development and evaluation hardware
 - Application specific products and services
- To drive the creation of value-added resources for customers
 - Reference designs
 - Turnkey solutions
 - System expertise
 - Applications knowledge and support
- To Help Customers Easily Identify Third Party Products and Services
- To learn more: <http://www.analog.com/dsp/3rdparty>

Analog Devices, Inc. (ADI) SPA Technology Centre

SPA DSP Software Products “New Products Guide”

ADI SPA Technology Centre

- Digital Signal Processing (DSP) Software for Voice Over Network (VON), TRAU, Telecommunications and Multimedia Applications.
 - Software development
 - Systems engineering
 - Applications engineering
 - Sales and marketing
 - Customer support

SPA DSP Software Algorithms

- ADSP-218x and ADSP-219x Code Modules
 - Speech coders
 - Echo cancellation
 - VON function blocks
 - Telephony
 - Fax and data modem pumps
 - Voice/fax/data relay
 - TRAU
- Echo Cancellation
 - G.168 – 2000 (line echo cancellation:
4 ms – 64 ms, sparse 128 ms)
 - G.165 (line echo cancellation)
 - AEC – variable span (acoustic echo cancellation)

- AEC – acoustic echo cancellation

SPA DSP Software Code Modules

■ Speech Coders (Speech Compression)

- G.723.1/A (5.3/6.3 kbit/s)
- G.729/A/B/AB (8 kbit/s)
- G.728 (16 kbit/s)
- G.722 (64/56/48 kbit/s)
- G.711/ II (64/56/48 kbit/s)
- G.726/G.727 (40/32/24/16 kbit/s)
- Auxiliary:
 - ◆ VAD (Voice Activity Detector)
 - ◆ CNG (Comfort Noise Generator)

SPA DSP Software Code Modules

- Telephony
 - Voice/fax/data relay
 - Voice Activity Detection (VAD)
 - Comfort Noise Generation (CNG)
 - DTMF encoder/decoder
 - Tone detection/generation
 - Ring detection
 - Caller ID
 - Call progress
 - E and M signaling
 - Forward Error Correction (FEC)
- VoN Function Blocks
 - Jitter Buffer (JIB)
 - RTP/RTCP
 - UDP/IP

SPA DSP Software Code Modules

■ Data Modem Pumps

- V.33 (14,400 bps 4-wire)
- V.32bis (14,400 bps)
- V.32 (9,600 bps)
- V.29 (9,600 bps 4-wire)
- V.27ter (4,800 bps 4-wire)
- V.22bis (2,400 bps)
- V.22 (1,200 bps)
- V.23 (1,200/75 bps)
- Bell212A (1,200 bps)
- Bell103 (300 bps)
- V.21 (300 bps)

■ Facsimile Modems

- V.17 (14,400 bps)
- V.33 (14,400 bps)
- V.29 (9,600 bps)
- V.27ter (4,800 bps)
- V.21 (300 bps)

$6M = \text{Program Memory (32-Bit)}$
 $DM = \text{Data Memory (16-Bit)}$
 $6M+DM+ = \text{Memory for extra channels}$

SPA Software Features

- Compliant to International Standards (ITU, etc)
- Extensively Tested
- Efficient Implementations (Optimized MIPS and Memory)
- Multichannel (Multiple Instance) Capable (High Channel Density)
- Used by Numerous Companies Worldwide (Proven Interoperability)
- Common API (Memory Mapped Interface)
- Detailed Developer's Guides
- Excellent Technical Support by Engineers
- Supplied As Integrated Solutions or Individual Modules
- On-Going Development (New DSPs (ADSP-219x, Blackfin) and Tools (Visual DSP++ Ver 2.0)

MIPS and Memory Summary

Vocoders	Description	Peak MIPS	Average MIPS	PM (words)	DM (words)	PM+ (words)	DM+ (words)
G.723.1	5.3 kbit/s	18.4	16.9	9558	11679	0	951
G.723.1	6.3 kbit/s	18.9	17.6	9558	11679	0	951
G.723.1A	5.3 kbit/s + VAD/CNG	18.6	17	9558	11679	0	951
G.723.1A	6.3 kbit/s + VAD/CNG	19.1	17.6	9558	11679	0	951
G.729	8 kbit/s	19.9	18.9	8844	4634	0	1432
G.729A	8 kbit/s (low MIPS)	10.8	10.4	7932	4677	0	1532
G.729B	8 kbit/s + VAD/CNG	20.1	19.3	12064	5405	0	1603
G.729AB	8 kbit/s (low MIPS AD/CNG)	12.9	11.6	11965	6426	0	1821
G.728	16 kbit/s	29	27	7947	2272	930	1743
G.726	40/32/24/16 kbit/s	8.5	8	1466	240	47	100
G.727	40/32/24/16 kbit/s	9.9	N/A	1262	252	N/A	N/A
G.722	64/56/48 kbit/s	12.9	N/A	1458	217	N/A	N/A
G.711	64 kbit/s	0.5	0.4	111	6	0	0

PM = Program Memory (24-Bit), DM = Data Memory (16-Bit), PM+/DM+ = Memory per extra channel

MIPS and Memory Summary

Echo Cancellation	Description	Peak MIPS	Average MIPS	PM (Words)	DM (Words)	PM+ (Words)	DM+ (Words)
G.165/G.168	16 ms, ECD On	6.7/7.03	N/A	1100/1211	354/412	276	340
G.165/G.168	16 ms, ECD Off	4.5/4.97	N/A	1100/1211	354/412	276	340
G.165/G.168	32 ms, ECD On	9.2/N/A	N/A	1100/1211	354/412	276	340
G.165/G.168	32 ms, ECD Off	7.1/8.57	N/A	1100/1211	354/412	276	340
AEC 64 ms span	Acoustic Echo Canceller	5.2	N/A	3153	3059	N/A	N/A
AEC 128 ms span	Acoustic Echo Canceller	7.2	N/A	3153	3059	N/A	N/A
AEC 256 ms span	Acoustic Echo Canceller	11.2	N/A	3153	3059	N/A	N/A
AEC 384 ms span	Acoustic Echo Canceller	15.2	N/A	3153	3059	N/A	N/A
Telephony							
DTMF	Encoder	0.5	N/A	68	78	2	0
DTMF	Decoder	1	N/A	1300	320	0	256

PM = Program Memory (24-Bit), DM = Data Memory (16-Bit), PM+/DM+ = Memory per extra channel

$BW = \text{Bandwidth (Hz)}$ $DW = \text{Data Width (bits)}$ $BW \times DW = \text{Data Rate (bits/sec)}$

ADI DSP Channel Capacity Examples

	2181-80	2188-80	2191-160	MOD980-640	MR4-1400
	(16k/16k)	(48k/56k)	(32k/32k)	(8 x 2188)	(4 x 219x)
DTMF (det)	63	80	124	640	854
G.168 (16 ms)	16	16	32	128	256
G.729AB	6	6	12	48	100
G.723.1A	4	4	8	24	64
VoN (G.711)	6	6	13	48	104
VoN (G.729AB)	3	3	6	24	56
VoN (G.723.1A)	2	2	5	16	44

SPA Code Module Applications Include:

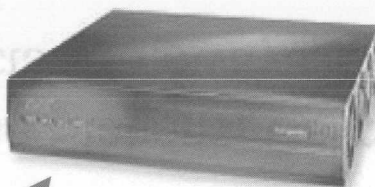
- VoN (VoIP, VoDSL, VoATM, VoCABLE, etc.)
- FoN (FoIP, etc)
- H.32x (H.324, H.323, H.320, etc)
- Internet Telephony
- Audioconferencing, Videophones, Feature Phones
- Digital Voice Storage
- Wireless, Mobile
- TRAU, Transcoders, Base Stations, Cellphones, MS, BSC, MSC
- Server and Client Products (Gateways, CO, CPE, IAD, SOHO, etc.)
- Pair Gain, DCME
- RAS, DSVD
- ISDN, ATM, Frame Relay
- Satellite, Microwave, Rural Radio Networks

Typical Product Applications



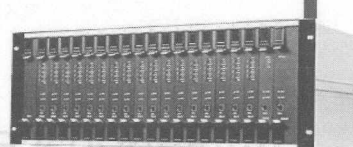
WIRELESS
SYSTEM
TRAU

MEDIA GATEWAY
VoDSL GATEWAY



HIGH PORT COUNT
(INFRASTRUCTURE)

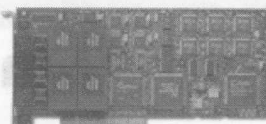
REMOTE ACCESS
CONCENTRATOR OR DSLAM



ADI / SPA
VoN SOLUTIONS

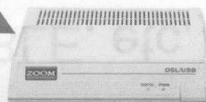


IP PBX, MTU, or
ENTERPRISE GATEWAY



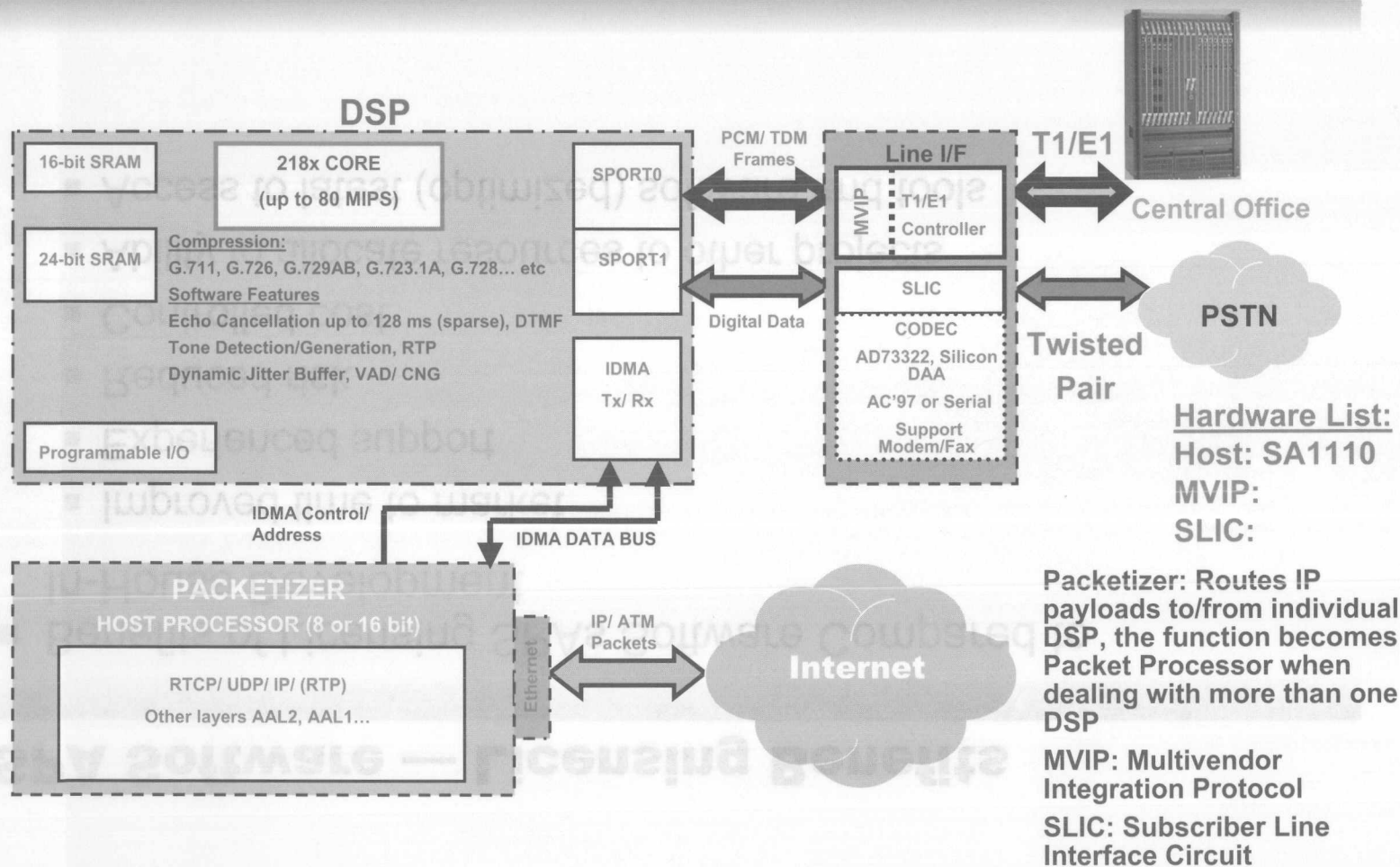
IP TELEPHONY CARD

VOICE/DATA
(SOHO/RESIDENTIAL)



LOW PORT COUNT
(PREMISES)

Typical VoIP System Layout



SPA Software — Licensing Benefits

- Benefits of Licensing SPAs Software Compared to In-House Development
 - Improved time to market
 - Experienced support
 - Reduced risk
 - Controlled cost
 - Ability to allocate resources to other projects
 - Access to latest (optimized) software and tools

- Flexible pricing and licensing arrangements

SPA Software Design-in Cycle

- Preliminary Information
 - Web site, email, phone, fax
 - Product summary sheets, specification sheets, technical support
- Demonstration Software
 - Executable file for EZ-Kit Development boards
 - Application Note
- Evaluation Software
 - Time-Out Library file (re-settable)
 - Developer's Guide (comprehensive)
 - Source host file (example)
 - Common API (simplifies code integration)
 - Architecture file (Ver 6.1) (Ver 2.0, VDSP++)
 - Plus all other files and documentation required for linking our software into customer application

SPA Software Design-in Cycle

- Production Object Code
 - Evaluation Software with time-out removed
 - One-time NRE
 - Unlimited channels for product application
- Production Source Code
 - Algorithm source code plus object code package
 - One time NRE
 - Unlimited channels for product application
- Licensing Agreements
 - NDA/MOU for demonstration and evaluation
 - SLA for production code (object or source)
 - Maintenance program available
 - Flexible pricing and licensing arrangements



www.analog.com

11-105

- DVD MPEG, HDCD
- THXselect, THXUltra, THXselect EX
- MPEG 1 layer 3 (MP3)
- MPEG 2 audio layers 1 and 2, AAC
- DTS-ES extended surround, DTS Neo: 6
- Dolby Digital, ProLogic, ProLogic II, Dolby Headphone
- Auto-Detect
- Dynamic Decoder and Post-Processor Platform with
csl audio
- For use in home theater systems, and high end
Encoder, Decoder, and Post-Processor Reference Designs
- Industry First 32-Bit Floating Point, Multichannel Audio

Multi-Channel Audio Processor



www.analog.com

11-105

Melody Floating-Point Audio Solution

- Industry First 32-Bit Floating Point, Multichannel Audio Encoder, Decoder, and Post-Processor Reference Designs
 - For use in home theater systems, and high end car audio
- Dynamic Decoder and Post-Processor Platform with Auto-Detect
 - Dolby Digital, Prologic, Pro-Logic II, Dolby headphone
 - DTS-ES extended surround, DTS Neo: 6
 - MPEG 2 audio layers 1 and 2, AAC
 - MPEG 1 layer 3 (MP3)
 - THXSelect, THXUltra, THXSurround EX
 - WaveSurround and SRS 3D surround
 - DVD MLP, HDCD

Melody Fixed-Point Audio Solution

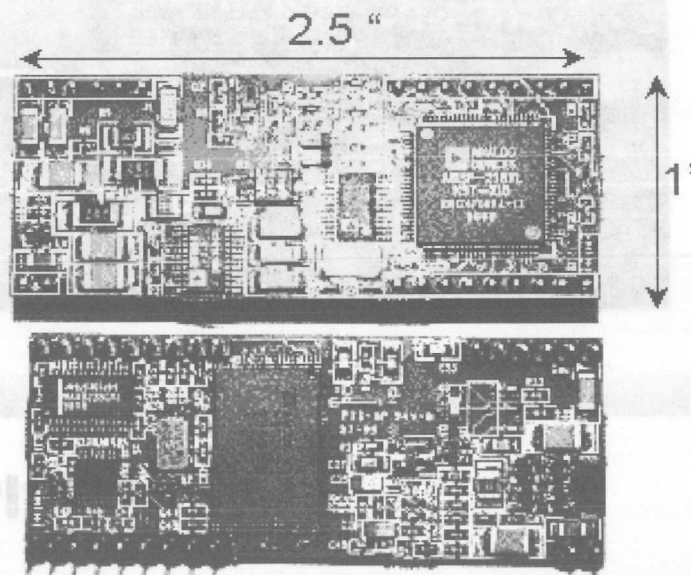
- High Quality Low Cost Audio Reference Designs
 - 16-bit fixed-point stereo audio encoder and decoder
- MPEG1 Layer 1, 2, and 3 Encoders and Decoders
 - Decoders support all bit rates (32 Kbps – 448 Kbps), all full and half sampling frequencies (16 kHz, 22.1 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz)
 - ◆ Software rate conversion eliminates external rate converters
 - ◆ Auto-detects and displays bit-stream information
 - Preset graphics equalizers: jazz, pop, rock, classical
- ADSST-MPEG-xxxx Chipset: ADSP-218x + Object Code
 - 10 K pricing: US \$12.00
- ADSST-MELODY-EVAL01 Available (US \$650)

Digital Audio Player Solution

- DAP1.0 — Turnkey Portable MP3 Player Reference Design
 - Supports all bit rates and sampling frequencies
 - Memory: 32 MB built-in flash plus 32 MB removable flash
 - Displays messages and song information on three-line LCD
 - Full operation controls (playback, volume, record)
 - Preset equalizer functions
 - Rock, jazz, pop, classical, and bass boost (5 dB)
 - Parallel port PC interface for MP3 file downloads
 - PC download manager software provided
 - Supports MP3 encoding of CD audio
 - Thirty minute memo recorder with built-in mic
 - Does not use up music storage memory

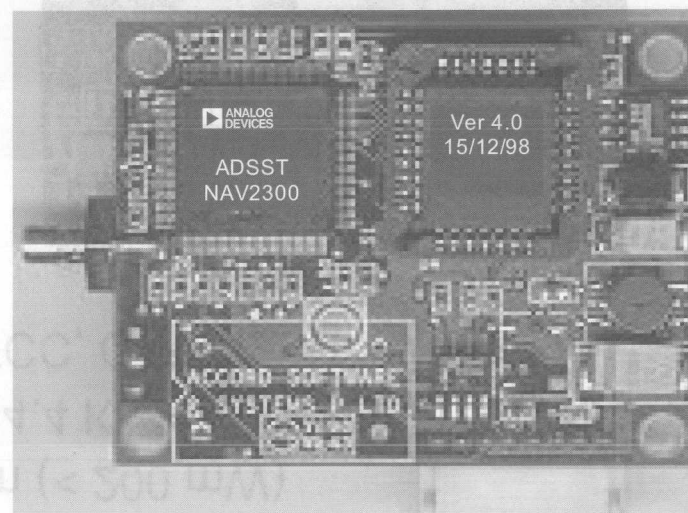
Embedded Modem Solution

- Integrated Standalone Modem Solution
 - Compact socket modem design (1" x 2.5" PCB)
 - Very low power consumption (< 200 mW)
 - Supports multiple speeds (14.4 Kbps to 56 Kbps)
 - Tested in many countries (FCC, CTR21, ...)
- ADSST-VxxATS Chipset
(Complete AT Modem)
 - ADSP218x + AD1803/04
+ object code
 - 10 K pricing: US \$22.00



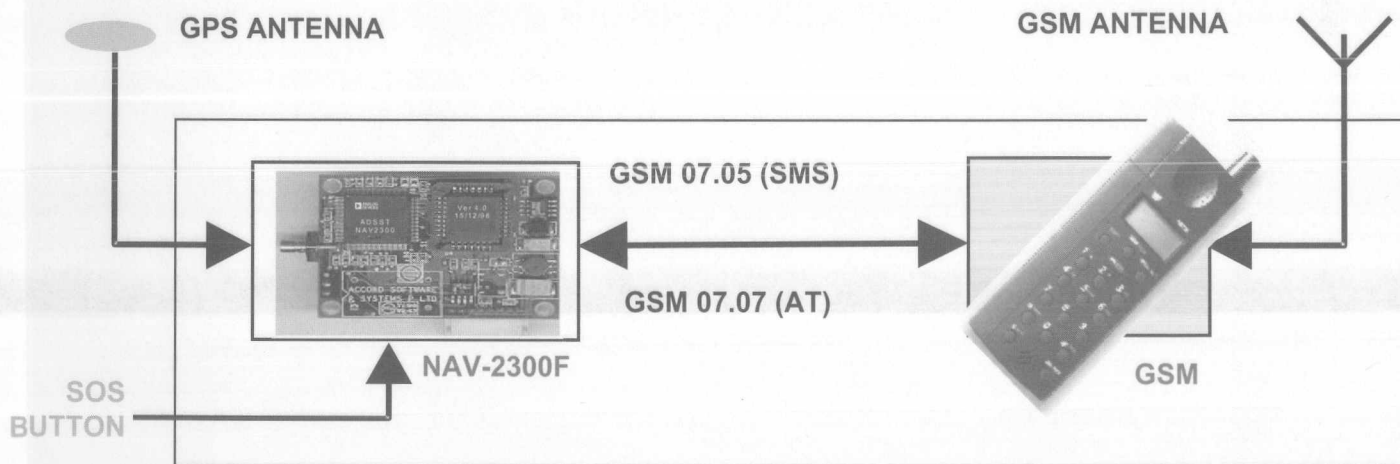
NAV 2K GPS Receiver Solution

- ADSST-NAV-2300 Chipset
(40 mm x 50 mm)
 - ADSP-2189M+GPS
object code
 - 10 K pricing: US \$16.50
- ADSST-NAV-2300-SDK
Available (US \$350)



NAV 2K GPS Receiver Solution

- ADSST-NAV-2300F Chipset
 - GSM-SMS and GSM-AT interface to GSM handsets
 - Allows configuration and transmission of position information
 - Used for fleet management, security, tracking...
 - ADSP2189M + GPS object code (with GSM Interface)
 - 10 K pricing: US \$18.50
- ADSST-NAV-2300F SDK Available (US \$1250)



1988

1990

2000

2004

2005

2009+

Mixed-Signal DSP Strategy

High Performance
DSP Cores

High Performance
Analog

State-of-the-Art
Development Tools

Mixed-Signal DSP

Motor
Control

Power
Systems
Control

Optical
Networking

Office
Automation

Industrial
Mass
Market

Data
Acquisition
Systems

Intelligent
Sensors

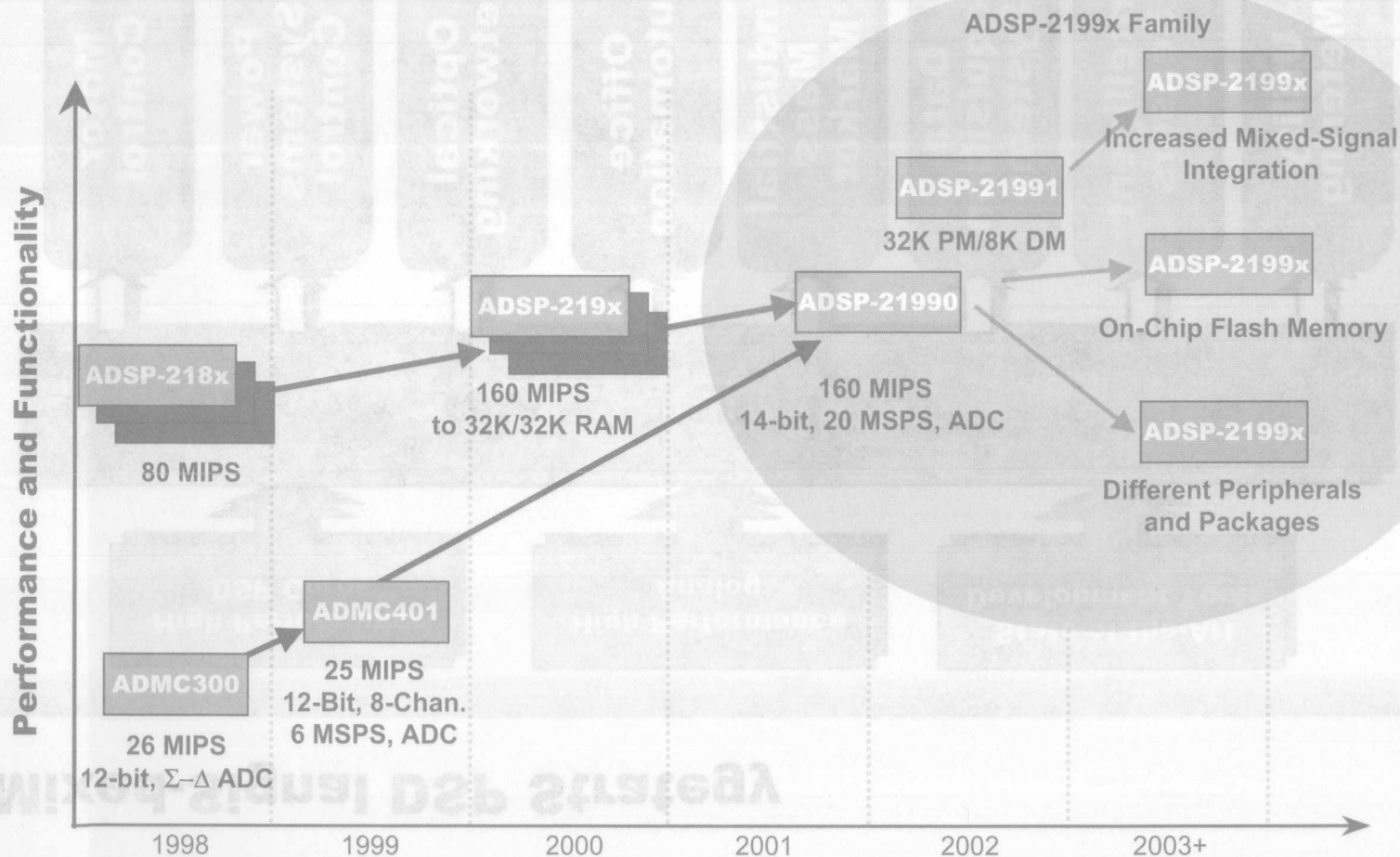
Utility
Metering

Embedded Control Applications

Embedded
Signal Processing Applications

ADSP-2199x Total Product Roadmap

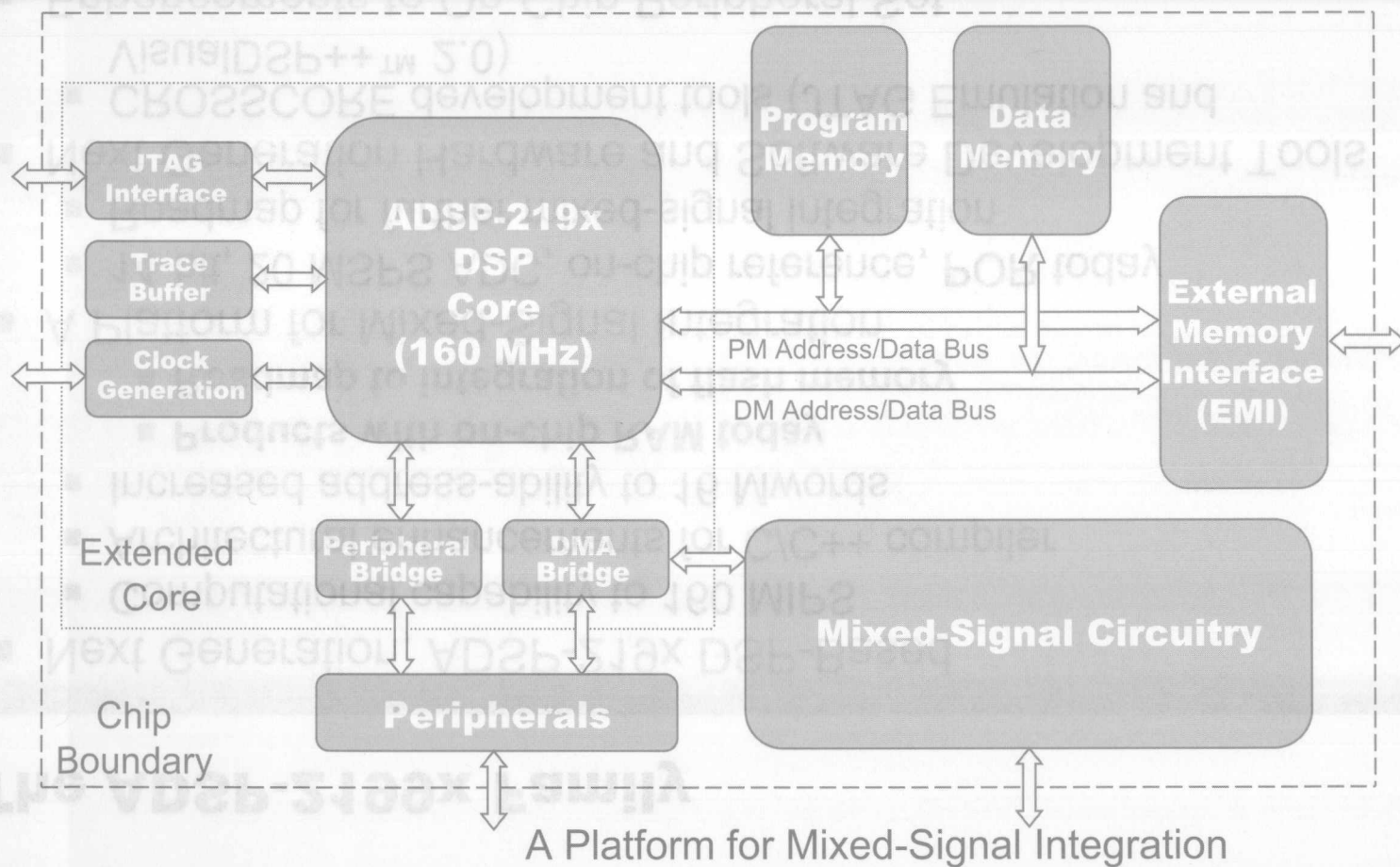
Meeting the Full Range of Customer Needs



The ADSP-2199x Family

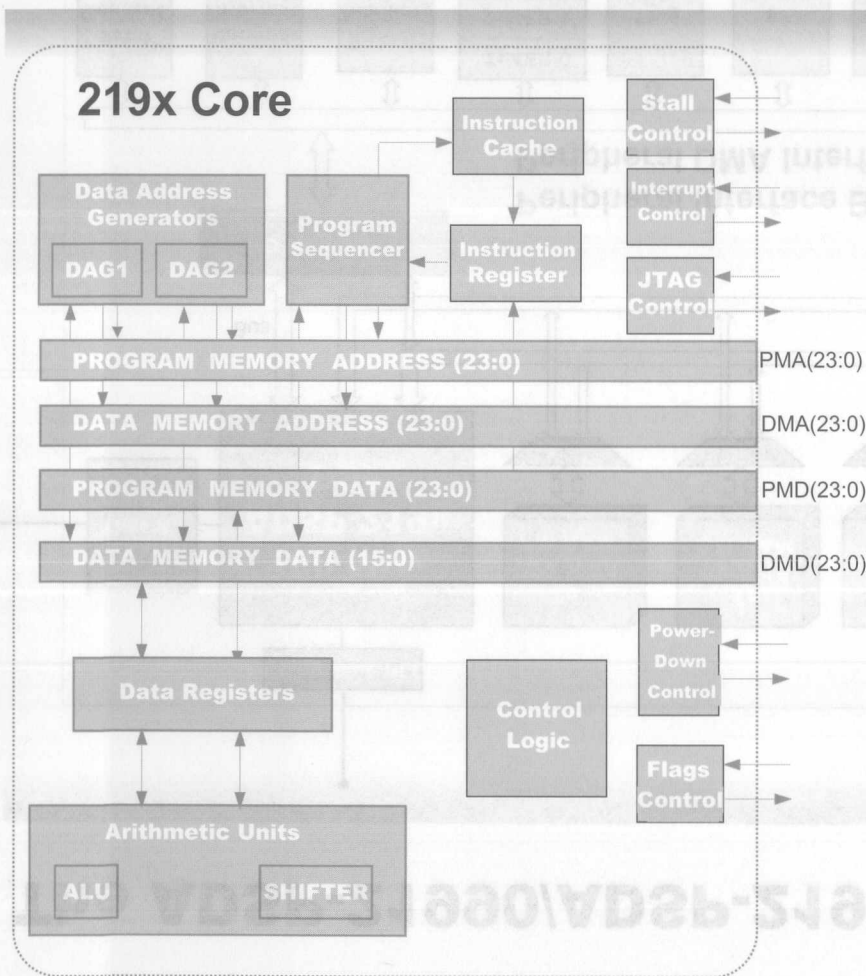
- Next Generation, ADSP-219x DSP-Based
 - Computational capability to 160 MIPS
 - Architectural enhancements for C/C++ compiler
 - Increased address-ability to 16 Mwords
 - Products with on-chip RAM today
 - Roadmap to integration of flash memory
- A Platform for Mixed-Signal Integration
 - 14-bit, 20 MSPS ADC, on-chip reference, POR today
 - Roadmap for further mixed-signal integration
- Next Generation Hardware and Software Development Tools
 - CROSSCORE development tools (JTAG Emulation and VisualDSP++™ 2.0)
- Enhancements to On-Chip Peripheral Set
 - Enhanced control peripherals today (PWM, EIU, SPI, etc.)
 - Roadmap to different application-specific peripherals (CAN, etc.)
- Based on 0.25 μm CMOS Technology

ADSP-2199x Family Architecture



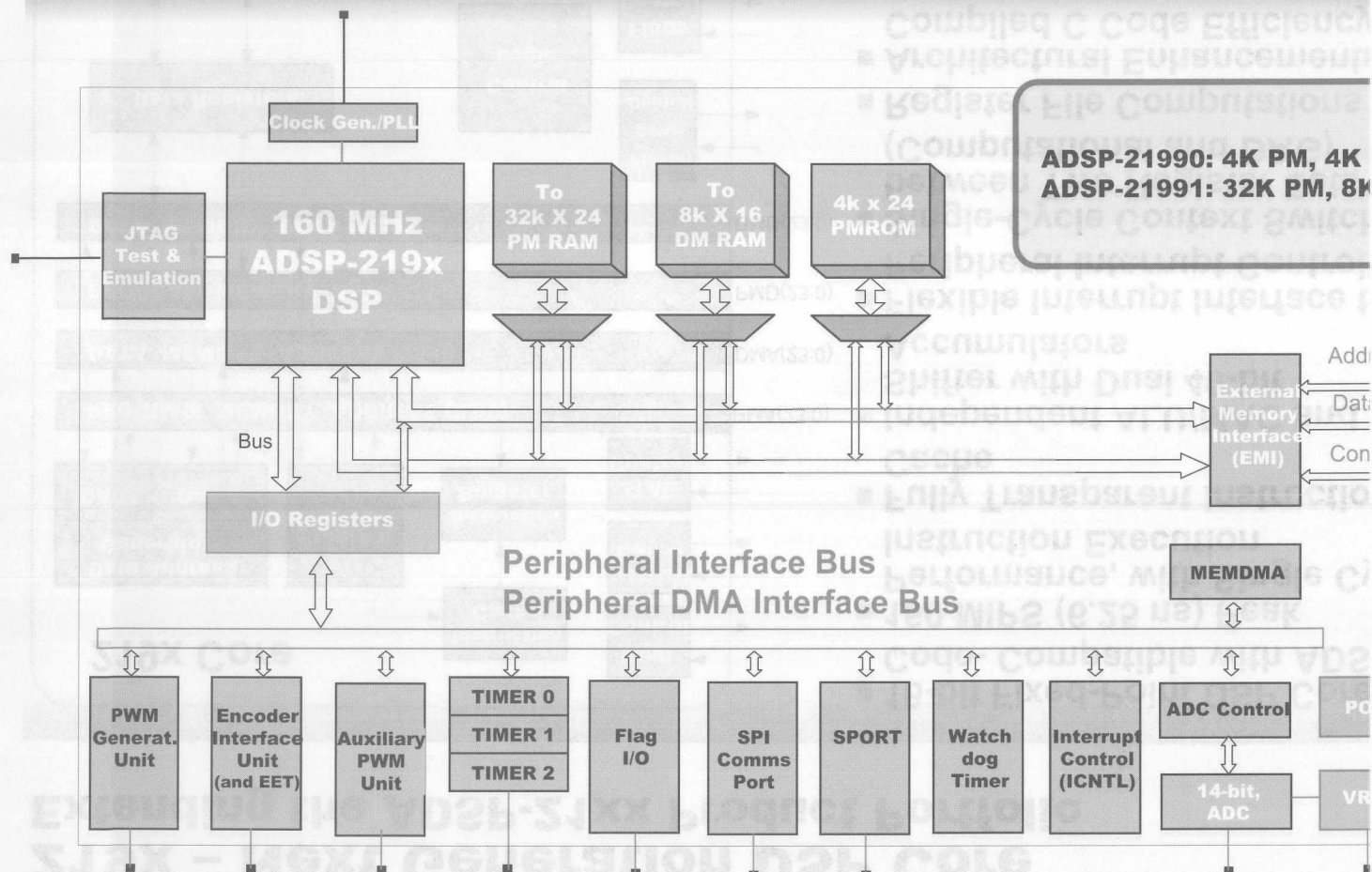
219x – Next Generation DSP Core

Extending the ADSP-21xx Product Portfolio



- 16-bit Fixed-Point DSP Core, Code- Compatible with ADSP-21xx
- 160 MIPS (6.25 ns) Peak Performance, with Single Cycle Instruction Execution
- Fully Transparent Instruction Cache
- Independent ALU/MAC and Barrel Shifter with Dual 40-bit Accumulators
- Flexible Interrupt Interface to Peripheral Interrupt Controller
- Single-Cycle Context Switch between Two Register Sets (Computational and DAG)
- Register File Computations
- Architectural Enhancements for Compiled C Code Efficiency
- Up to 16 MWord Addressability
- Flexible Power Management and Power-Down Control
- JTAG Tools Interface

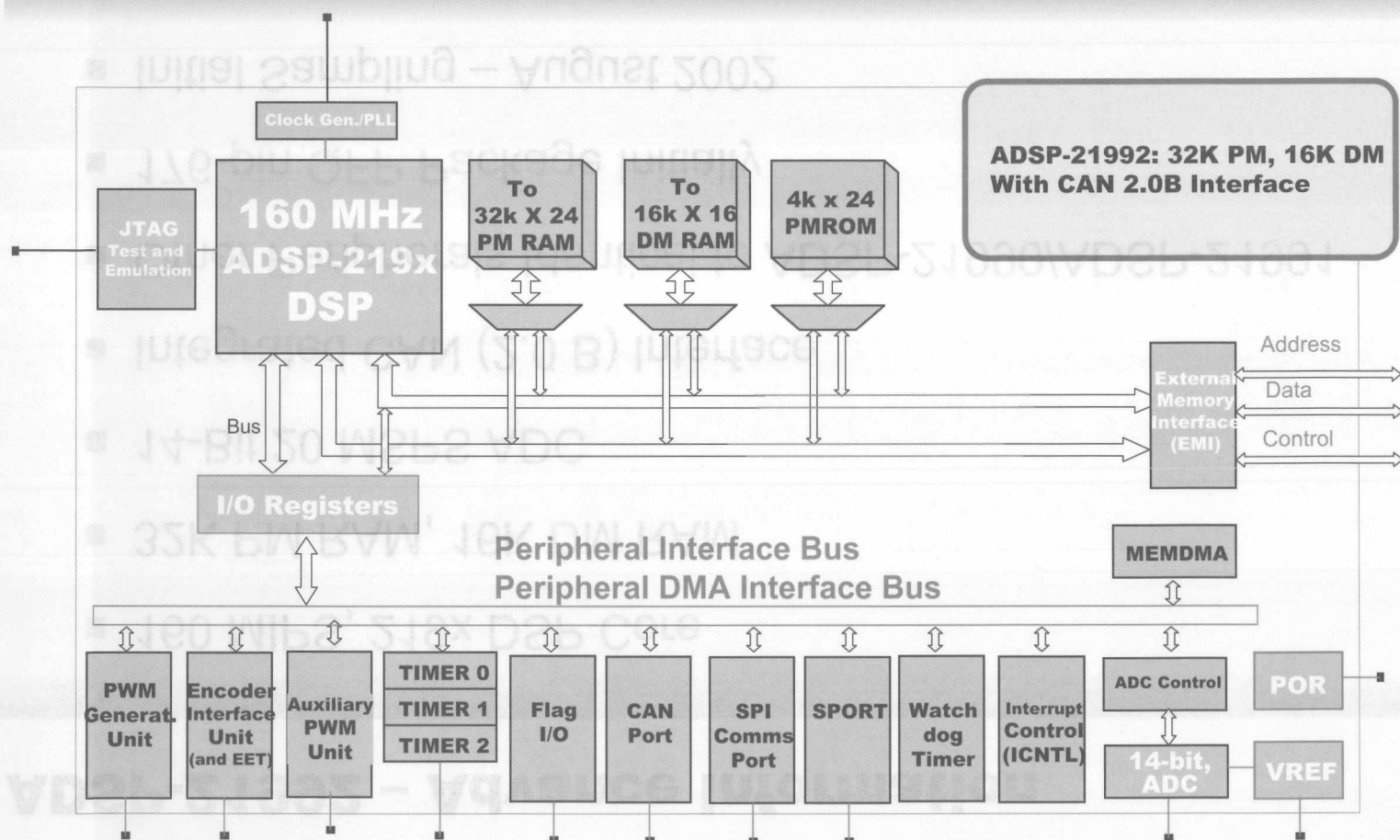
The ADSP-21990/ADSP-2199 Chip Architecture



ADSP-21992 – Advance Information

- 160 MIPS, 219x DSP Core
- 32K PM RAM, 16K DM RAM
- 14-Bit 20 MSPS ADC
- Integrated CAN (2.0 B) Interface
- Other Peripherals Identical to ADSP-21990/ADSP-21991
- 176-pin QFP Package Initially
- Initial Sampling – August 2002
- -40°C to $+125^{\circ}\text{C}$ Ambient Temperature

The ADSP-21992 – Advance Information

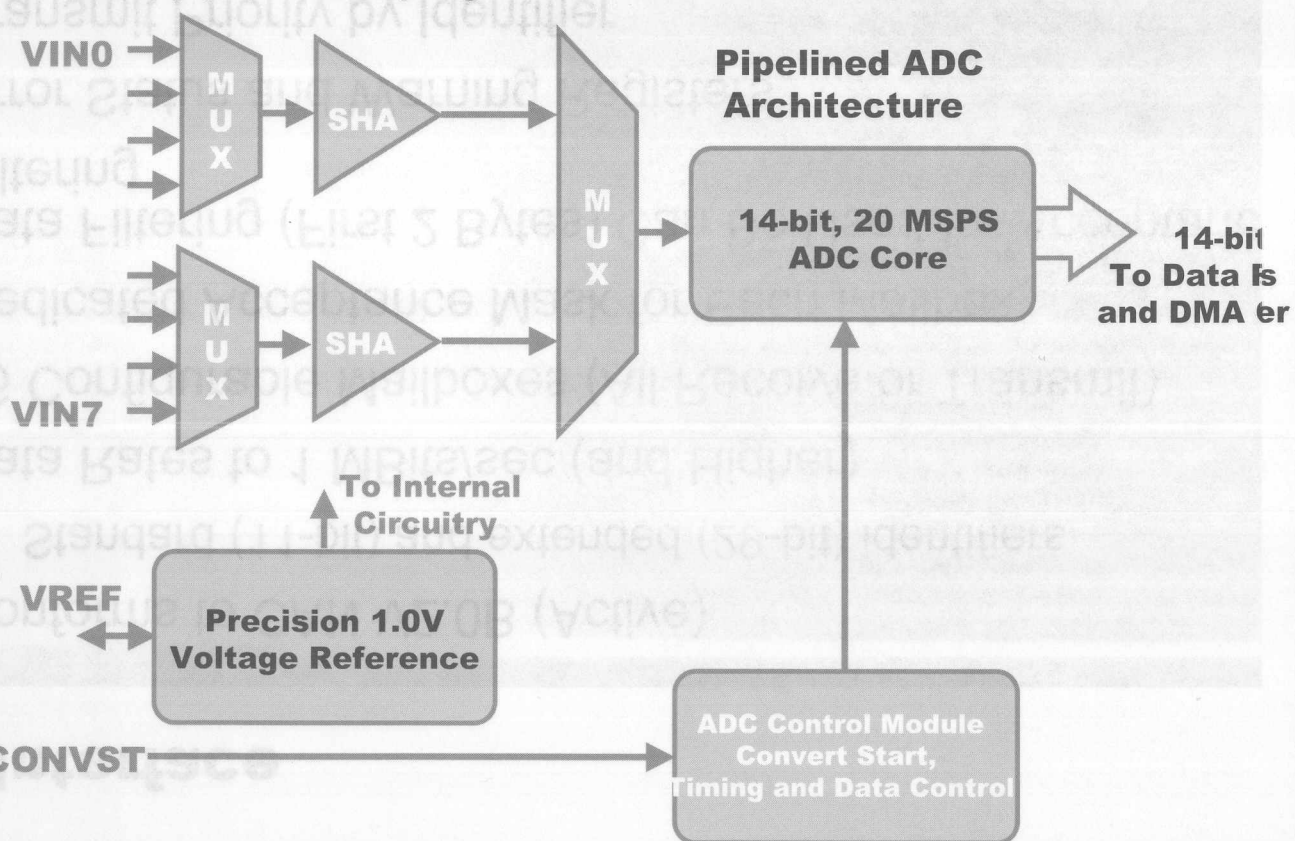


CAN Interface

- Conforms to CAN V2.0B (Active)
 - Standard (11-bit) and extended (29-bit) identifiers
- Data Rates to 1 MBits/sec (and Higher)
- 16 Configurable Mailboxes (All Receive or Transmit)
- Dedicated Acceptance Mask for Each Mailbox
- Data Filtering (First 2 Bytes) Can Be Used for Acceptance Filtering
- Error Status and Warning Registers
- Transmit Priority by Identifier
- Universal Counter Module
- Power-Down/Sleep Mode
- Readable Transmit and Receive Counters

ADSP-21990/91/92 ADC Architecture

- 8 Analog Inputs Simultaneous Sampling
- 2.0 V p-p

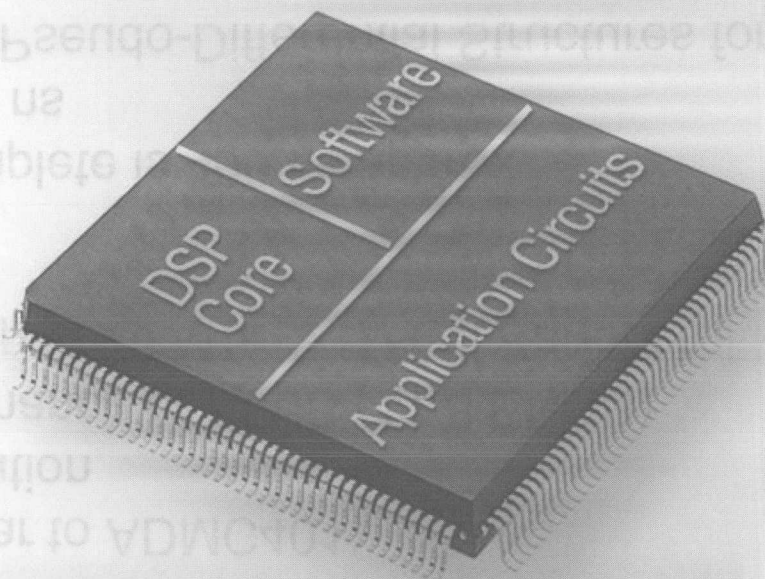


Pipeline ADC Architecture of ADSP-21990/91/92

- 14-bit Pipeline Architecture (Similar to ADMC401)
 - 14-bit data bus => 14-bit resolution
 - Typical Signal to Noise Performance of 71 dB (11.5 ENOB)
- Programmable ADC Clock Rate up to 20 MSPS (1/4 of Peripheral Clock)
- 6-Stage ADC Pipeline
 - Latency to first conversion complete is 400 ns approx.
 - 8 Channels converted in < 800 ns
- 2 V p-p Input Voltage Range with Pseudo-Differential Structures for Increased Noise Immunity
- Dual Sample and Hold Amplifiers (SHA) for Simultaneous Sampling
- Automatic DMA Data Transfer Capability from 1, 2, 4, or 8 Channels
- Variety of Programmable CONVST Sources
- Timed Latching of ADC Results Relative to CONVST
- Integrated Precision 1.0 V Voltage Reference

ADSP-21990/ADSP-2199 Control Peripherals

- Control Peripherals
 - 3-Phase PWM generation unit
 - ADC control module
 - 32-Bit encoder interface unit
 - Dual auxiliary PWM outputs
 - 16-bit watchdog timer
- General-Purpose Peripherals
 - Three, 32-bit general purpose timers
 - 16-bit digital IO Port (Flag IO)
 - Peripheral interrupt controller
- Serial Communications
 - SPORT
 - SPI
 - JTAG

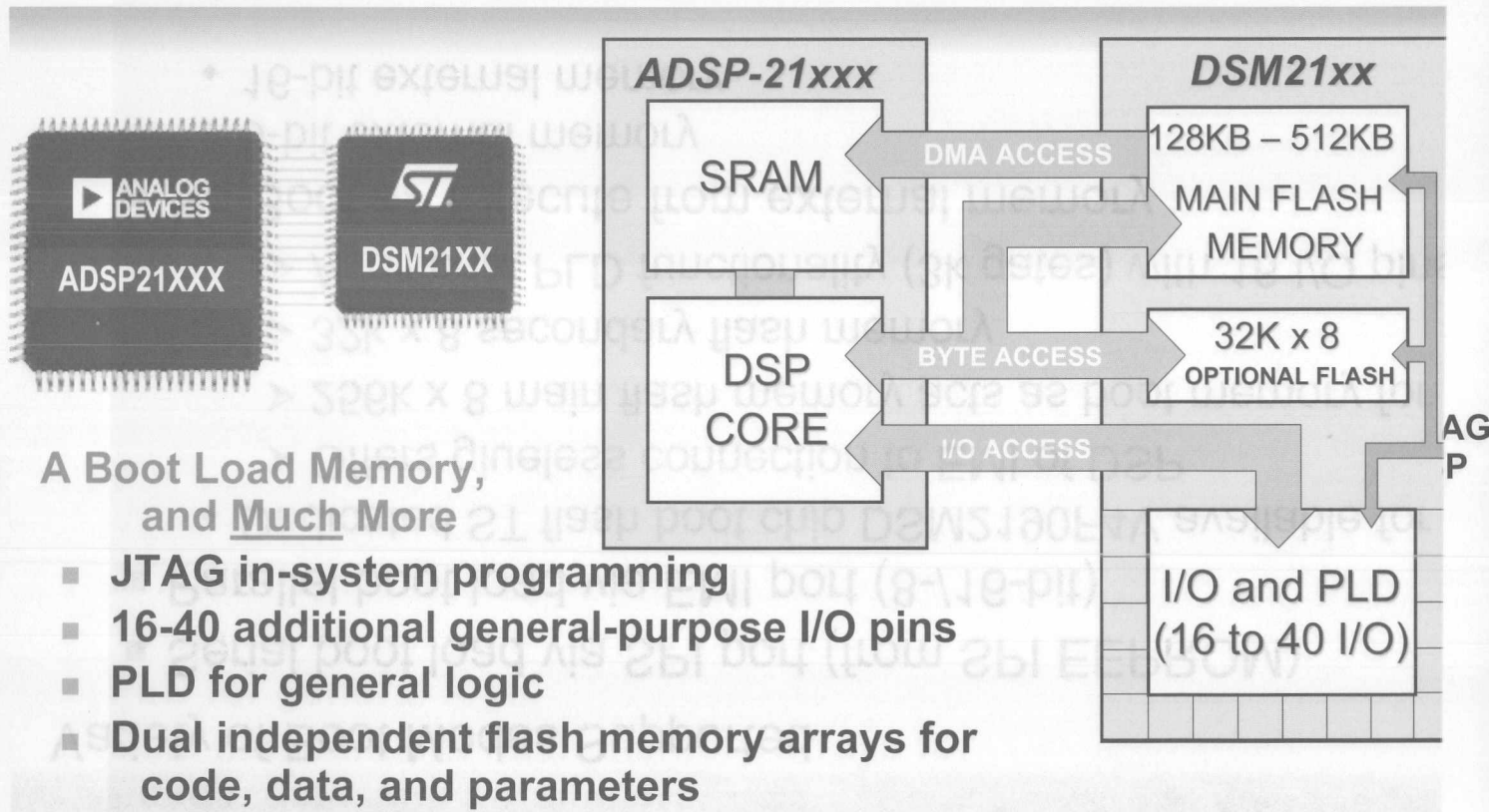


Boot Loading Options for ADSP-21990/ADSP-21991

Variety of Boot Modes Supported

- Serial boot load via SPI port (from SPI EEPROM)
- Parallel boot load via EMI port (8-/16-bit)
 - ◆ Dedicated ST flash boot chip DSM2190F4V available for 219x
 - Offers glueless connection to EMI of DSP
 - 256k x 8 main flash memory acts as boot memory for DSP
 - 32k x 8 secondary flash memory
 - Additional PLD functionality (3k gates) with 16 I/O pins
- No-Boot => Execute from external memory
 - ◆ 8-bit external memory
 - ◆ 16-bit external memory

DSP System Memory (DSM) from ST



■ A Boot Load Memory, and Much More

- JTAG in-system programming
- 16-40 additional general-purpose I/O pins
- PLD for general logic
- Dual independent flash memory arrays for code, data, and parameters
- Content security
- Low power operation
- Simple development software tools. . . download at no cost

ADSP-21990/91/92 Product Details

- 160 MIP 219X Core
- 14-Bit 8-Channel 20 MSPS ADC
 - Vref
 - Power on Reset
- Embedded Peripherals
 - 3-Phase PWM
 - Dual 16-Bit Auxiliary PWM
 - 32-Bit Encoder Interface
- Other Peripherals
 - 3 32-Bit Timers
 - 16-Bit Watchdog Timer
 - Programmable Interrupt Control
- 2.5 V Core 3.3 V I/O
- 196-Pin BGA or 176-Pin TQFR Packages

ADSP-21990/91/92 Product Details

- 16 Digital I/O
- Ports
 - 1 20 Mbaud SPI
 - 1 40 Mbaud SPORT
 - 1 CAN Interface (ADSP-21992 only)
- Memory
 - 4 K by 24-Bit (ADSP-21990)
 - 8 K by 24-Bit (ADSP-21991)
 - 16 K by 24-Bit (ADSP-21992)
- 1 M Word External Memory Interface
- -40° C to +85° C Temperature Range
 - -40° C to +125° C (ADSP-21992 only)

ADI Mixed-Signal DSP Web Site: <http://www.analog.com/DSP/Mixedsignal>



Home | Buy | Order Samples | Technical Support | myAnalog

ADI Site Navigation

ADI Home > Digital Signal Processing >

Mixed Signal DSPs

Mixed Signal DSPs

[Selection Guide](#)

[Architectural Overview](#)

[Benchmarks](#)

[Roadmap](#)

[Development Tools](#)

[Technical Library](#)

[Contact Mixed Signal DSP](#)

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Digital Signal Processing

Digital Signal Processing

ADI Design Resources

Product Selection...

Design Tools...

Technical Library...

Digital Signal Processing



Featured

Request a [FREE Mixed Signal VisualDSP++ Test Drive](#) and Register To Qualify For a Complete Mixed Signal DSP Development Tools Package.

Download New [Mixed Signal DSP Application Code Examples](#) for the ADSP-2199x Products.

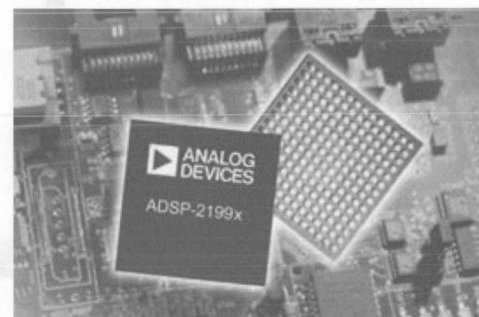
[ADSP-2199x EZ-KIT Lite™](#) Now Available.

Mixed Signal DSPs

The ADSP-2199x family of mixed-signal DSPs provides single-chip, high-performance solutions for embedded control and signal processing applications.

The ADSP-2199x family represents the highest-performance mixed-signal DSPs generally available today. These products combine the 160 MIPS, ADSP-219x DSP core with an 8-Channel, 14-bit, 20 MSPS analog to digital conversion system as well as the right mix of embedded control peripherals and comprehensive development tools. The various pin-for-pin compatible models provide different on-chip memory sizes and peripherals, allowing users to select the optimal memory and peripheral mix for a given application.

The ADSP-219x core architecture has also been optimized for high C/C++ compiler efficiency, resulting in increased code density and ease of use. All products are supported by CROSSCORE™, ADI's award-winning DSP development tools.





ANALOG DEVICES

11-130

Developers can use the ADSP-2199x to develop applications for a wide range of applications. The ADSP-2199x is a 32-bit DSP with a 100 MHz clock rate. It features a 100 MHz clock rate and a 100 MHz clock rate. The ADSP-2199x is a 32-bit DSP with a 100 MHz clock rate. It features a 100 MHz clock rate and a 100 MHz clock rate.

The ADSP-2199x is a 32-bit DSP with a 100 MHz clock rate. It features a 100 MHz clock rate and a 100 MHz clock rate. The ADSP-2199x is a 32-bit DSP with a 100 MHz clock rate. It features a 100 MHz clock rate and a 100 MHz clock rate.

ADSP-2199x Hardware and Software Development Tools

Mixed Signal DSPs

Digital Signal Processing

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Search

Find a Product

<http://www.analog.com/dsp/mixedsignal>
ADI Mixed-Signal DSP Web Site

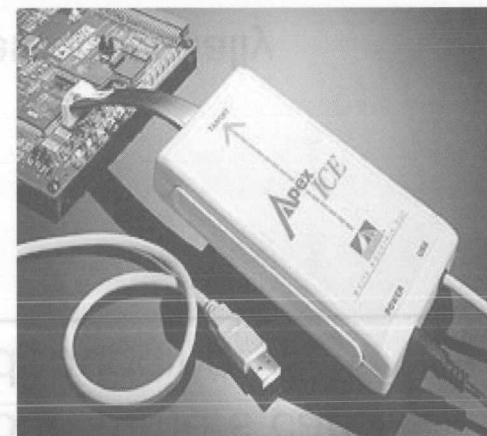


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11-130

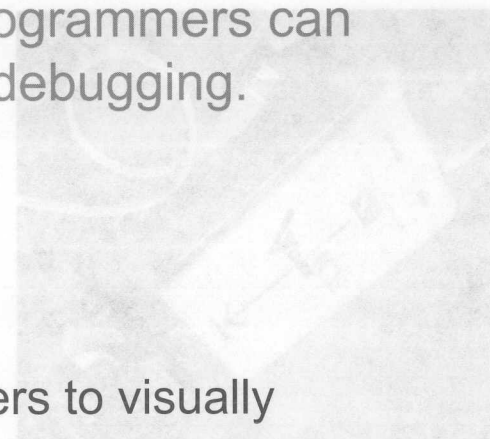
ADSP-2199x Family Development Tools

- Supported by ADI's Award-Winning CROSSCORE Development Tools
- VisualDSP++ 2.0 Integrated Development Environment
 - The VisualDSP++ Kernel (VDK)
 - C/C++ high level language compiler
 - Advanced plotting tools
 - Statistical profiling to easily identify programming bottlenecks
- JTAG In-Circuit Emulation (ICE) Capabilities
 - On-chip emulation and debug support
 - PCI emulation => Summit ICE
 - USB emulation => Apex-ICE
- EZ-KIT Lite for ADSP-2199x
 - Low cost evaluation platform for ADSP-2199x silicon
 - Expandable as development platform via JTAG emulator connector
 - ADSP-21990 EZ-KIT available



What is VisualDSP++

- VisualDSP++ is an integrated development environment that delivers efficient project management so programmers can move easily between editing, building, and debugging.
- Key Features Include:
 - The VisualDSP++ Kernel (VDK)
 - C++ compiler
 - Advanced plotting tools enabling programmers to visually measure software performance
 - Statistical profiling to easily identify programming bottlenecks
- VisualDSP++ offers programmers a powerful programming tool with flexibility that significantly decreases the time required to port software code to a DSP, reducing time to market



Features of VisualDSP++

- VisualDSP++ RTOS/Kernel/Scheduler (VDK)
- High Level Language Including C++
- Rich Debug Ability Including MP Support
- Advanced Profiling Features
- High Quality Visualization/Plot Capability
- Expandable with ActiveX™
- Easy to Test and Verify Applications with Tcl Scripts
- Easy to Learn with Online Help
- New Flexible Licensing Mechanism

Integrated Development and Debugging Environment (IDE)

The screenshot displays the Analog Devices VisualDSP++ IDE interface, titled "Analog Devices VisualDSP++ [Target: ADSP-219x Simulator] - [Project: EventDemo.dsp]". The interface is divided into several panes:

- Parameter Window:** Shows configuration parameters for the kernel and system, such as Clock Frequency (40 MHz), Tick Period (5 ms), History Buffer Size (256), and Max Running Threads (10).
- Source Code Editor:** Displays the C code for "Vdk_conf.h" and "Factory.cpp". The code includes semaphore definitions and thread management functions.
- Imaging Data Window:** Shows a 3D surface plot of imaging data with axes labeled "x", "y", and "z".
- State History Window:** Displays a timeline of thread execution, showing the state of Thread 2, Thread 1, Thread 0, and the Idle Thread over time.
- Thread Window:** Lists the current state of threads, including "Current Tick", "Idle Thread", "Thread 0", "Thread 1", "Thread 2", and "Thread 3".
- Console Window:** Shows the output of the program, including the "cd event_example" command and the "ls -las" command output.

The status bar at the bottom indicates the target is "Halted" at "Line 48, Col 20" with a value of "00000000".

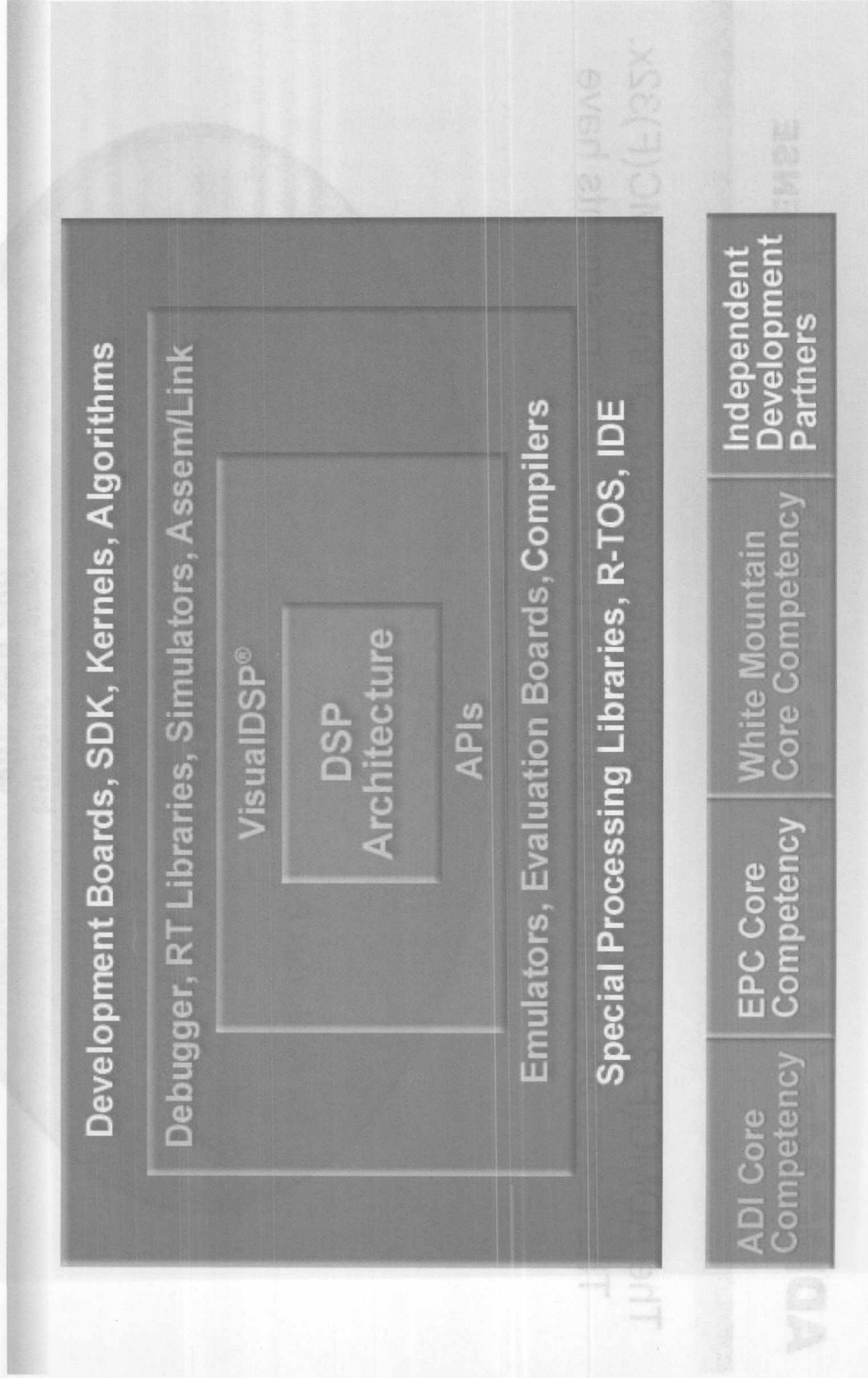
High Level Language Compilation

- C/C++ Support
 - High level languages (HLL) can shorten the customers time to market. HLLs are more common, allowing for a greater talent pool to take advantage of the real-time processing performance offered by DSPs.
 - “Don’t just do it, do it well!” ADI purchased Edinburgh Portable Compilers for their expertise in DSP compilation technology. They are intimately aware of the DSP architectures and the target applications, which leads to optimized C and C++ compilers.
 - ADI’s C++ is based on superset of Embedded C++ standard that adds the code reuse aspect of C++ without bloating the complied code.
 - Object-oriented programming shortens time to market.

Statistical Profiling

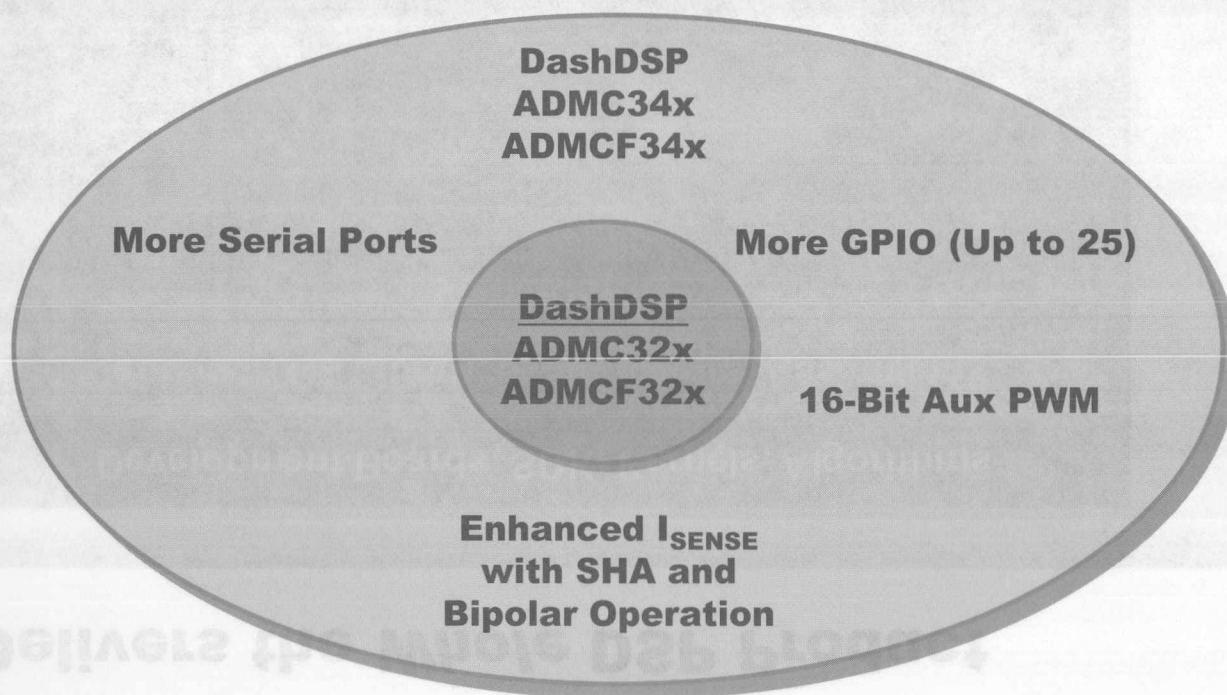
- **Non-Intrusive Statistical Profiling** (Patent Pending)
 - Does not halt the DSP
 - No extra code added to the application
- The Debugger has the ability to randomly sample the target processors PC and then present the user with a graphical display of the resultant samples. This will let the user easily see where their application is spending most of its time. Since the JTAG sampling is completely non-intrusive, this process will not incur any additional run-time overhead.
- Allows developer to passively gather important metrics without interrupting the real-time characteristics
- Programmer can focus on those areas in the program that impact performance and take corrective action

ADI Delivers the *Whole* DSP Product



ADMC34x / ADMCF34x: DashDSP with I_{SENSE}

The ADCM(F)34x family is an enhanced version of the ADCM(F)32x. The cores are similar, but numerous product enhancements have been made.



ADMC(F)34x Product Enhancements

- The ADCMC(F)32x ADC System Has Been Augmented:
 - Addition of sample-and-hold circuits for timed sampling
 - Up to three bipolar current sense amplifiers
 - Over-current protection on bipolar limits
 - Flexibility for operation from single dc link shunt or three low-side shunts
 - Filtered PWMTRIP to prevent accidental PWM tripping
 - Addition of more analog channels
- Enhancements will Further Reduce Total System Cost by Eliminating Components from the Design.
- Two Serial Ports Available Now with SPI Emulation
- Extra I/O Ports (up to 25 on ADCMC(F)340)
- 16-Bit Aux PWM (Wider Frequency Range)

ADMC(F)34x Product Selection Guide

■ 16-Bit Aux PWM (Mid-Frequency Range)

■ Extra I/O Pins (up to 52 on ADC(F)340)

■ Two Serial Ports Available Now with SPI Emulation

ADMC PART #	PACKAGE	GPIO	ADC I _{SENSE} INPUTS	ADC VOLTAGE INPUTS	FEATURES
340	64-LQFP	25	3	10	SR Mode, PWM Polarity
341	28-SOIC	9	3	3	

ADMC(F)34x Product Enhancements

Embedded DSP Applications Support

- Dedicated Product Line Website Providing Latest Product Information, Articles, Third Party Contact Information, Application Notes and Product Support.
- Worldwide Applications Support: mcgapps@analog.com





www.analog.com

15-3

SECTION 12

MicroConverters

Flash/EEP Memory

+

High Performance Analog I/O

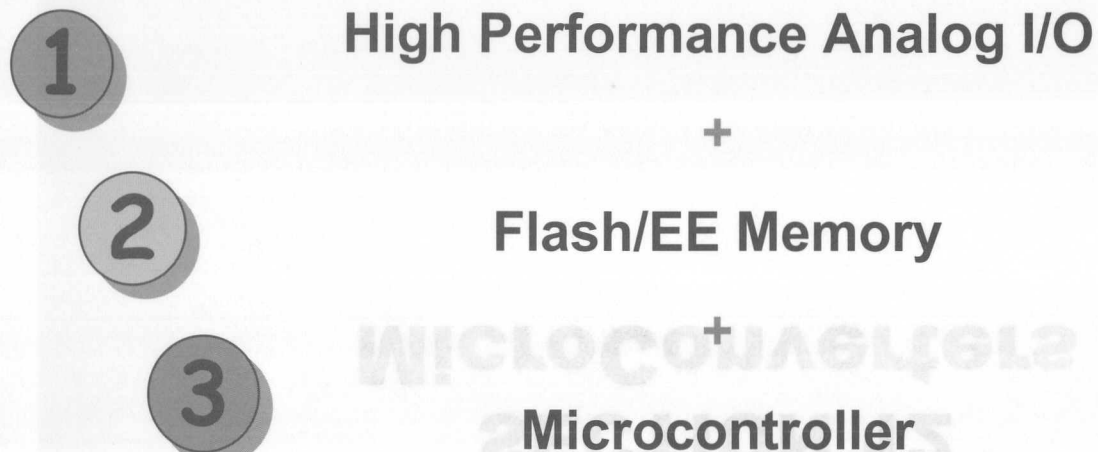
MicroConverter® Definition



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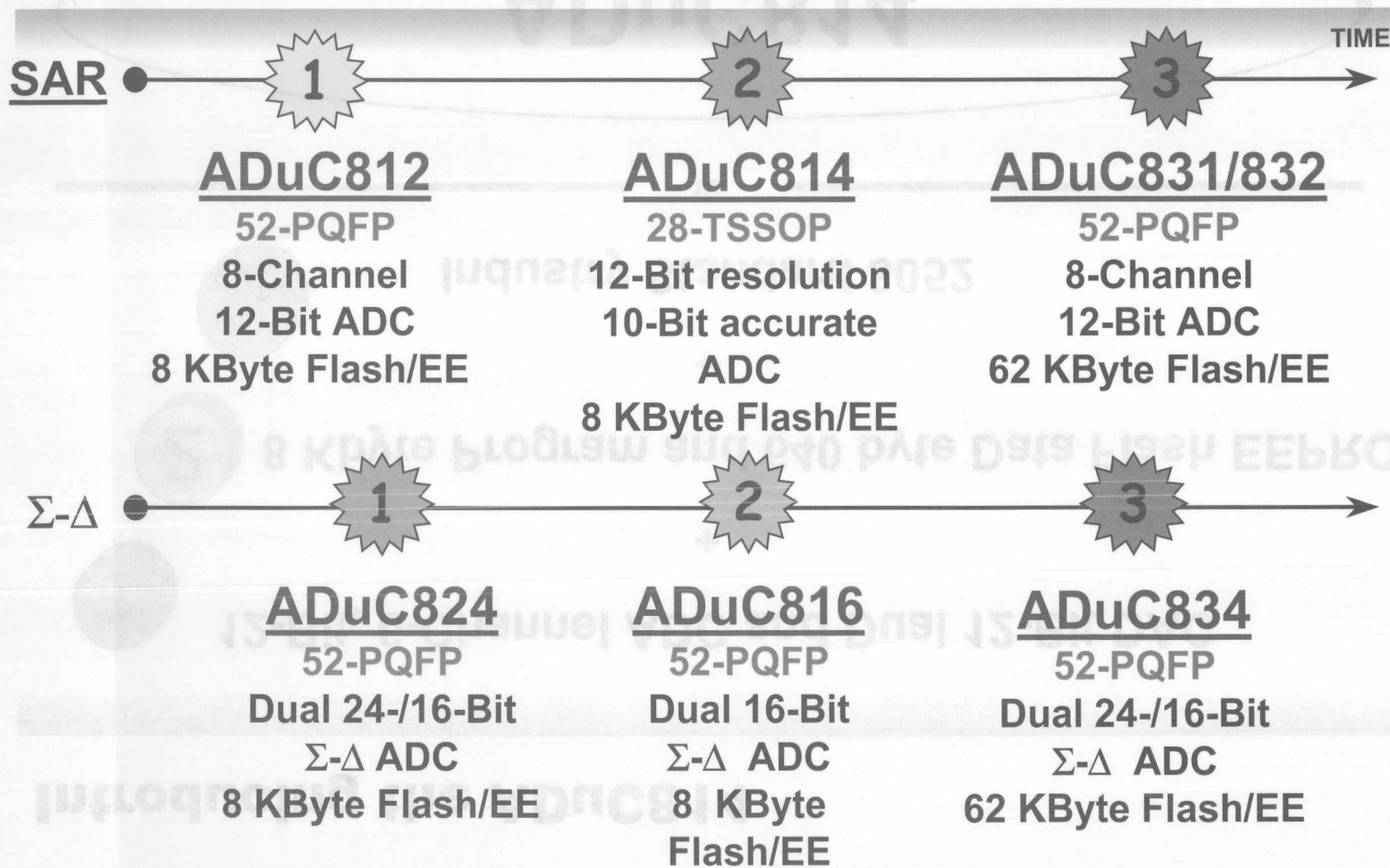
12-1

MicroConverter[®] Definition



MicroConverter[®]

MicroConverter® Product Roadmap



Introducing the ADuC814

1

12-Bit, 6-Channel ADC and Dual 12-Bit DAC

+

2

8 Kbyte Program and 640 byte Data Flash EEPROM

+

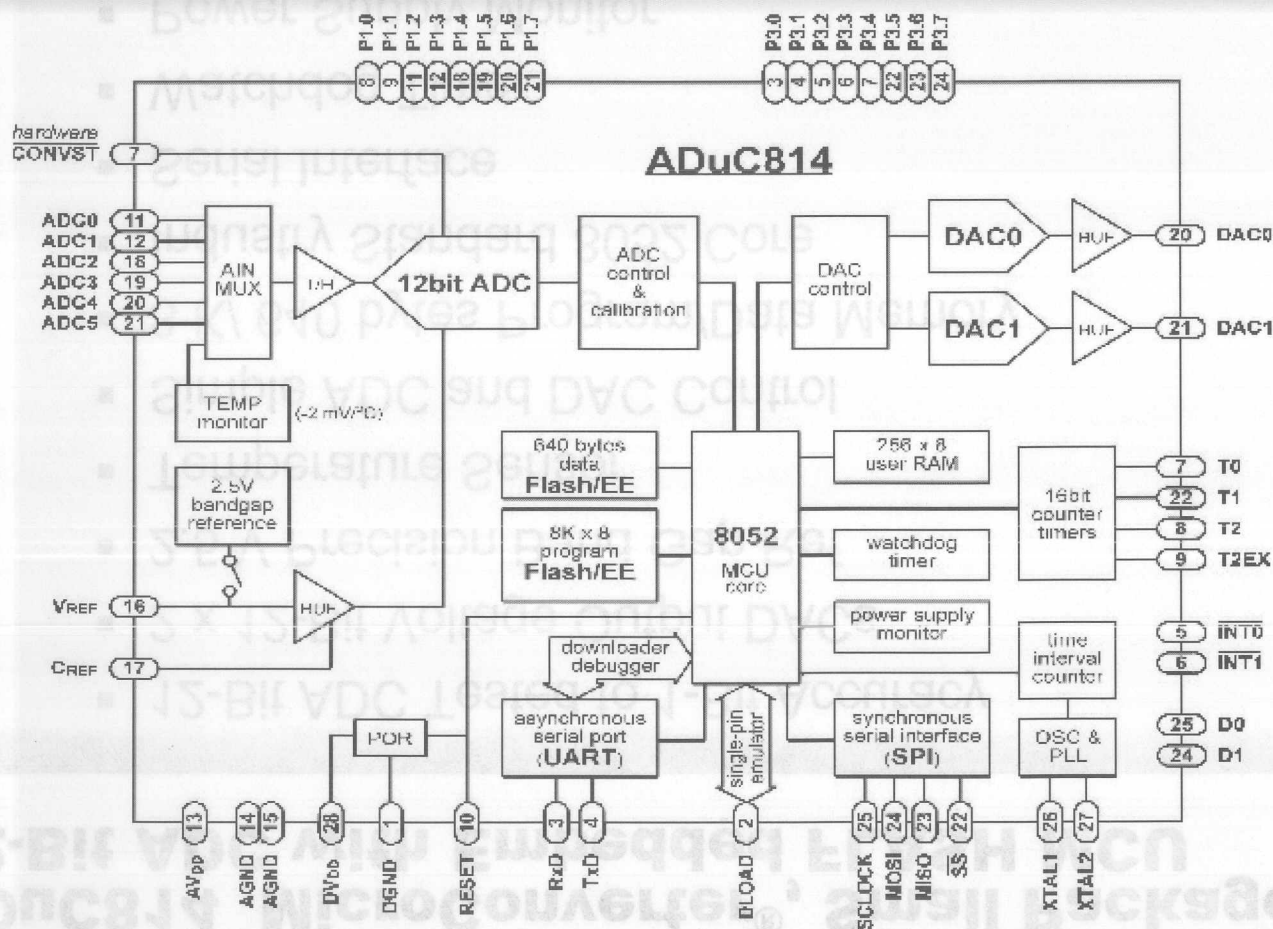
3

Industry Standard 8052

=

ADuC814

ADuC814 MicroConverter®, Small Package 12-Bit ADC with Embedded FLASH MCU



ADuC814 MicroConverter®, Small Package 12-Bit ADC with Embedded FLASH MCU

- 12-Bit ADC Tested to 1-Bit Accuracy
- 2 x 12-Bit Voltage Output DACs
- 2.5 V Precision Band Gap Ref
- Temperature Sensor
- Simple ADC and DAC Control
- 8 K/ 640 bytes Program/Data Memory
- Industry Standard 8052 Core
- Serial Interface
- Watchdog Timer
- Power Supply Monitor
- On-Chip PLL
- 28-TSSOP

ADuC814 MicroConverter[®], Small Package

12-Bit ADC with Embedded FLASH MCU

- **ANALOG I/O**
 - 6-channel 247 kSPS ADC 12-bit resolution
 - High-speed ADC to serial RAM capture
 - Dual voltage output DACs
 - 12-bit resolution, 15 μ s settling time
- **Memory**
 - 8 Kbytes on-chip Flash/EE program memory
 - 640 Bytes on-chip Flash/EE data memory
 - Flash/EE, 100-year retention, 100 K cycles endurance
 - 256 Bytes on-chip data RAM
- **Power**
 - Specified for 3 V and 5 V operation
 - Normal: 3 mA @ 3 V (core CLK = 2.1 MHz)
 - Power-Down: 15 μ A (32 kHz oscillator running)

ADuC814 MicroConverter[®], Small Package 12-Bit ADC with Embedded FLASH MCU

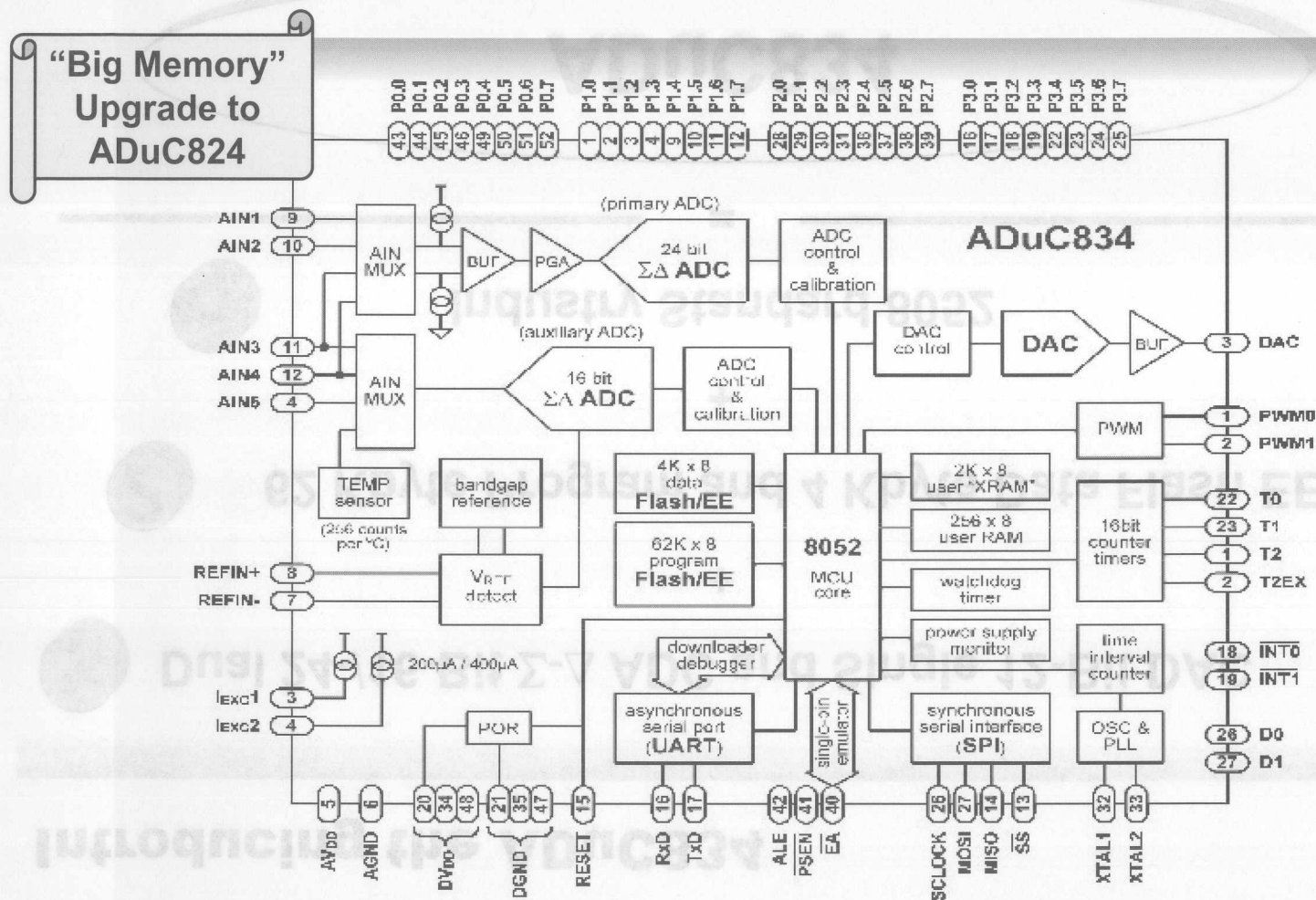
- 8051-Based Core
 - 8051-compatible instruction set (16.78 MHz max)
 - 32 kHz external crystal, on-chip programmable PLL
 - Three 16-bit timer/counters
 - 11 programmable I/O lines
 - 11 interrupt sources, two priority levels
- On-Chip Peripherals
 - On-chip temperature monitor
 - Precision voltage reference
 - Time Interval Counter (TIC)
 - UART serial I/O
 - I²C[®]-compatible and SPI[®] serial I/O
 - Watchdog Timer (WDT), Power Supply Monitor (PSM)

Introducing the ADuC834

- 1 Dual 24-/16-Bit Σ - Δ ADC and Single 12-Bit DAC
- 2 62 Kbyte Program and 4 Kbyte Data Flash EEPROM
- 3 Industry Standard 8052

ADuC834

ADuC834 MicroConverter®, Dual 16-/24-Bit ADCs with Embedded 62 KB FLASH MCU



ADuC834 MicroConverter[®], Dual 16-/24-Bit ADCs with Embedded 62 KB FLASH MCU

- High-Resolution Sigma-Delta ADCs
 - Two independent ADCs (16- and 24-bit resolution)
 - 24-bit no missing codes, primary ADC
 - 13-bit p-p resolution @ 20 Hz, 20 mV range
 - 16-bit p-p resolution @ 20 Hz, 2.56 V range
- Memory
 - 62 Kbytes on-chip Flash/EE program memory
 - 4 KBytes on-chip Flash/EE data memory
 - Flash/EE, 100-year retention, 100 K cycles endurance
 - 2304 bytes on-chip data RAM
- 8051-Based Core
 - 8051-compatible instruction set (12.58 MHz max)
 - 32 kHz external crystal, on-chip programmable PLL
 - 11 interrupt sources, two priority levels
 - Dual data pointer
 - Extended 11-bit stack pointer

ADuC834 MicroConverter[®], Dual 16-/24-Bit ADCs with Embedded 62 KB FLASH MCU

- On-Chip Peripherals
 - 12-bit voltage output DAC
 - Dual 16-bit Σ - Δ DACs/PWMs
 - On-chip temperature sensor
 - Dual excitation current sources
 - Time Interval Counter (TIC)
 - Flexible Serial I/O
 - Watchdog Timer (WDT), Power Supply Monitor (PSM)
- Power
 - Specified for 3 V and 5 V Operation
 - Normal: 3 mA @ 3 V (Core CLK = 1.5 MHz)
 - Power-down: 20 μ A max with wake-up CCT running

ADuC834 MicroConverter[®], Dual 16-/24-Bit ADCs with Embedded 62 KB FLASH MCU

100% Identical to ADuC824 (hardware & software), except....

- 62K of Flash/EE Code Space (versus 8K)
- 4K of Flash/EE Data Space (versus 640bytes)
- 2K of Additional on-chip RAM (plus normal 256bytes)
- Flexible Dual PWM
- Flexible High-Speed UART Baud Rate Generator (up to 230kbaud)
- “U-Load Mode” – Allows User Implemented Remote Download (among other things)

Introducing the ADuC836

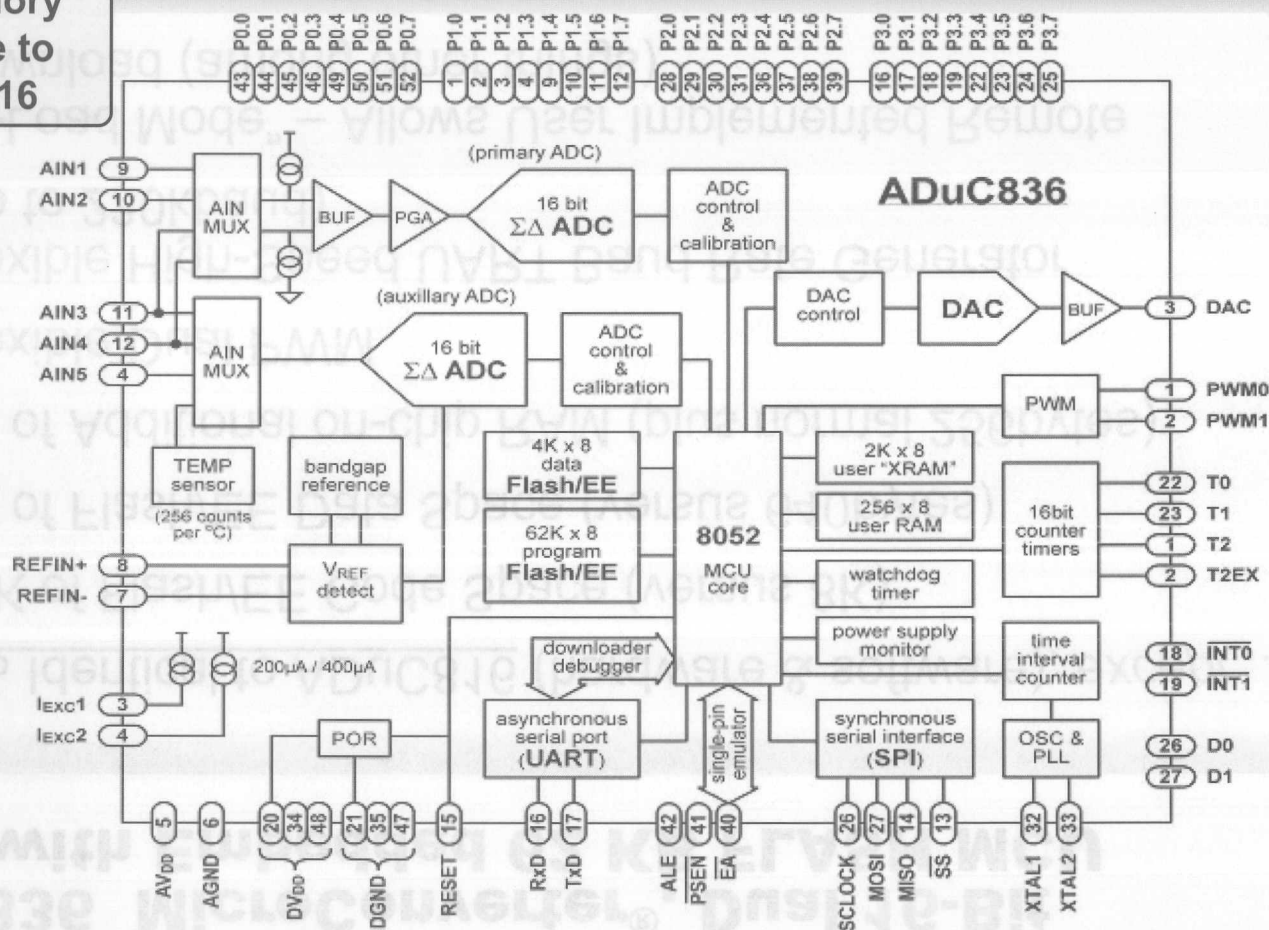
- 1 Dual 16-Bit Σ - Δ ADC and Single 12-Bit DAC
- +
- 2 62 Kbyte Program and 4 Kbyte Data Flash EEPROM
- +
- 3 Industry Standard 8052

=

ADuC836

ADuC836 MicroConverter[®], Dual 16-Bit ADCs with Embedded 62 KB FLASH MCU

"Big Memory"
Upgrade to
ADuC816



ADuC836 MicroConverter®, Dual 16-Bit ADCs with Embedded 62 KB FLASH MCU

100% Identical to ADuC816 (hardware & software), except....

- 62K of Flash/EE Code Space (versus 8K)
- 4K of Flash/EE Data Space (versus 640bytes)
- 2K of Additional on-chip RAM (plus normal 256bytes)
- Flexible Dual PWM
- Flexible High-Speed UART Baud Rate Generator (up to 230kbaud)
- “U-Load Mode” – Allows User Implemented Remote Download (among other things)

100% Identical to ADuC834 (hardware & software), except....

- Primary ADC is 16 Bits rather than 24 Bits

Introducing the ADuC831/ADuC832

1

12-Bit, 8-Channel ADC and Dual 12-Bit DAC

2

62 Kbyte Program and 4 Kbyte Data Flash EEPROM

3

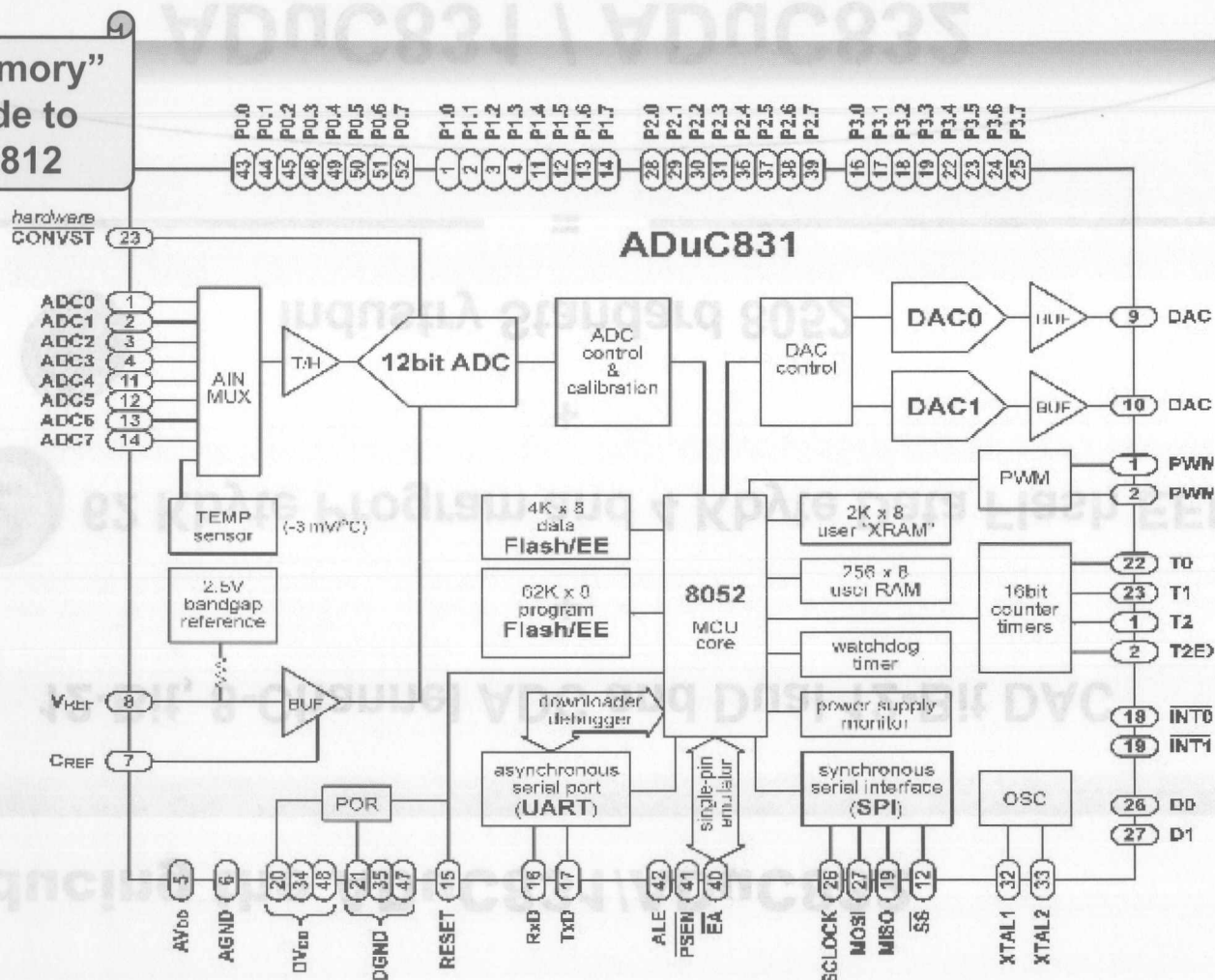
Industry Standard 8052

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ADuC831 / ADuC832

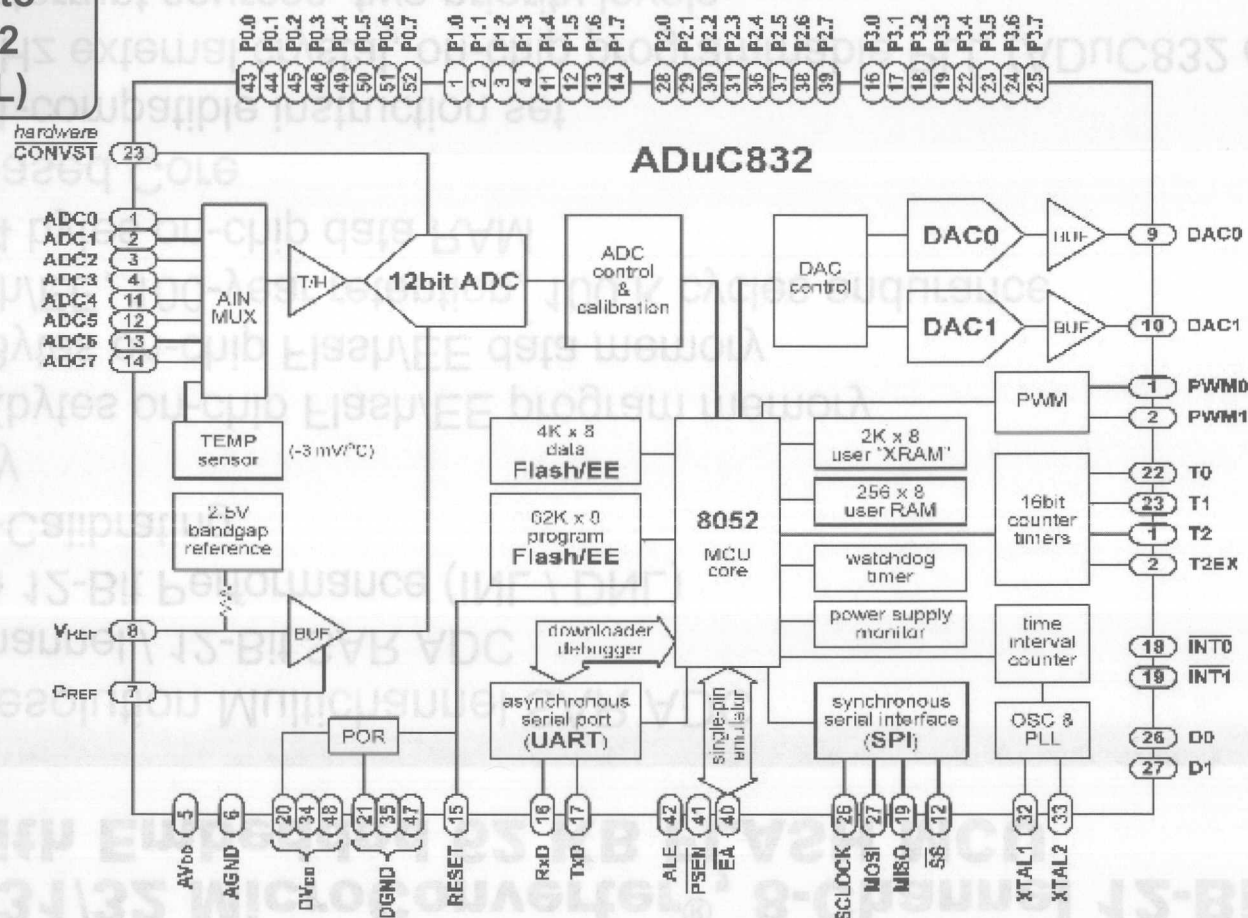
ADuC831 MicroConverter®, 8-Channel 12-Bit ADC with Embedded 62 KB FLASH MCU

**“Big Memory”
Upgrade to
ADuC812**



ADuC832 MicroConverter®, 8-Channel 12-Bit ADC with Embedded 62 KB FLASH MCU

“Big Memory”
Upgrade to
ADuC812
(plus PLL)



ADuC831/32 MicroConverter®, 8-Channel 12-Bit ADC with Embedded 62 KB FLASH MCU

- High-Resolution Multichannel SAR ADC
 - 8-Channel / 12-Bit SAR ADC
 - True 12-Bit Performance (INL / DNL)
 - Self-Calibrating
- Memory
 - 62 Kbytes on-chip Flash/EE program memory
 - 4 KBytes on-chip Flash/EE data memory
 - Flash/EE, 100-year retention, 100 K cycles endurance
 - 2304 bytes on-chip data RAM
- 8051-Based Core
 - 8051-compatible instruction set
 - 32 kHz external crystal, on-chip programmable PLL (ADuC832 only)
 - 11 interrupt sources, two priority levels
 - Dual data pointer
 - Extended 11-bit stack pointer

ADuC831/32 MicroConverter®, 8-Channel 12-Bit ADC with Embedded 62 KB FLASH MCU

- On-Chip Peripherals
 - Dual 12-bit voltage output DACs
 - Dual 16-bit Σ - Δ DACs/PWMs
 - On-chip temperature monitor
 - Dual excitation current sources
 - Time Interval Counter (TIC) (ADuC832 only)
 - Flexible Serial I/O
 - Watchdog Timer (WDT), Power Supply Monitor (PSM)
- Power
 - Specified for 3 V and 5 V Operation
 - Normal: 3 mA @ 3 V (Core CLK = 2 MHz)
 - Power-down: 20 μ A max with wake-up CCT running (ADuC832 only)

ADuC831/32 MicroConverter[®], 8-Channel 12-Bit ADC with Embedded 62 KB FLASH MCU

100% Identical to ADuC812 (hardware and software) *except...*

- 62K of Flash/EE Code Space (Versus 8 K)
- 4K of Flash/EE Data Space (Versus 640 Bytes)
- 2K of Additional On-Chip RAM (Plus Normal 256 Bytes)
- Flexible Dual PWM
- Flexible High-Speed UART Baud Rate Generator (up to 230 k Baud)
- “U-Load Mode”—Allows User-Implemented Remote Download (Among Other Things)
- Some Minor Register Differences (i.e., Can not Claim 100% Software Backward Compatibility)
- PLL and Time-Interval-Counter (ADuC832 Only)

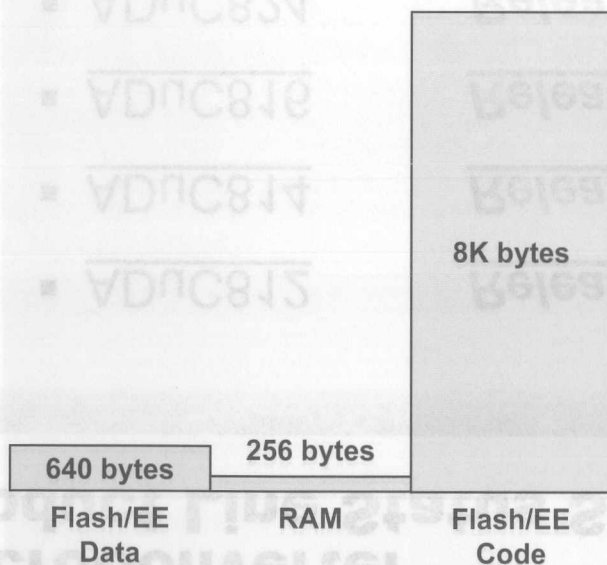
MicroConverter® Product Line Status Summary

- | | |
|------------------|------------------------|
| ▪ <u>ADuC812</u> | <u><i>Released</i></u> |
| ▪ <u>ADuC814</u> | <u><i>Released</i></u> |
| ▪ <u>ADuC816</u> | <u><i>Released</i></u> |
| ▪ <u>ADuC824</u> | <u><i>Released</i></u> |
| ▪ <u>ADuC831</u> | (Sampling) |
| ▪ <u>ADuC832</u> | (Sampling) |
| ▪ <u>ADuC834</u> | (Sampling) |
| ▪ <u>ADuC836</u> | (Sampling) |

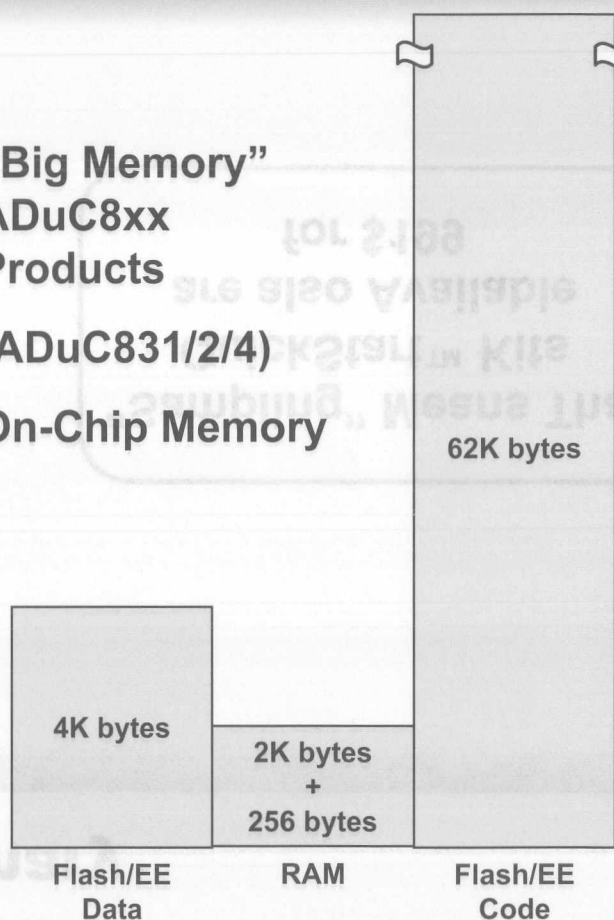
**“Sampling” Means That
QuickStart™ Kits
are also Available
for \$199**

New Product Developments — More Memory

“Standard” ADuC8xx Products
(ADuC812/814/816/824)
On-Chip Memory

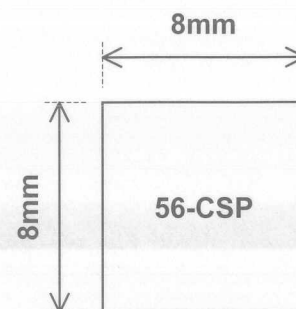
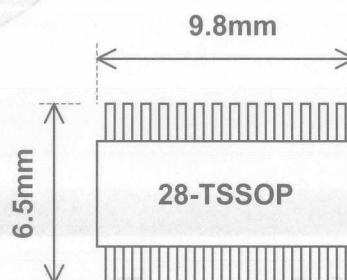
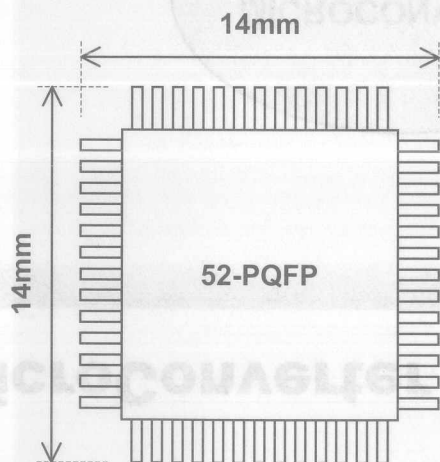
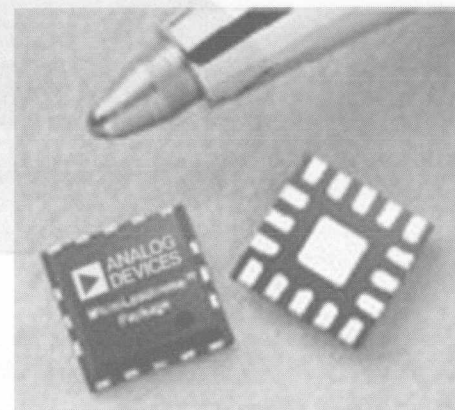


“Big Memory” ADuC8xx Products
(ADuC831/2/4)
On-Chip Memory



New Product Developments — Smaller Packages

- Chip Scale Packages (CSP)
- ADuC812, ADuC816, ADuC824...
 - 56-CSP versions released or soon to come
- ADuC834, ADuC836, ADuC831, ADuC832...
 - Will release in both 56-CSP and 52-PQFP



MicroConverter — Design Support

**MICROCONVERTER
WEBSITE**

1

**QUICKSTART
DEVELOPMENT KIT**

2

**THIRD PARTY
DEVELOPMENT TOOLS**

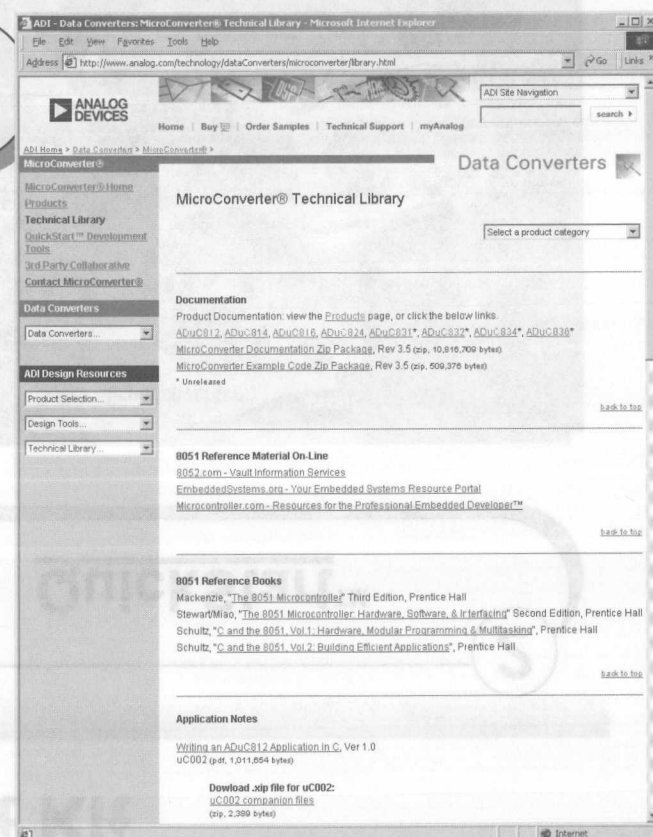
3

MicroConverter — Website

1

www.analog.com/MicroConverter

- Data Sheets, Technical Notes
- Example Code
- 8051 Reference Material
- Free Tools Downloads/Upgrades
- Links to Third Party Sites
- Articles and Press Releases



MicroConverter Development Kit

- Documentation
- Evaluation Board
- Regulated Power Supply
- Serial Port
- Software
 - Metalink Assembler
 - Windows Simulator
 - Serial Downloader
 - Windows Debugger
 - Example Code

QuickStart™

2



MicroConverter Third Parties

3

Third Party Tools

COMPILERS —



RAISONANCE



EMULATORS —



*

PROGRAMMERS —



PROGRAMMERS



EMULATORS



Accellion
Limited



COMPILERS



SOFTWARE
RESOURCE



MICROCONVERTER THIRD PARTIES

Third Party Tools

3

SECTION 13

MICROPROCESSOR SUPPORT

INTERFACE

INTERFACE

THERMAL MANAGEMENT

SYSTEM MANAGEMENT



www.analog.com

13-1

SYSTEM MANAGEMENT

SYSTEM MANAGEMENT

INTERFACE

INTERFACE

MICROPROCESSOR SUPPORT

SECTION 13



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13-2

ADIs “E” Series Of Interface Chips

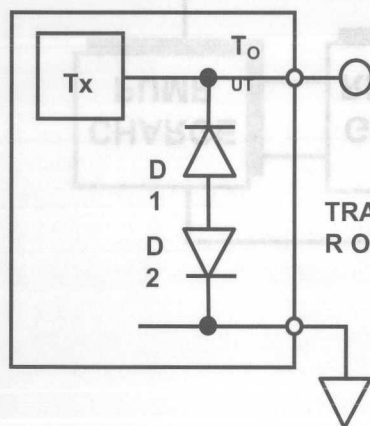
- Provides 15 KV ESD Protection
 - Protection diodes on-chip
 - Eliminates TransZorbs
- Low EMI
- Meets European “CE” Requirements
 - IEC 1000-4-2 (ESD)
 - IEC 1000-4-3 (Immunity)
 - IEC 1000-4-4 (EFT)
 - EN55022/CISPR22 (EMC)

European Requirements — The CE Mark

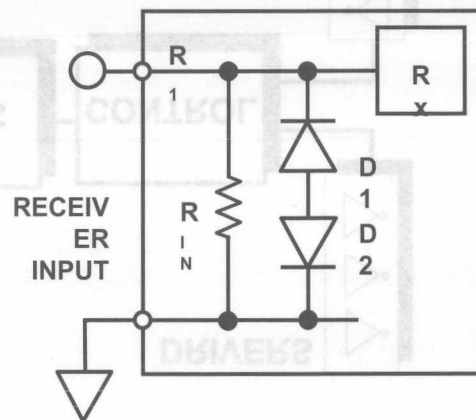


- EN 20551 (CISPR 25) (EMC)
- IEC 1000-4-4 (EFT)
- IEC 1000-4-3 (Immunity)
- IEC 1000-4-2 (ESD)
- Meets European EMC Requirements
- Low EMI
- EMC Compatibility
- Eliminate EM Emissions
- Protection diodes on-chip
- Provides 100% ESD Protection
- EM Immunity
 - ESD
 - EFT

ESD/EFT Protection



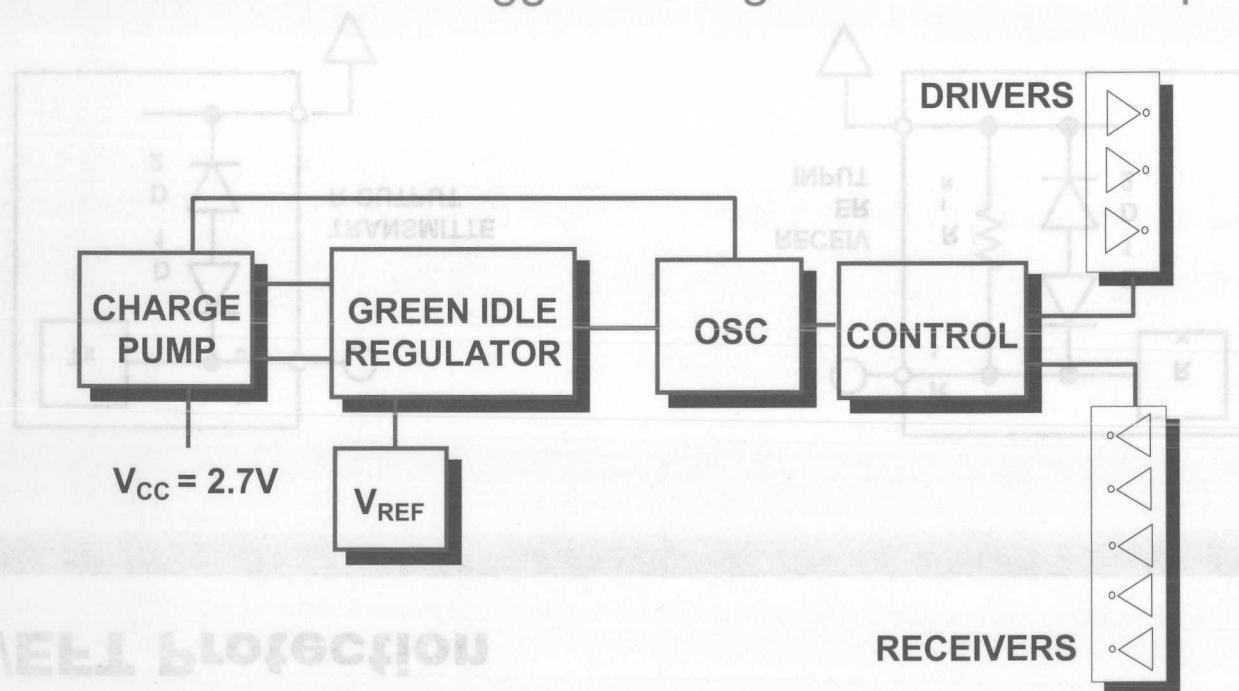
**TRANSMITTER OUTPUT
PROTECTION STRUCTURE**



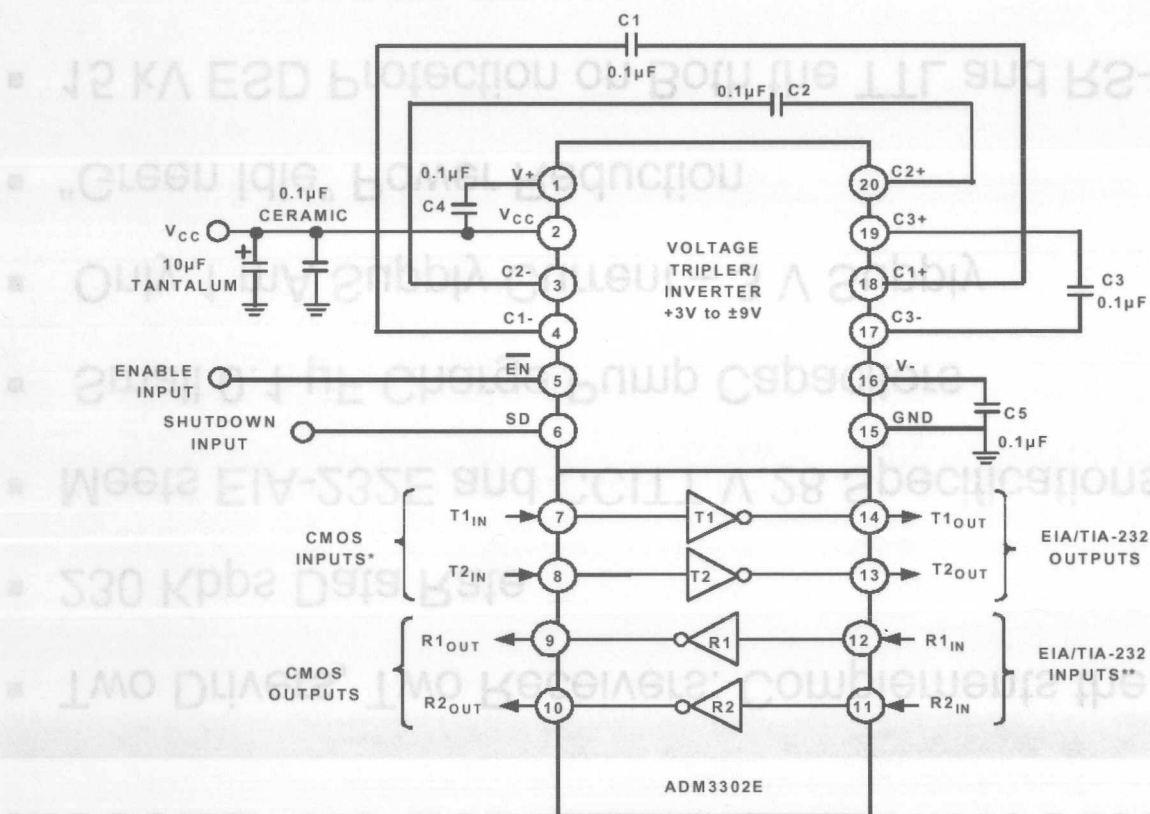
**RECEIVER INPUT
PROTECTION STRUCTURE**

Green Idle™ Architecture

The Green Idle Architecture slows the charge pump during periods of inactivity to reduce the power dissipation. One receiver is left active to trigger the regulator back to full power.



ADM3302E RS-232E Line Driver/Receiver



Notes:

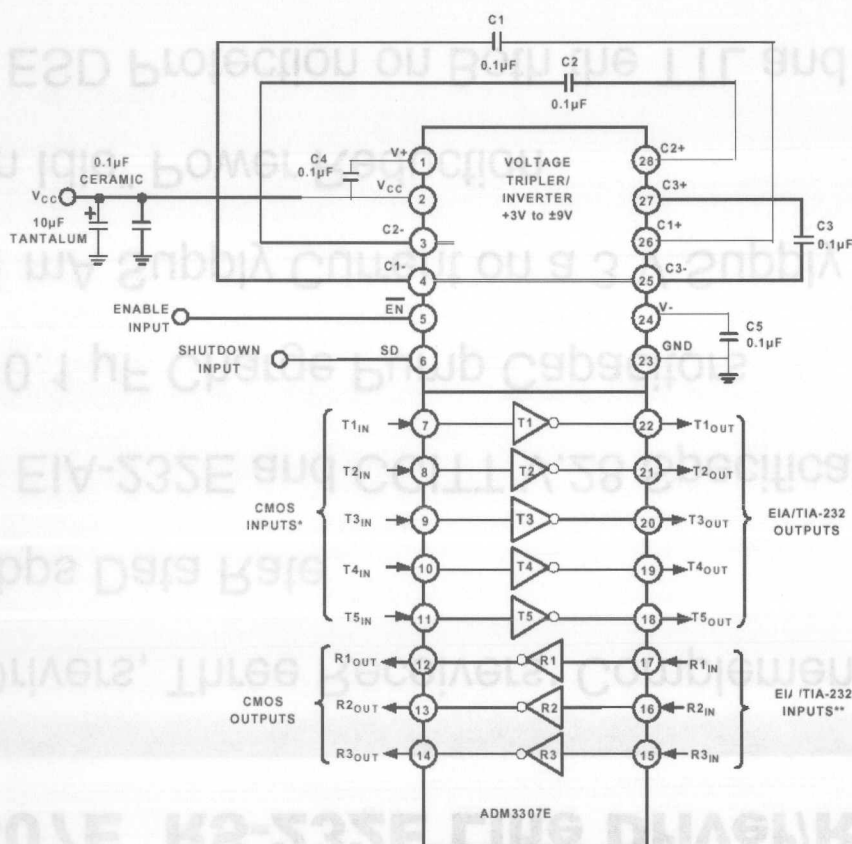
* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH CMOS INPUT

** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

ADM3302E RS-232E Line Driver/Receiver

- Two Drivers, Two Receivers: Complements the ADM3311
- 230 Kbps Data Rate
- Meets EIA-232E and CCITT V.28 Specifications
- Small 0.1 μ F Charge Pump Capacitors
- Only 1 mA Supply Current – 3 V Supply
- “Green Idle” Power Reduction
- 15 kV ESD Protection on Both the TTL and RS-232 Sides
- 20-Lead TSSOP Package
- –40° C to +85° C Operation

ADM3307E RS-232 Line Driver/Receiver



Notes:

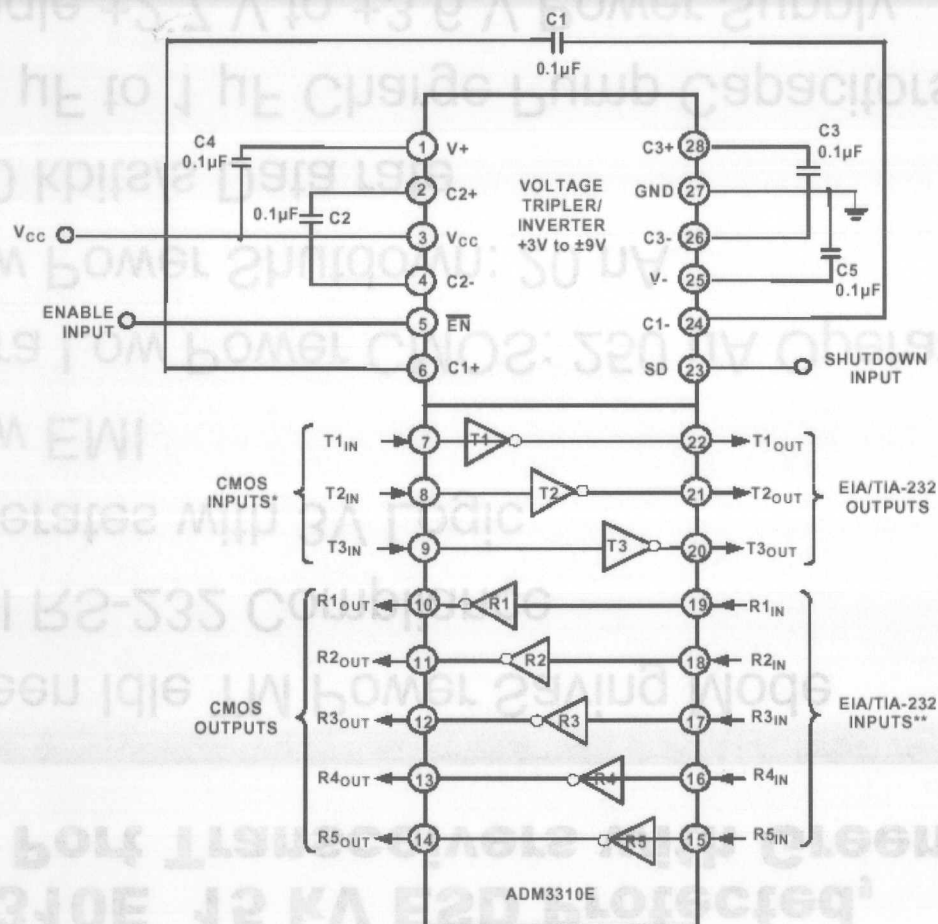
* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH CMOS INPUT

** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

ADM3307E RS-232E Line Driver/Receiver

- Five Drivers, Three Receivers: Complements the ADM3311
- 230 Kbps Data Rate
- Meets EIA-232E and CCITT V.28 Specifications
- Small 0.1 μ F Charge Pump Capacitors
- Only 1 mA Supply Current on a 3 V Supply
- “Green Idle” Power Reduction
- 15 kV ESD Protection on Both the TTL and RS-232 Sides
- 28-Lead TSSOP and LFCSP Packages
- -40° C to $+85^{\circ}$ C Operation

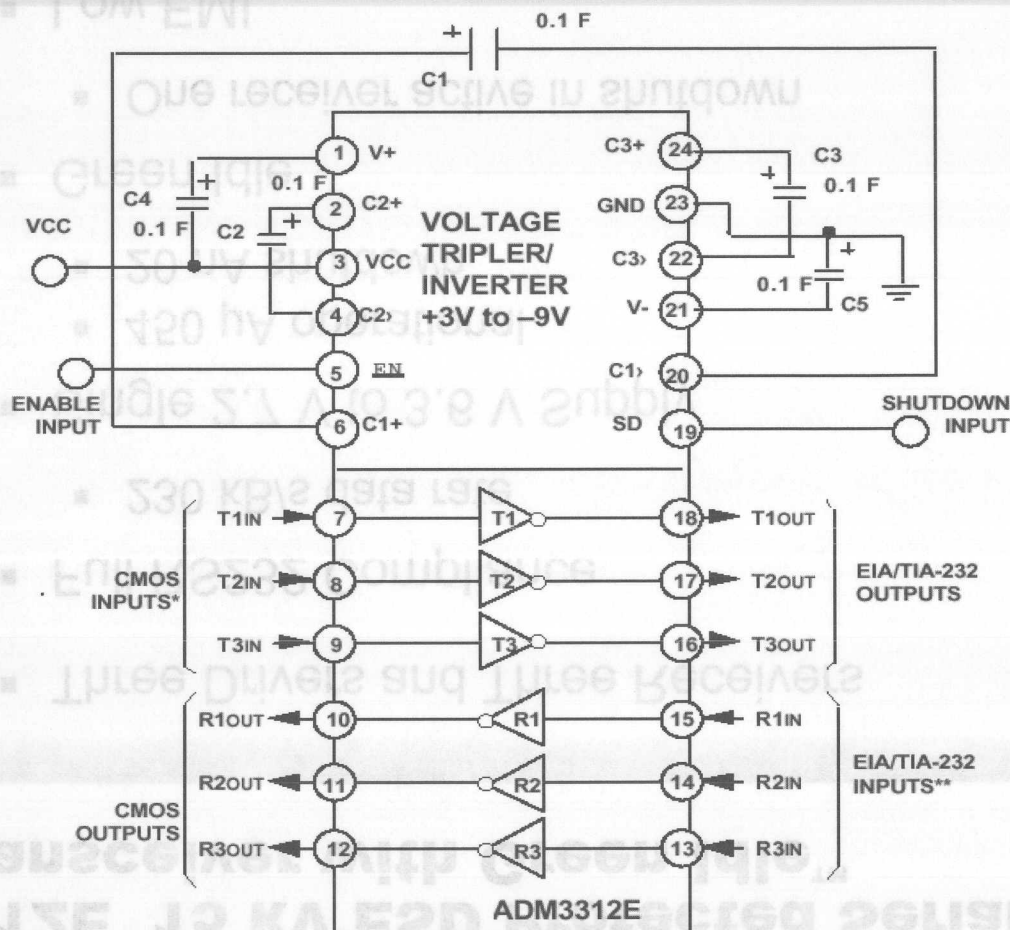
ADM3310E 15 kV ESD Protected, Serial Port Transceivers with Green-Idle™



ADM3310E 15 kV ESD Protected, Serial Port Transceivers with Green-Idle™

- Green Idle™ Power Saving Mode
- Full RS-232 Compliance
- Operates with 3V Logic
- Low EMI
- Ultra Low Power CMOS: 250 μ A Operation
- Low Power Shutdown: 20 nA
- 460 kbits/s Data rate
- 0.1 μ F to 1 μ F Charge Pump Capacitors
- Single +2.7 V to +3.6 V Power Supply
- Two Receivers Active in Shutdown
- ESD >15 kV

ADM3312E 15 kV ESD Protected Serial Port Transceiver with Green Idle™



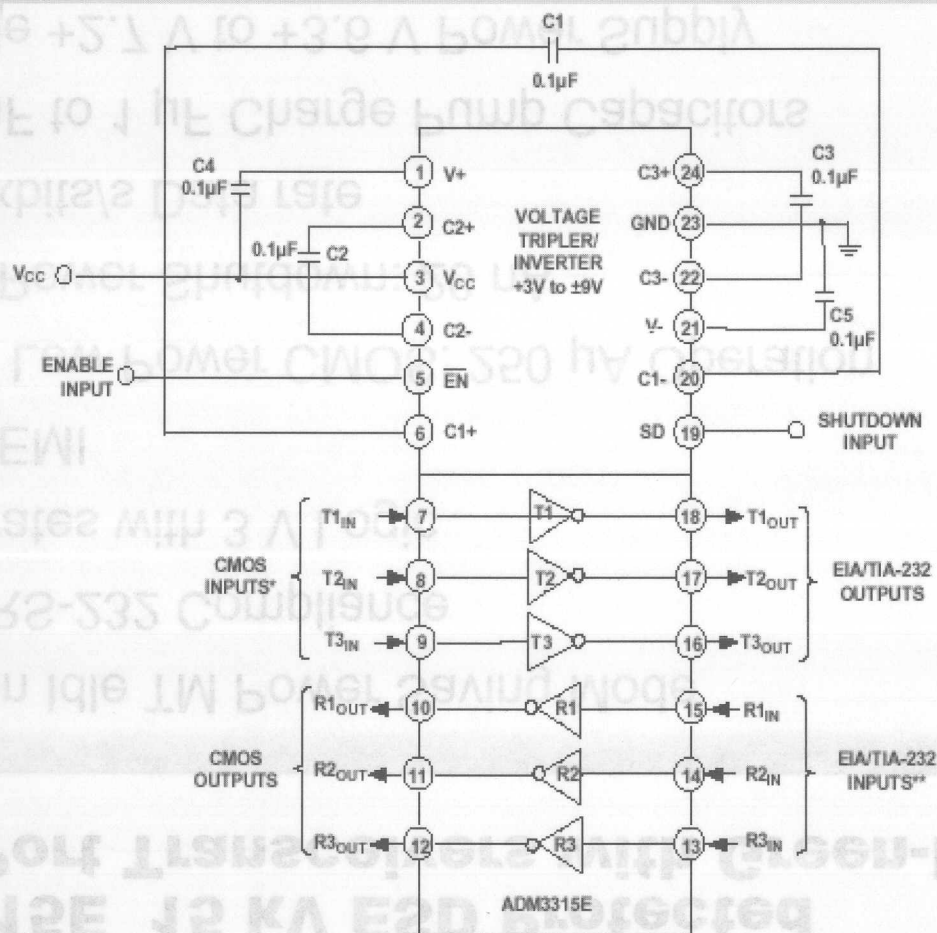
ADM3312E 15 kV ESD Protected Serial Port Transceiver with Green Idle™

- Three Drivers and Three Receivers
- Full RS232 Compliance
 - 230 kB/s data rate
- Single 2.7 V to 3.6 V Supply
 - 450 μ A operational
 - 20 nA shutdown
- Green Idle
 - One receiver active in shutdown
- Low EMI

ADM3315E 15 kV ESD Protected Serial Port Transceivers with Green-Idle™

- One Receiver Active in Shutdown

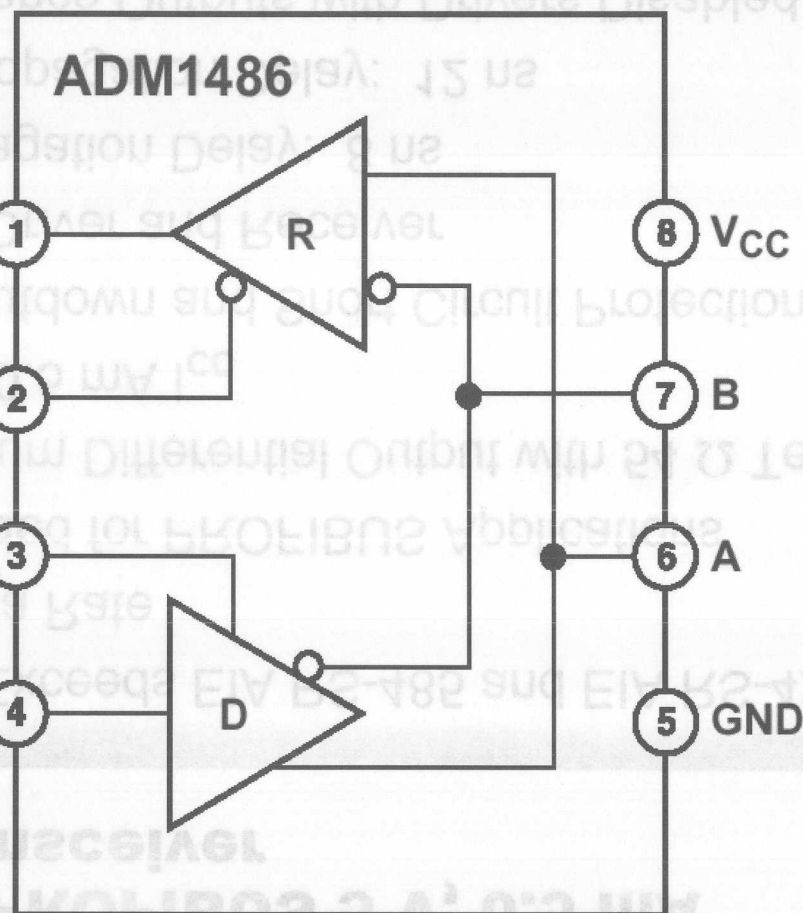
- Single +5V A to +3.0 V Low Voltage Supply
- 0.1 μ F to 1 μ F Charge Pump Capacitors
- 480 kbps Data Rate
- Low Power Shutdown Mode
- Ultra Low Power CMOS 3.3V to 5V Operation
- Low EMI
- Operates with 3 V Logic
- Full RS-232 Compliance
- Green Idle™ Low Power Standby Mode



ADM3315E 15 kV ESD Protected Serial Port Transceivers with Green-Idle™

- Green Idle™ Power Saving Mode
- Full RS-232 Compliance
- Operates with 3 V Logic
- Low EMI
- Ultra Low Power CMOS: 250 μ A Operation
- Low Power Shutdown: 20 nA
- 460 kbits/s Data rate
- 0.1 μ F to 1 μ F Charge Pump Capacitors
- Single +2.7 V to +3.6 V Power Supply
- One Receiver Active in Shutdown
- ESD >15 kV

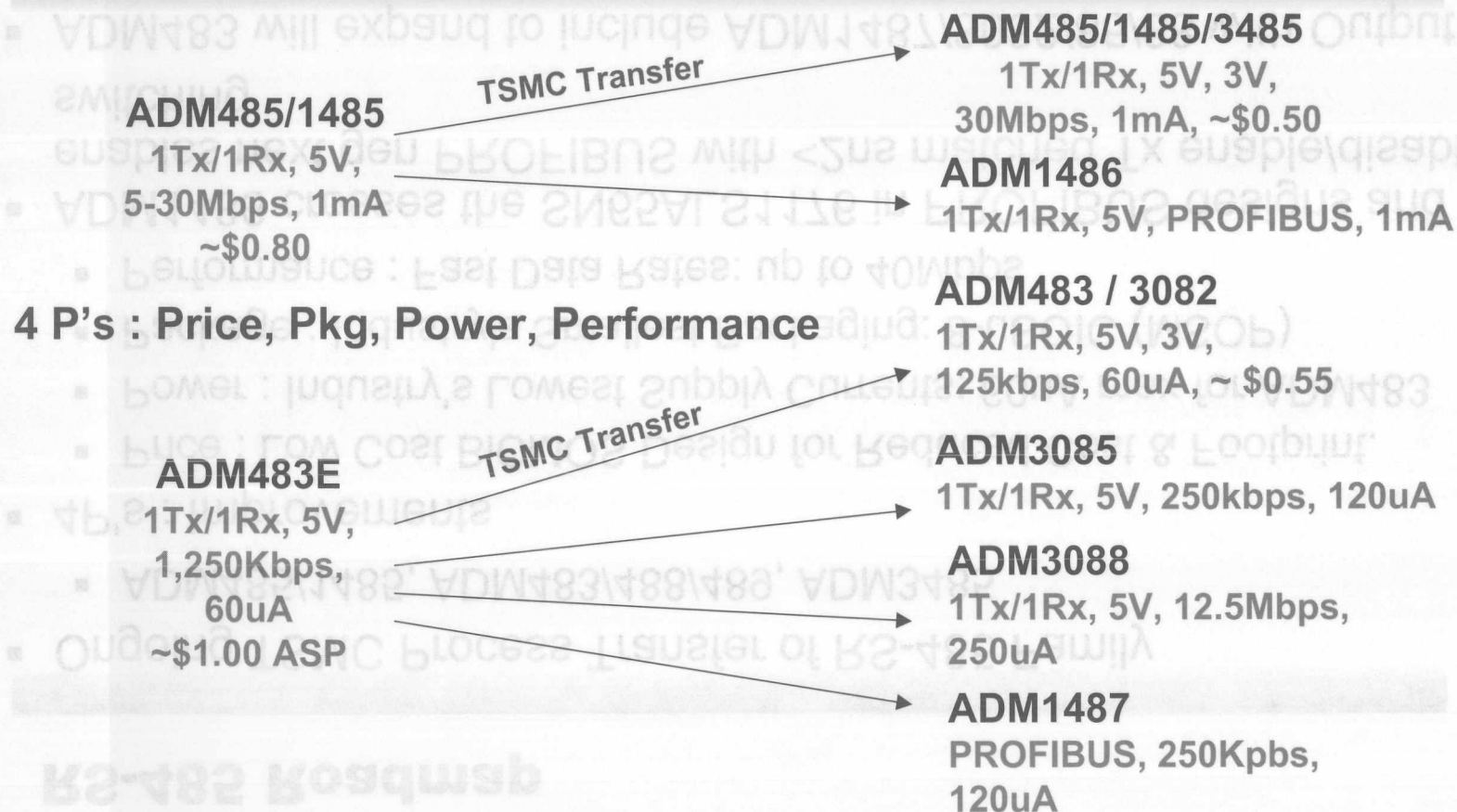
ADM1486 PROFIBUS 5 V, 0.5 mA RS-485 Transceiver



ADM1486 PROFIBUS 5 V, 0.5 mA RS-485 Transceiver

- Meets and Exceeds EIA RS-485 and EIA RS-422
- 40 Mb/s Data Rate
- Recommended for PROFIBUS Applications
- 2.1 V Minimum Differential Output with 54 Ω Termination
- Low Power 0.5 mA I_{CC}
- Thermal Shutdown and Short Circuit Protection
- Zero Skew Driver and Receiver
- Driver Propagation Delay: 8 ns
- Receiver Propagation Delay: 12 ns
- High Impedance Outputs with Drivers Disabled or Power Off
- Superior Upgrade for SN65ALS1176

RS-485 Roadmap



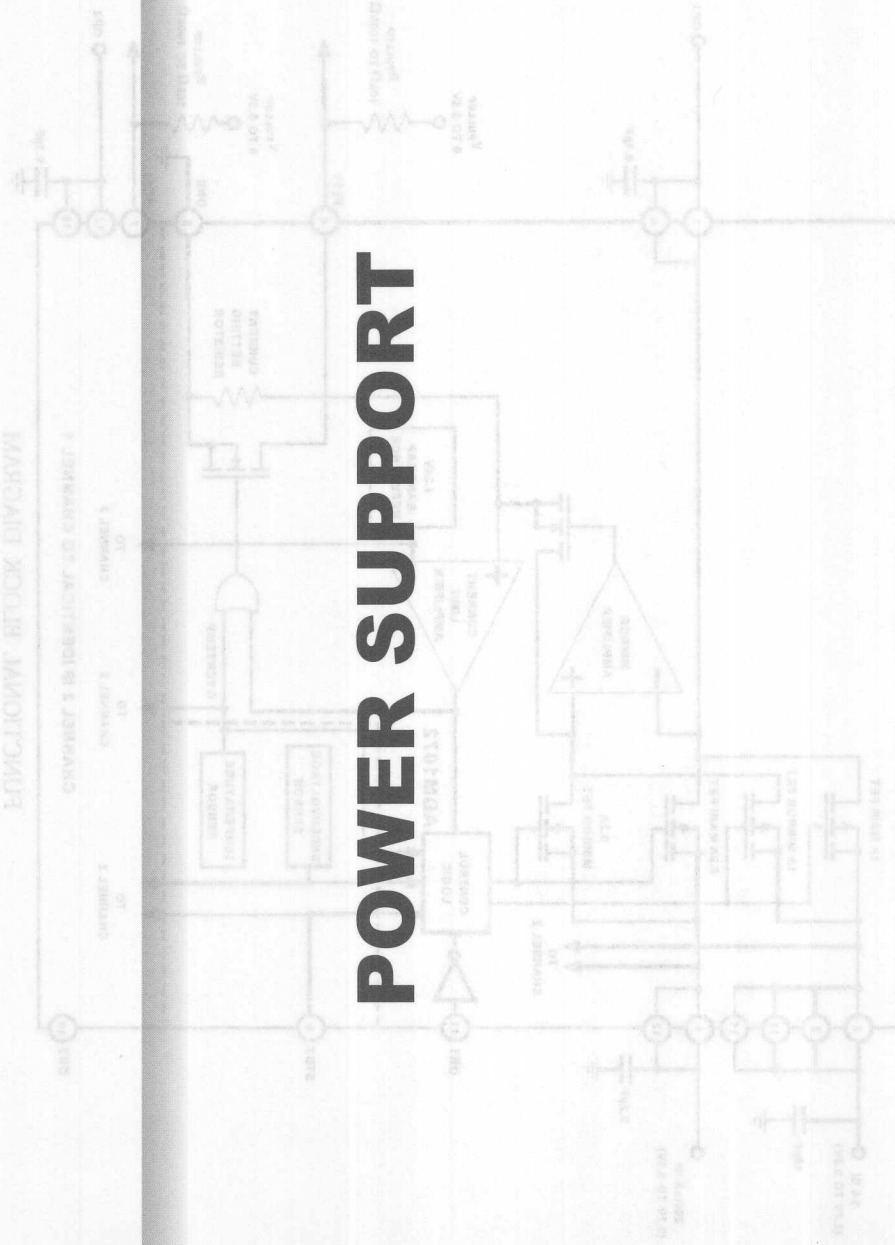
4 P's : Price, Pkg, Power, Performance

Further Extension of 3V RS485

RS-485 Roadmap

- Ongoing TSMC Process Transfer of RS-485 Family
 - ADM485/1485, ADM483/488/489, ADM3485
- 4P's : Improvements
 - Price : Low Cost BiCMOS Design for Reduced Cost & Footprint.
 - Power : Industry's Lowest Supply Currents: 60uA max for ADM483
 - Package : Industry's Smallest Packaging: 8-uSOIC (MSOP)
 - Performance : Fast Data Rates: up to 40Mbps
- ADM1486 crosses the SN65ALS1176 in PROFIBUS designs and enables next gen PROFIBUS with <2ns matched Tx enable/disable switching
- ADM483 will expand to include ADM1487/3082/85/88 with Output Slew Rate Limiting, True Fail Safe and 1/8 unit load inputs and 1uA Shutdown.

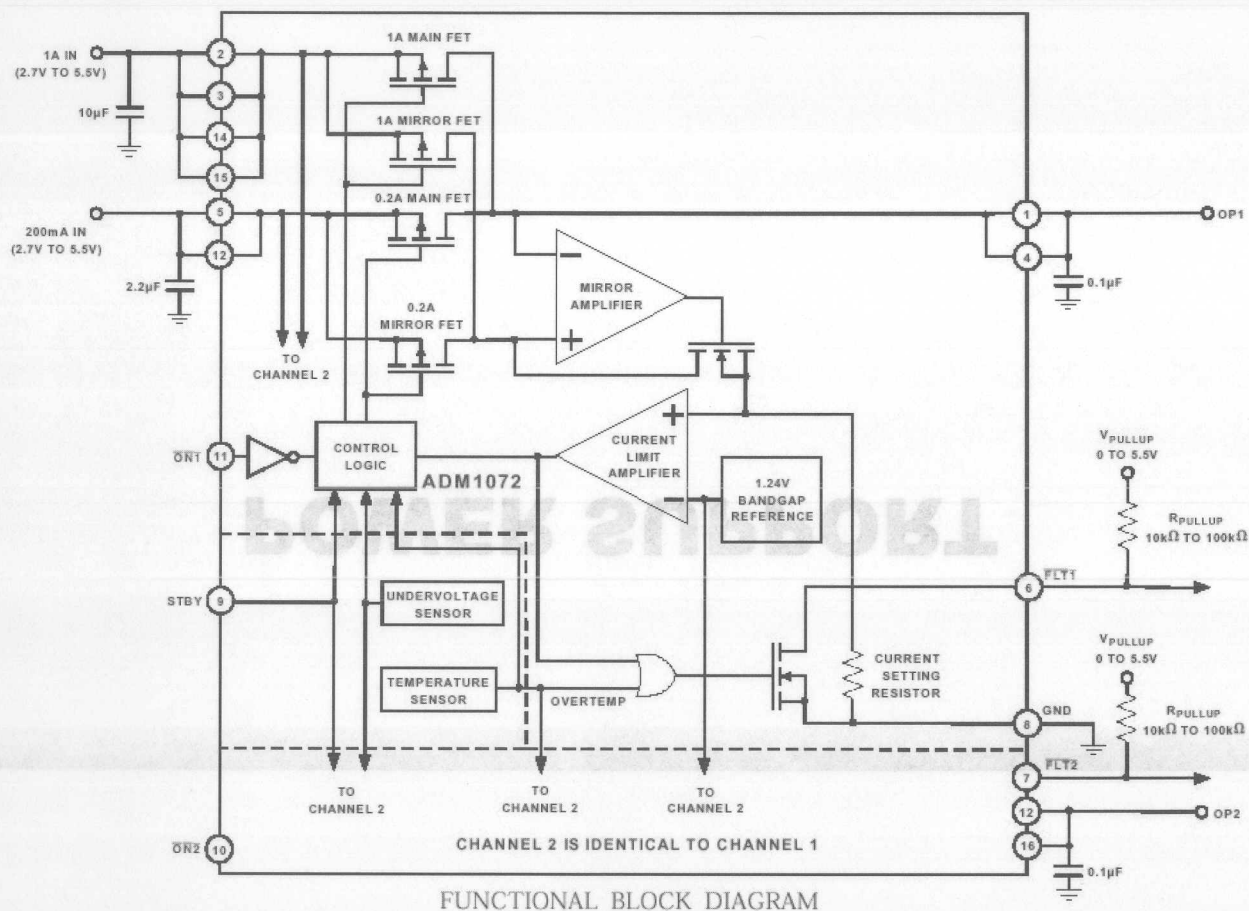
EXCLUSIVE BLOCK DIAGRAM



POWER SUPPORT

With current limit and thermal shutdown
AD9405 Dual 10-Bit DAC

ADM1072 Dual 1 A High-Side Switch with Current Limit and Thermal Shutdown

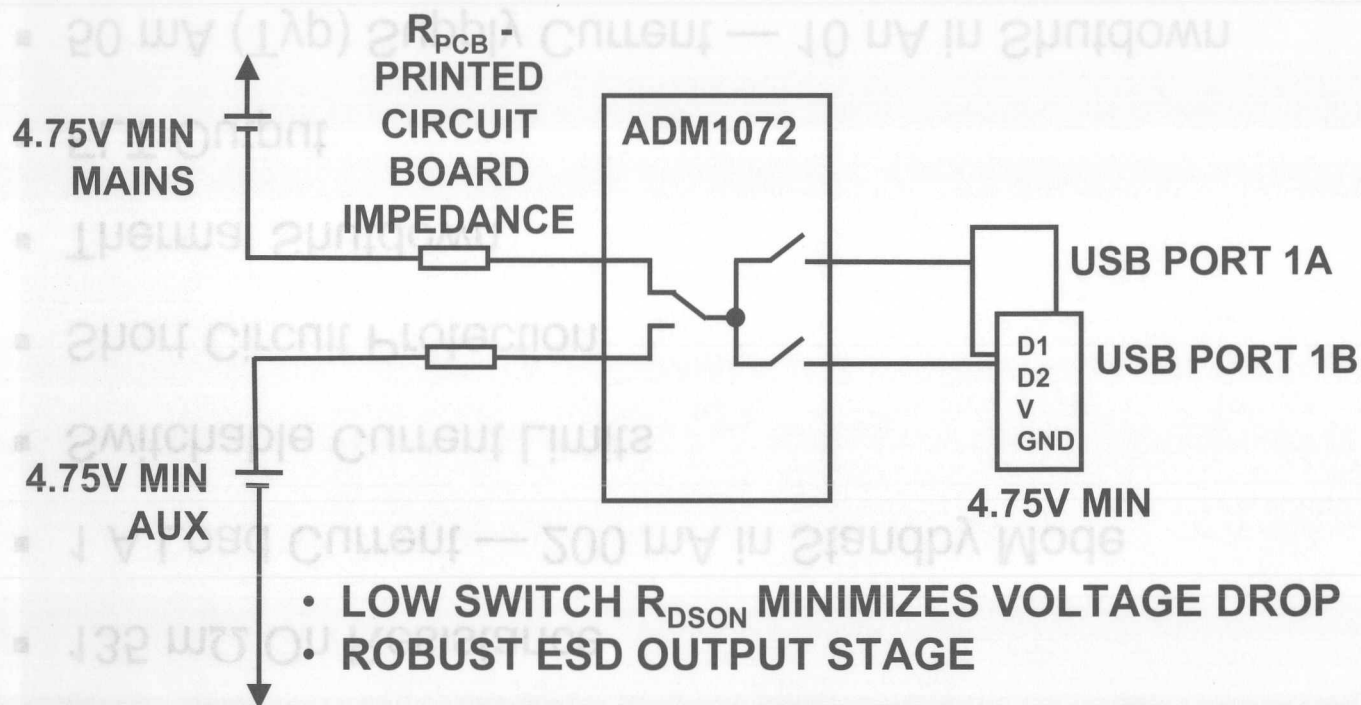


ADM1072 Dual 1 A High-Side Switch with Current Limit and Thermal Shutdown

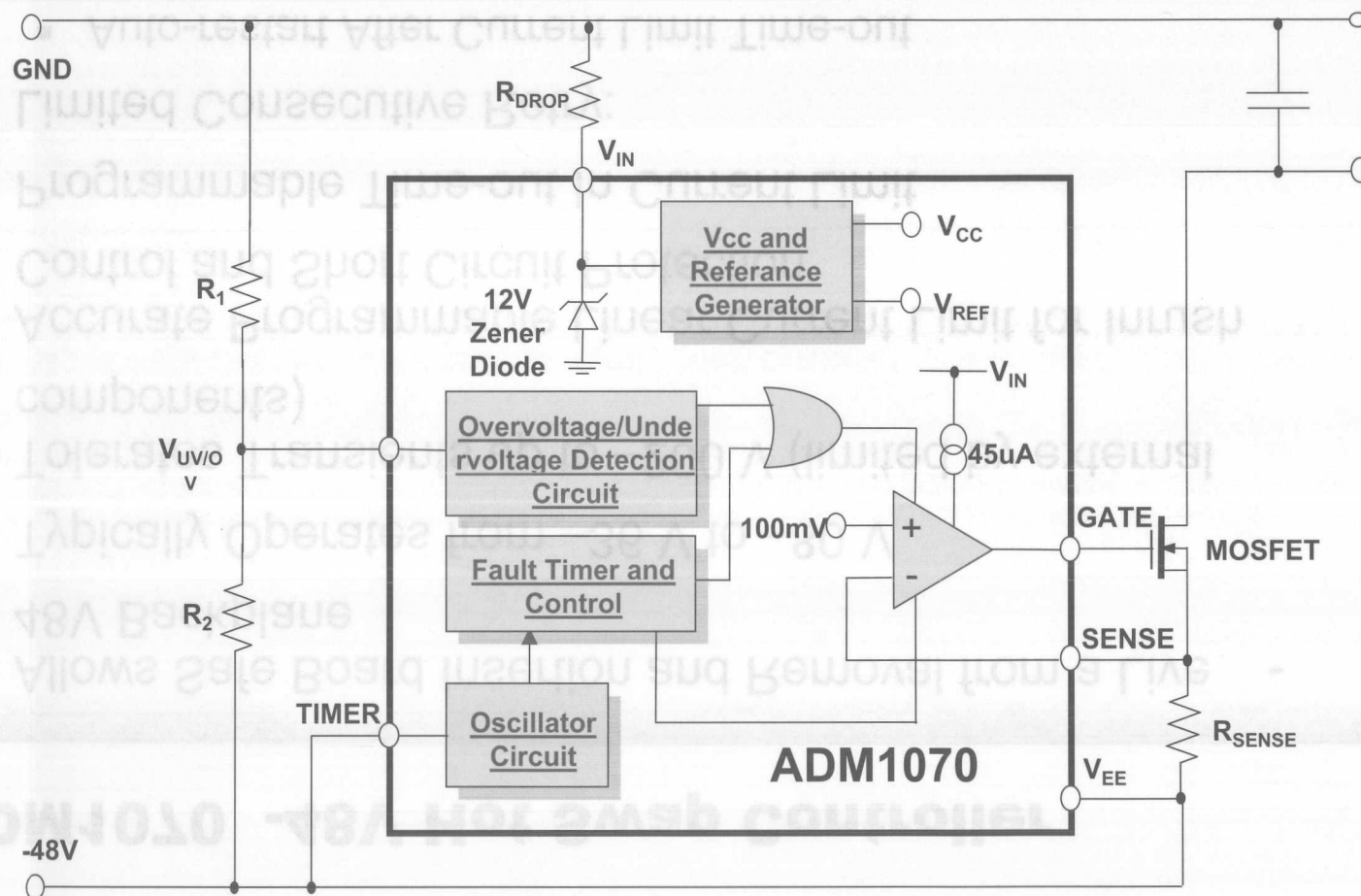
- 135 mΩ On Resistance
- 1 A Load Current — 200 mA in Standby Mode
- Switchable Current Limits
- Short Circuit Protection
- Thermal Shutdown
- FLT Output
- 50 mA (Typ) Supply Current — 10 nA in Shutdown
- 40 nA (Typ) Switch-Off Leakage



ADM1072 Used In a Portable System



ADM1070 -48V Hot Swap Controller



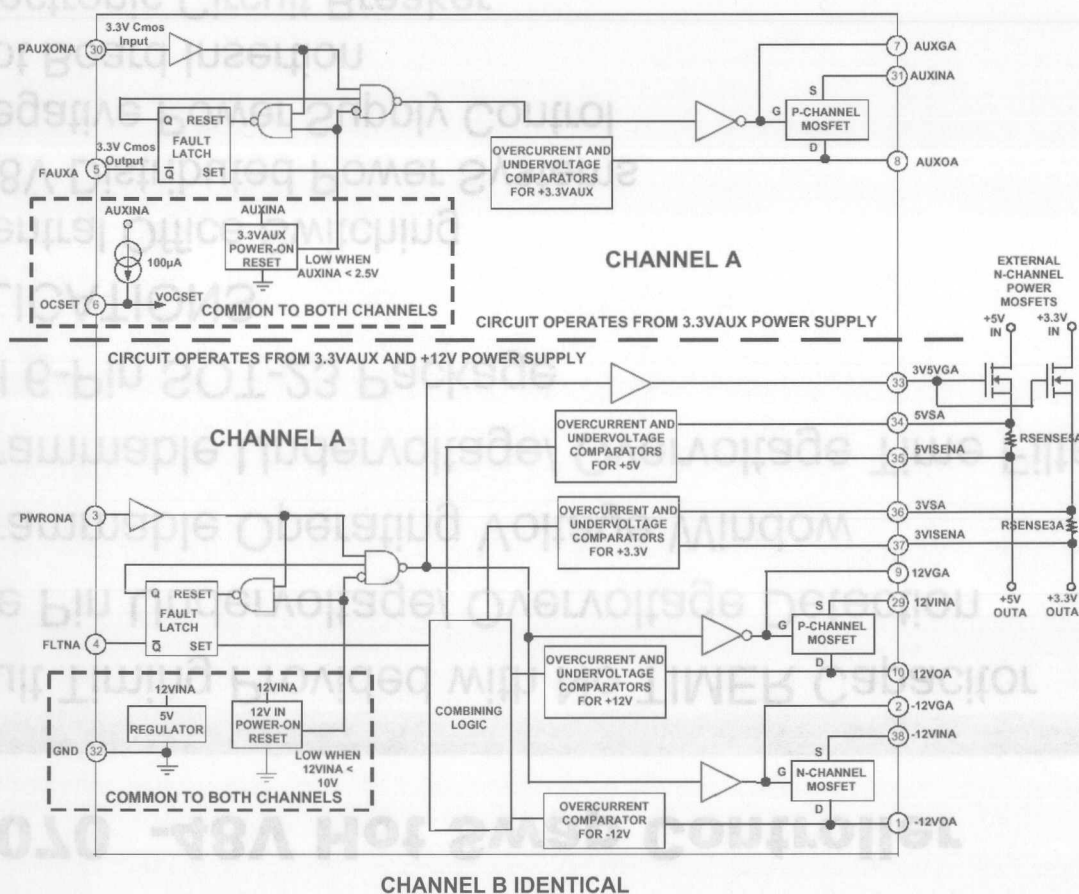
ADM1070 -48V Hot Swap Controller

- Allows Safe Board Insertion and Removal from a Live -48V Backplane
- Typically Operates from -36 V to -80 V
- Tolerates Transients up to -200 V (limited by external components)
- Accurate Programmable Linear Current Limit for Inrush Control and Short Circuit Protection
- Programmable Time-out In Current Limit
- Limited Consecutive Retry:
 - Auto-restart After Current Limit Time-out
 - Shutdown after 7 Consecutive Auto-restarts
 - Provides Immunity from Step Induced Current Spikes

ADM1070 -48V Hot Swap Controller

- Default Timing Provided with No TIMER Capacitor
- Single Pin Undervoltage/ Overvoltage Detection
- Programmable Operating Voltage Window
- Programmable Undervoltage/ Overvoltage Time Filter
- Small 6-Pin SOT-23 Package
- APPLICATIONS
 - Central Office Switching
 - -48V Distributed Power Systems
 - Negative Power Supply Control
 - Hot Board Insertion
 - Electronic Circuit Breaker
 - High Availability Servers
 - Programmable Current Limiting Circuit
 - -48V Power Supply Modules

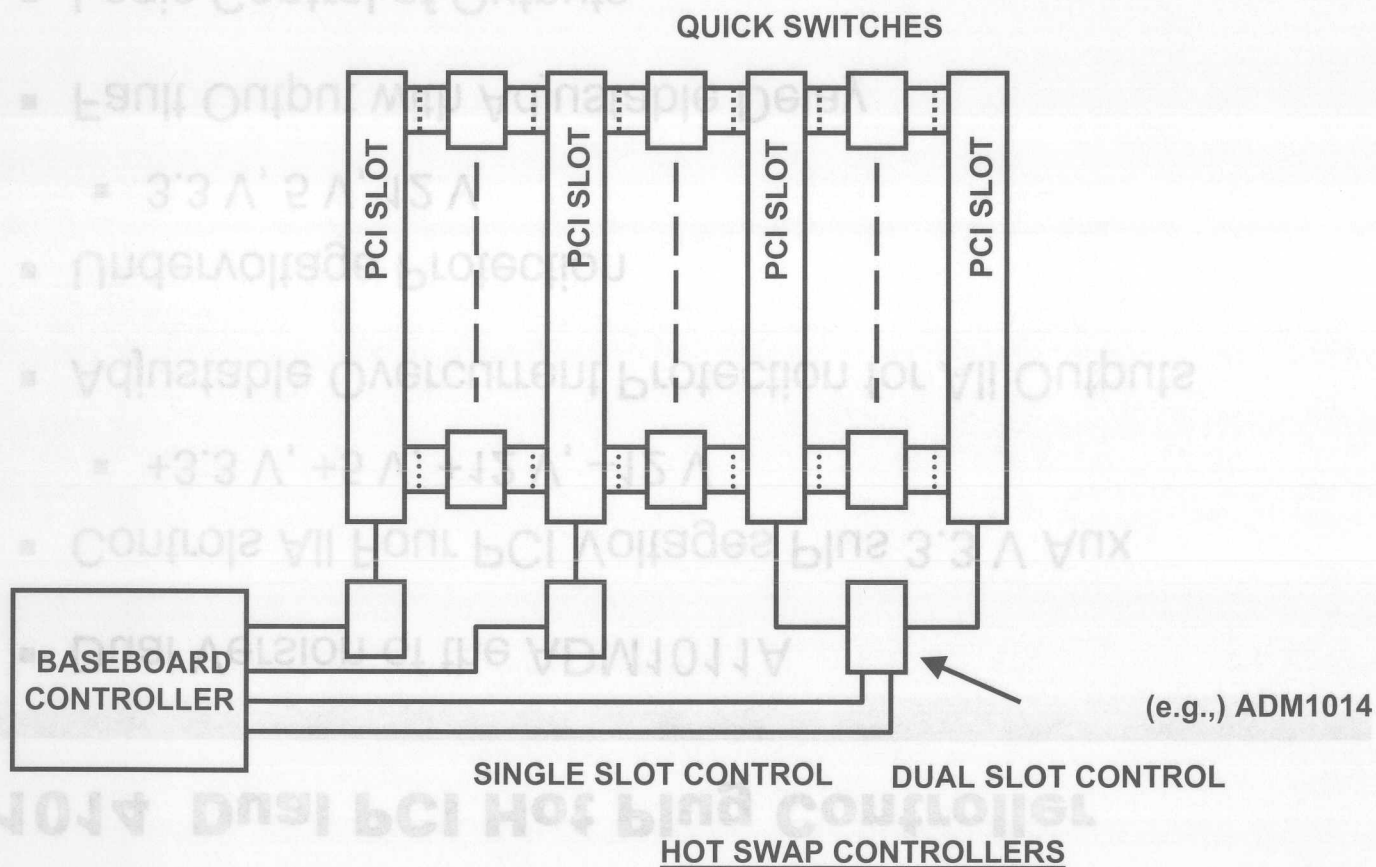
ADM1014 Dual PCI Hot Plug Controller



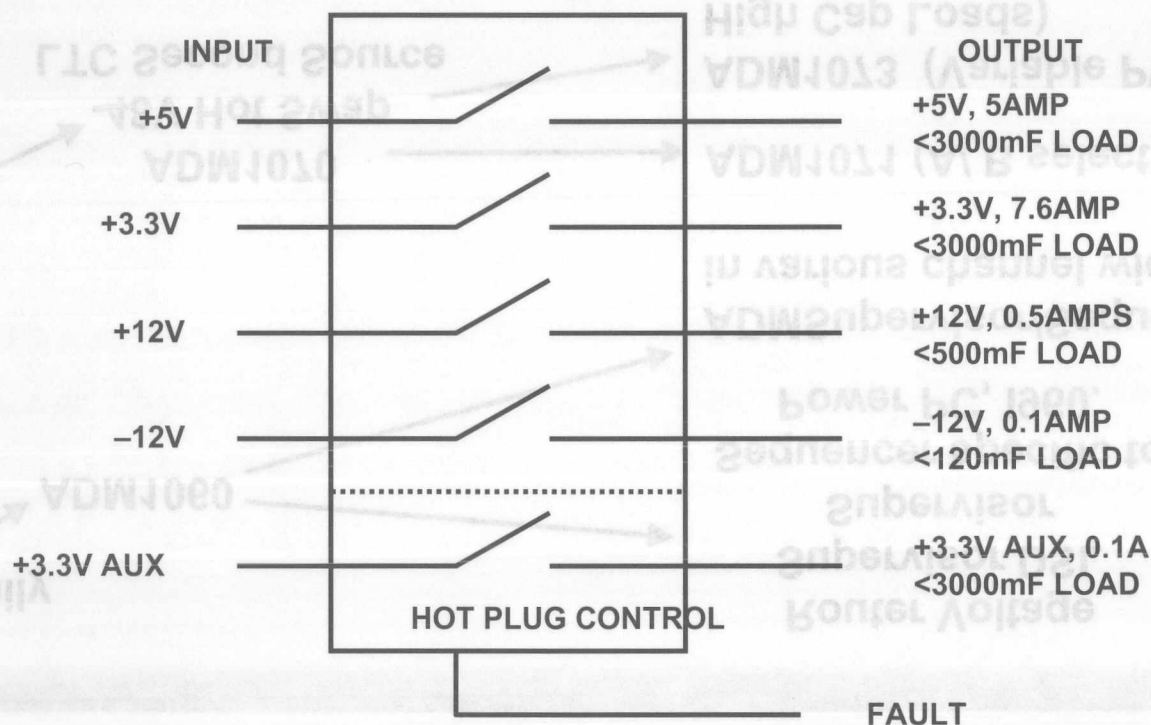
ADM1014 Dual PCI Hot Plug Controller

- Dual Version of the ADM1011A
- Controls All Four PCI Voltages Plus 3.3 V Aux
 - +3.3 V, +5 V, +12 V, -12 V
- Adjustable Overcurrent Protection for All Outputs
- Undervoltage Protection
 - 3.3 V, 5 V, 12 V
- Fault Output with Adjustable Delay
- Logic Control of Outputs
- Adjustable Soft Start

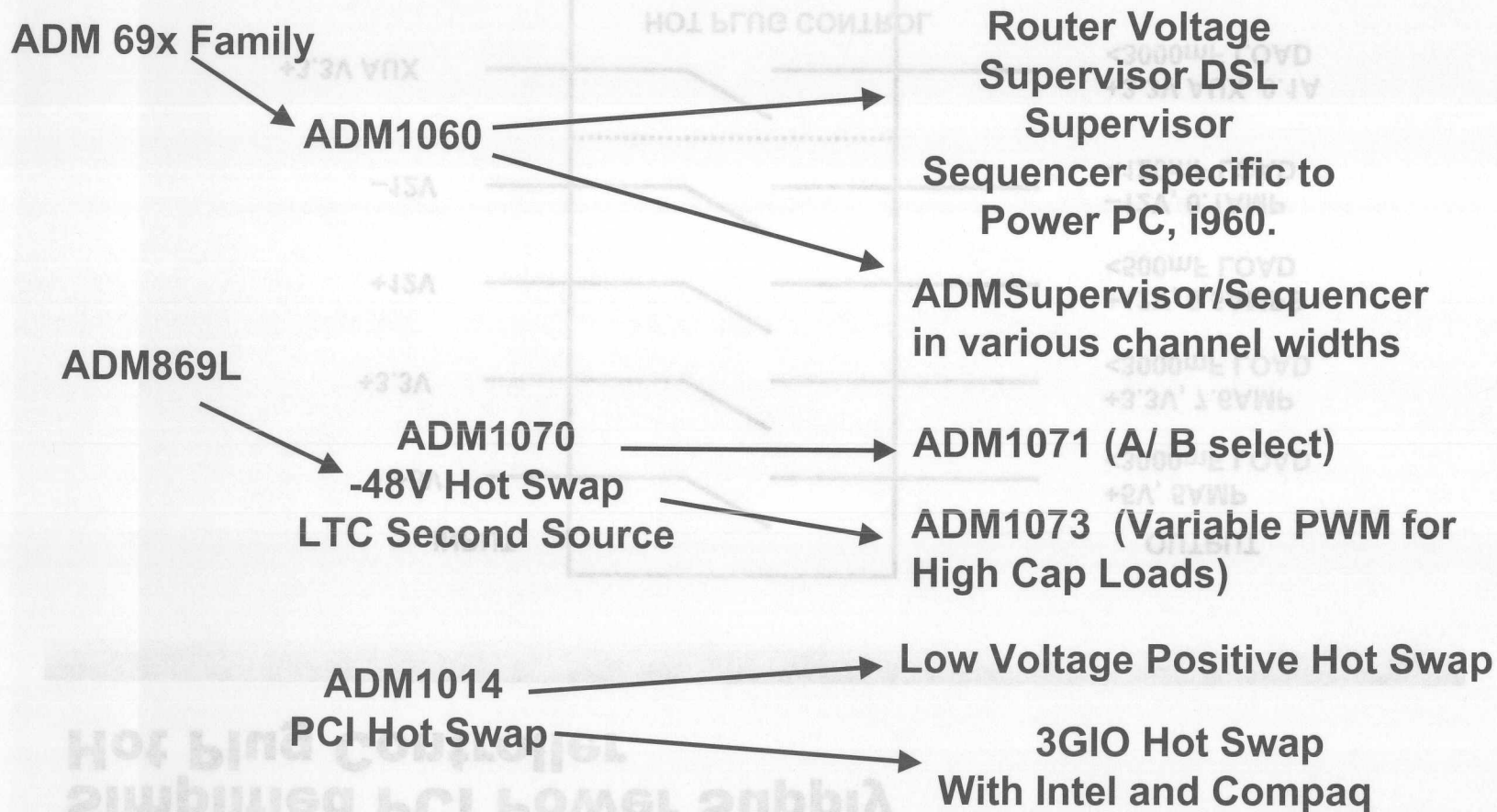
Dual PCI Hot Plug Control



Simplified PCI Power Supply Hot Plug Controller



Hot Swap & Sequencing Roadmap





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REGISTERED DATA

13-34

BUS SWITCHES



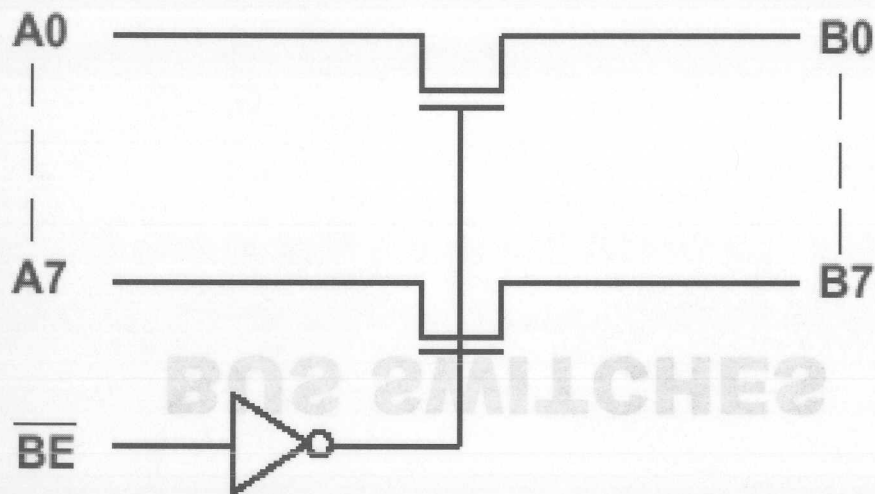
Level Translator, Bus Switch
ADG3542 5.2 V/3.3 V, 8 Bit, 5 Volt



www.analog.com

13-33

ADG3245 2.5 V/3.3 V, 8 Bit, 2 Port Level Translator, Bus Switch



ADG3245 2.5 V/3.3 V, 8 Bit, 2 Port Level Translator, Bus Switch

- 175 ps Propagation Delay through the switch
- 3.5 Ω Switch Connection between Ports
- 2.5 V/ 3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Level Translation
 - 3.3 V to 2.5 V
 - 3.3 V to 1.8 V
 - 2.5 V to 1.8 V
- 20 Lead TSSOP & CSP Packages

ADG3246 2.5 V/ 3.3 V, 10 Bit, 2 Port Level Translator, Bus Switch

• 5.0 V to 1.8 V

• 3.3 V to 1.8 V

• 3.3 V to 5.0 V

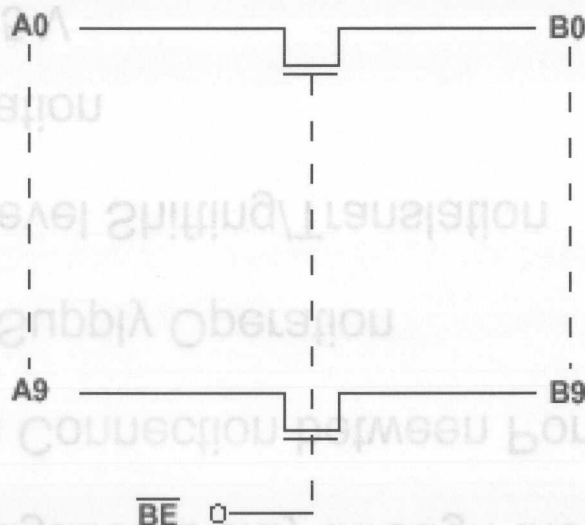
• Level Translation

• Selectable Level Shifting/Translation

• 2.5 V/ 3.3 V Subsystem Operation

• 3.2 Ω Switch Connection between Ports

• 175 ps Propagation Delay through the switch



Level Translator, Bus Switch

ADG3246 2.5 V/ 3.3 V, 10 Bit, 2 Port

ADG3246 2.5 V/ 3.3 V, 10 Bit, 2 Port Level Translator, Bus Switch

- 175 ps Propagation Delay through the switch
- 3.5 Ω Switch Connection between Ports
- 2.5 V/ 3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Level Translation:
 - 3.3 V to 2.5 V
 - 3.3 V to 1.8 V
 - 2.5 V to 1.8 V
- 24 Lead TSSOP and CSP Packages

ADG3247 2.5 V/ 3.3 V, 16 Bit, 2 Port Level Translator, Bus Switch

■ 54 Pins, 1220b, and 25b Packages

■ 2.5 V to 1.8 V
■ 3.3 V to 1.8 V
■ 3.3 V to 2.5 V

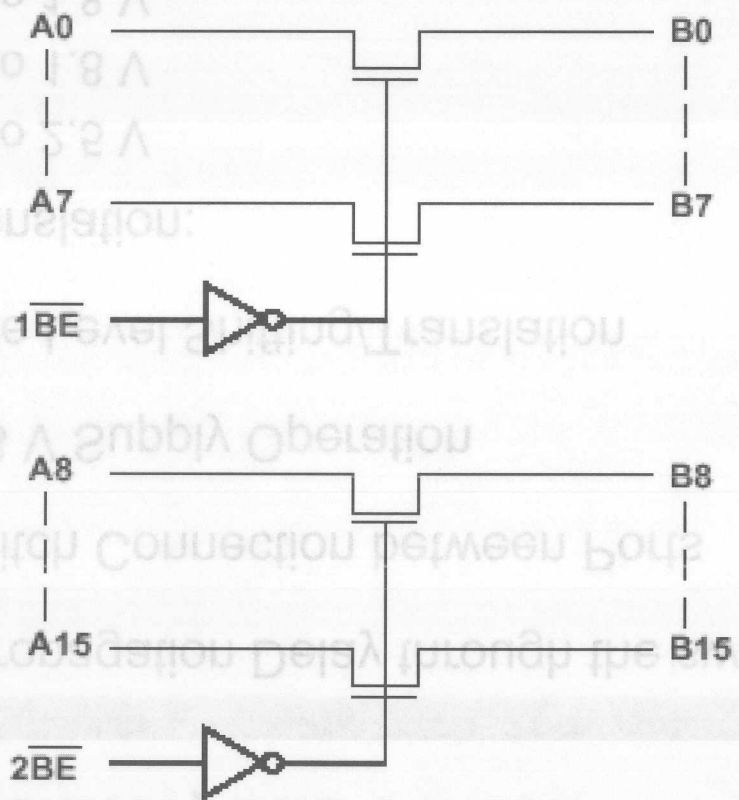
■ Level Translation:

■ Selectable Level and Delay Translation

■ 2.5 V to 3.3 V Supply Operation

■ 3.2 Ω Switch Connection between Ports

■ 175 ps Propagation Delay through the



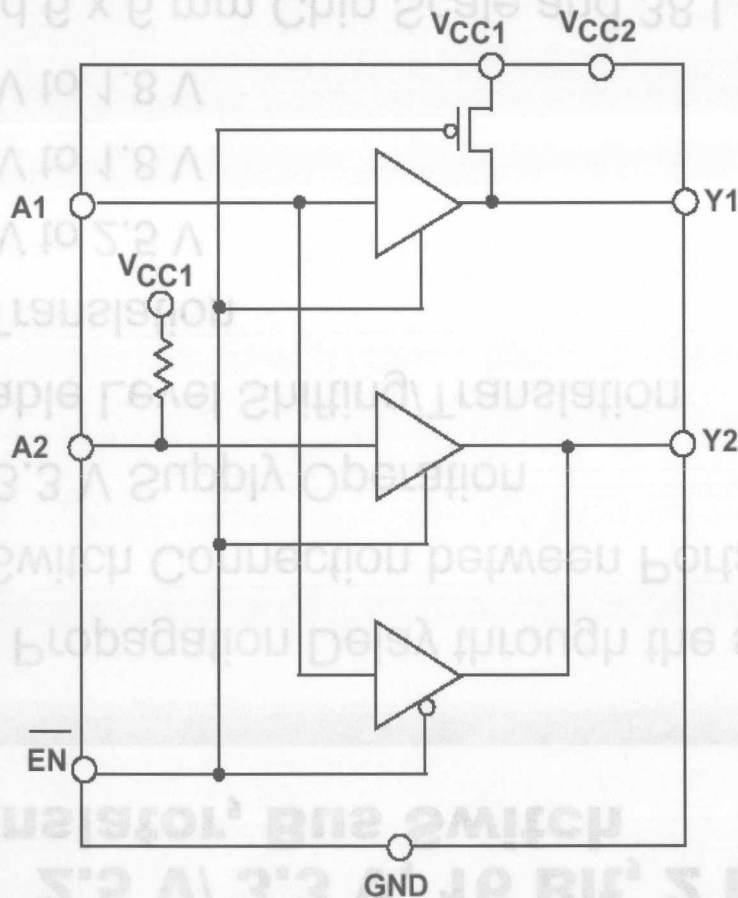
ADG3247 2.5 V/ 3.3 V, 16 Bit, 2 Port Level Translator, Bus Switch

- 175 ps Propagation Delay through the switch
- 3.5 Ω Switch Connection between Ports
- 2.5 V/ 3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Level Translation
 - 3.3 V to 2.5 V
 - 3.3 V to 1.8 V
 - 2.5 V to 1.8 V
- 40 Lead 6 x 6 mm Chip Scale and 38 Lead TSSOP Packages

ADG3233 Low Voltage, Uni-Directional (Up/Down) Level Translation, Bypass Switch

Packages

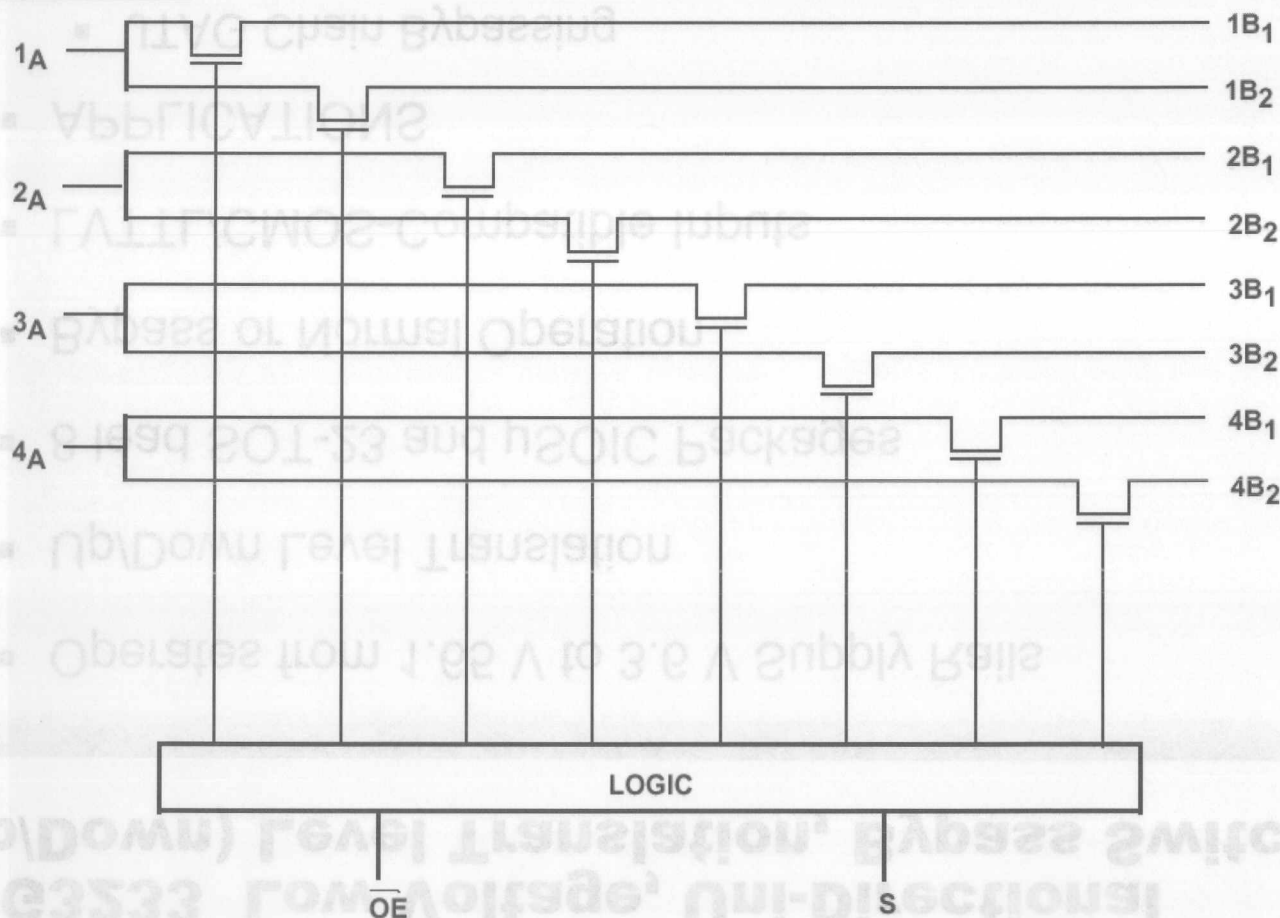
- 40 Lead 8 x 8 mm Chip Scale and 38 Lead TSSOP
- 5.2 V to 1.8 V
- 3.3 V to 1.8 V
- 3.3 V to 5.2 V
- Level Translator
- Selectable Level Shifting Translation
- 5.2 V to 3.3 V Subly Operation
- 3.2 Ω Switch Connection between Ports
- 175 ps Propagation Delay through the switch



ADG3233 Low Voltage, Uni-Directional (Up/Down) Level Translation, Bypass Switch

- Operates from 1.65 V to 3.6 V Supply Rails
- Up/Down Level Translation
- 8 lead SOT-23 and μ SOIC Packages
- Bypass or Normal Operation
- LVTTL/CMOS-Compatible Inputs
- APPLICATIONS
 - JTAG Chain Bypassing
 - Daisychain Bypassing
 - Digital Switching

ADG3257 3.3 V/ 5 V, Quad 2:1 Mux/Demux Bus Switch



ADG3257 3.3 V/ 5 V, Quad 2:1 Mux/Demux Bus Switch

- 110 ps Propagation Delay through the switch
- 2.2 Ω Switches Connect Inputs to Outputs
- Single 3.3 V/ 5 V Supply Operation
- Level Translation Operation
- Ultra Low Quiescent Supply Current (1 nA Typical)
- Rapid 3 ns Switching
- Standard '3257 Type' Pinout
- 16 pin QSOP

- 10 pin QSOB

- Standard 352V Type, Pinout

- Rapid 3 ms Switching

SUPERVISORY CIRCUITS

- Level Translation Operation

- Single 3.3 V 2 V Supply Operation

- 5.5 V Switches Connect Inputs to Outputs

- 110 ps Propagation Delay through the switch

MAXIMUM BUS SWITCH
ADG352V 3.3 V/ 2 V' ONOFF 5:1

ADM6315 Open-Drain Microprocessor Supervisory Circuit in 4-Lead SOT-143

• Pin Compatible with the ADM6312

• Built-in Manual Reset

• Brownout Section Down to $V_{CC} > 1V$

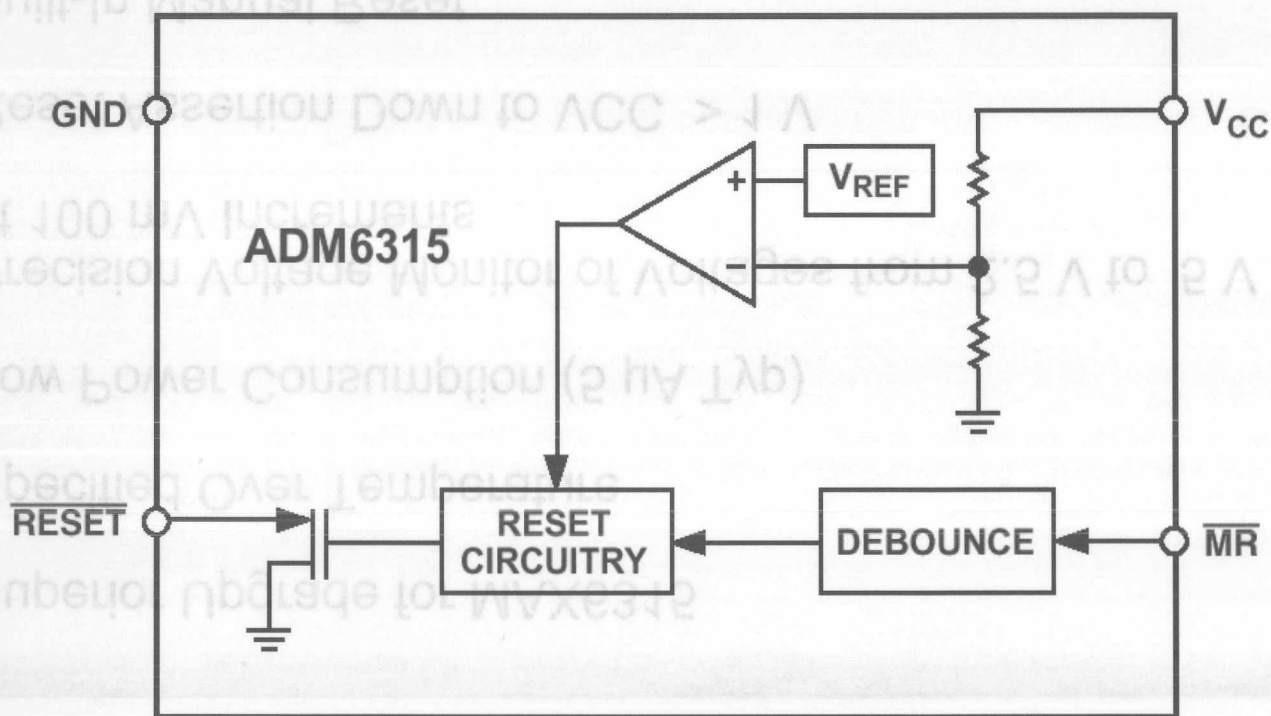
• at 100 nA Increment

• Precision Voltage Monitor of V_{CC} (2.5 V to 5 V)

• Low Power Consumption (2 nA Typ)

• Specified Over Temperature

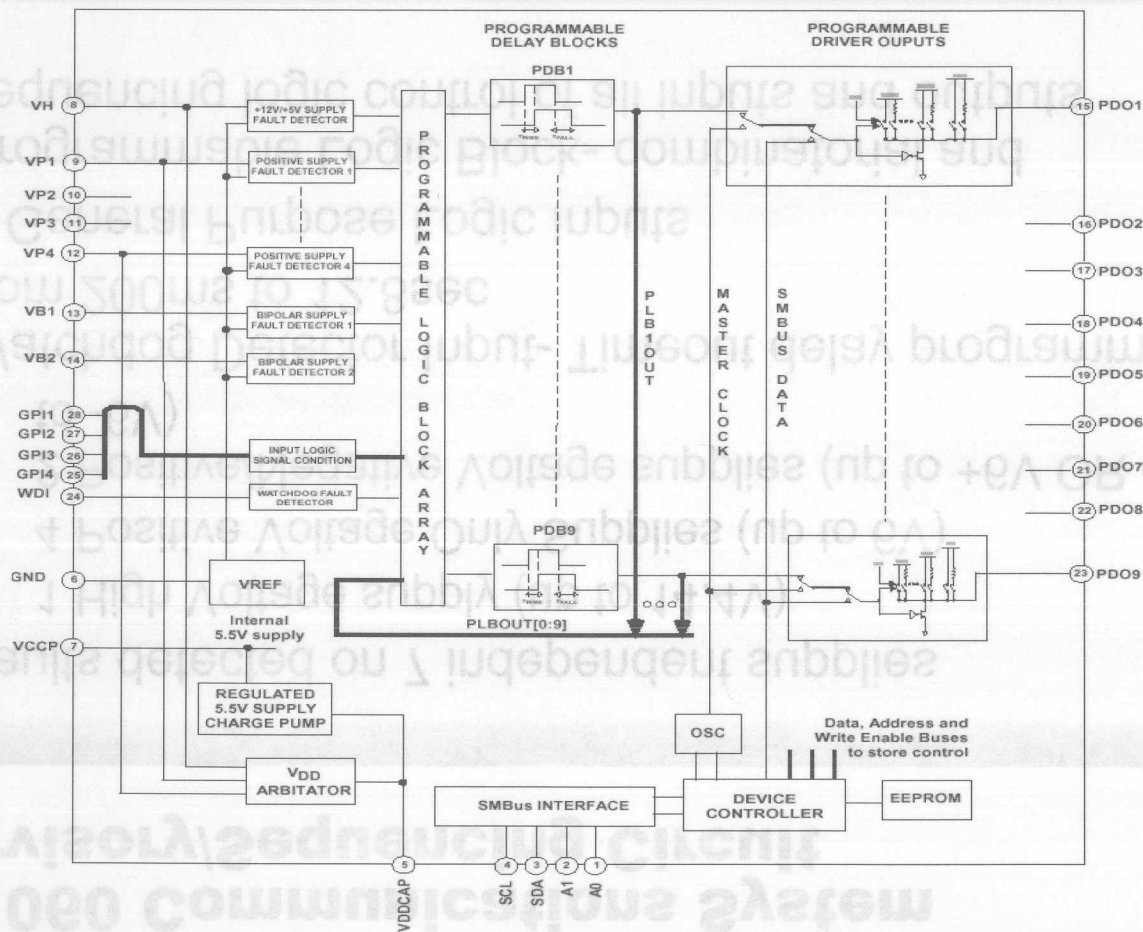
• Subsequent Voltage to V_{CC}



ADM6315 Open-Drain Microprocessor Supervisory Circuit in 4-Lead SOT-143

- Superior Upgrade for MAX6315
- Specified Over Temperature
- Low Power Consumption (5 μ A Typ)
- Precision Voltage Monitor of Voltages from 2.5 V to 5 V at 100 mV Increments
- Reset Assertion Down to $V_{CC} > 1$ V
- Built-In Manual Reset
- Pin Compatible with the ADM811

ADM1060 Communications System Supervisory/Sequencing Circuit



ADM1060 Communications System Supervisory/Sequencing Circuit

- Faults detected on 7 independent supplies
 - 1 High Voltage supply (up to 14.4V)
 - 4 Positive Voltage Only Supplies (up to 6V)
 - 2 Positive/Negative Voltage supplies (up to +6V OR down to -6V)
- Watchdog Detector Input- Timeout delay programmable from 200ms to 12.8sec
- 4 General Purpose Logic Inputs
- Programmable Logic Block- combinatorial and sequencing logic control of all inputs and outputs

supervisory/sequencing circuit
ADM1060 communications system

ADM1060 Communications System Supervisory/Sequencing Circuit

- 9 Programmable Output Drivers
 - Open Collector (external resistor required)
 - Open Collector with internal pull-up to VDD
 - Fast Internal pull-up to VDD
 - Open Collector with internal pull-up to VPn
 - Fast Internal pull-up to VPn
 - Internally charge pumped high drive (for use with external N- channel FETS- PDO's 1 to 4 only)
- EEPROM- 512 Bytes
- Industry Standard 2- Wire Bus Interface (SMBus)

Thermal System Management Products

- Open Collector with internal pull-up to VDD
- Open Collector (external resistor required)
- Programmable Output Drivers

TSM Portfolio Summary

- Local, Remote and Multichannel Remote Digital Temperature Sensors
 - Local - Detect and Measure Temperature
 - Remote - External Sensor is Used to Detect Temperature and is Remotely Sensed and Measured
 - Multichannel Remote – Up to Two External Sensors are Used
 - Note: All Remote Digital Temp Sensors also Provide Local Detection
- Stand Alone and Integrated Solutions
 - Standalone - Measures Temperature
 - Integrated - Combines Local/Remote Temperature Measurement with System Management Features
- Fan Speed Controllers – Linear and PWM
- Serial, PWM, Ratiometric and Trip Point Output Formats

TSM Part Numbers Will Transition to ADT73XX, ADT74XX and ADT75XX

- Temperature Sensors Were Developed by Different Strategies and Therefore the Various Prefixes – AD5XX, AD22XXX, AD7XXX, ADT1X, ADM10XX, TMPXX. ADT Was Reserved for Temperature Sensors
- With the Exception of Next Generation PWM Devices (ie TMP03/04) Future TSM Products Will Use the Following Part Numbering Format:
 - ADT73XX
 - ADT74XX
 - ADT75XX
- IIA Will Continue to Support AD5XX and AD22XXX Linear and Controller Sensors

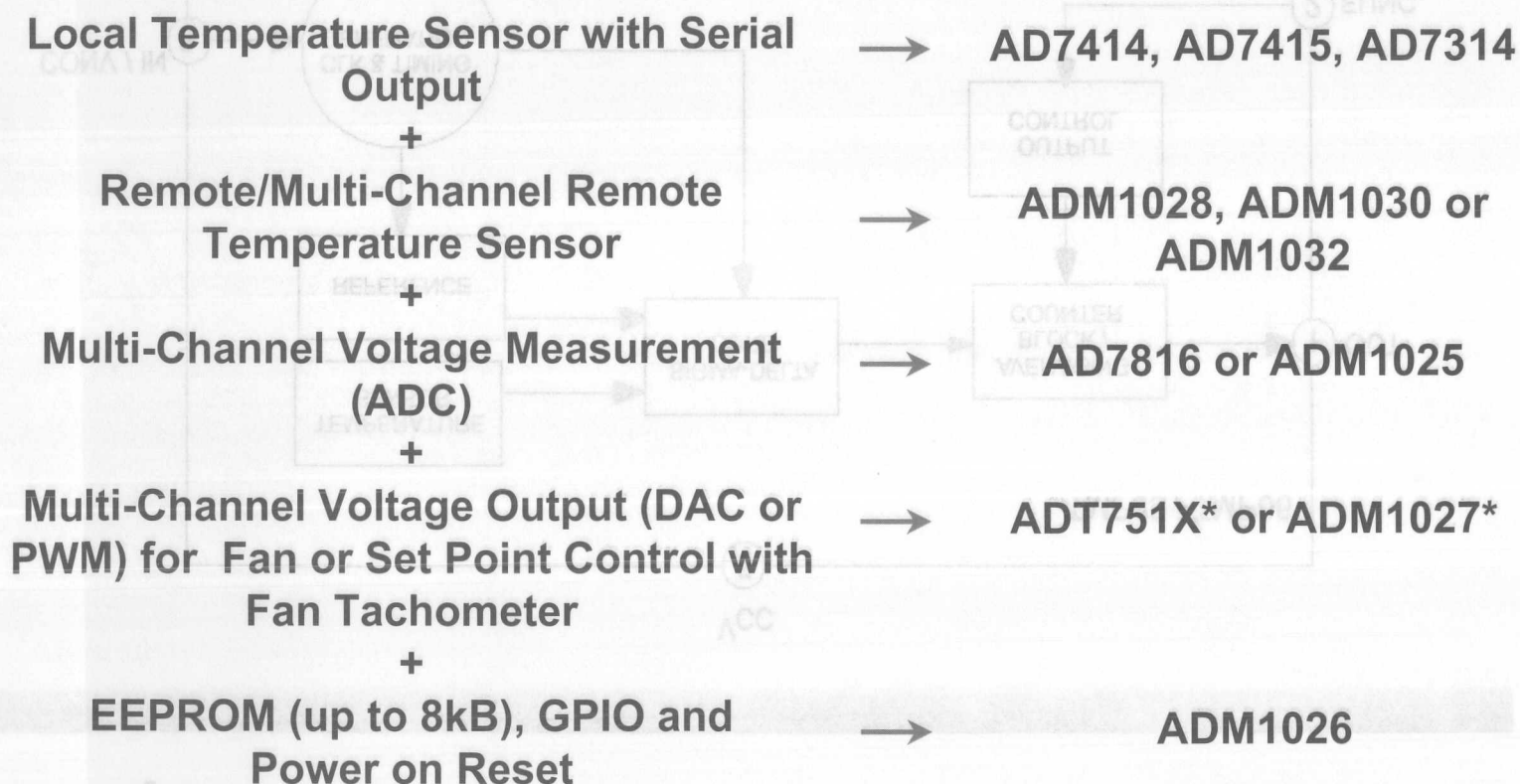
TSM Competitive Advantage Summary

- Integrated Feature Set – Thermal Sensors are Typically a Subset of a Larger System Management Architecture
- Temperature Accuracy Guaranteed Over Power Supply Tolerance and Wide Temperature Ranges
- Closed Loop Automatic Fan Speed Control – Reduces Acoustic Pollution
- Standard Interfaces – Competitive 1-Wire Solutions are Proprietary and Therefore Not Recommended for High Availability Designs
- ADI Market Leadership in Data Converters – Core of Digital Temperature Sensors
- Design In Tools – Evaluation Boards, Demo Software are Rated Industry Best for Ease of Use for Design In Confirmation

Feature Set Expansion Supports All System Management Applications

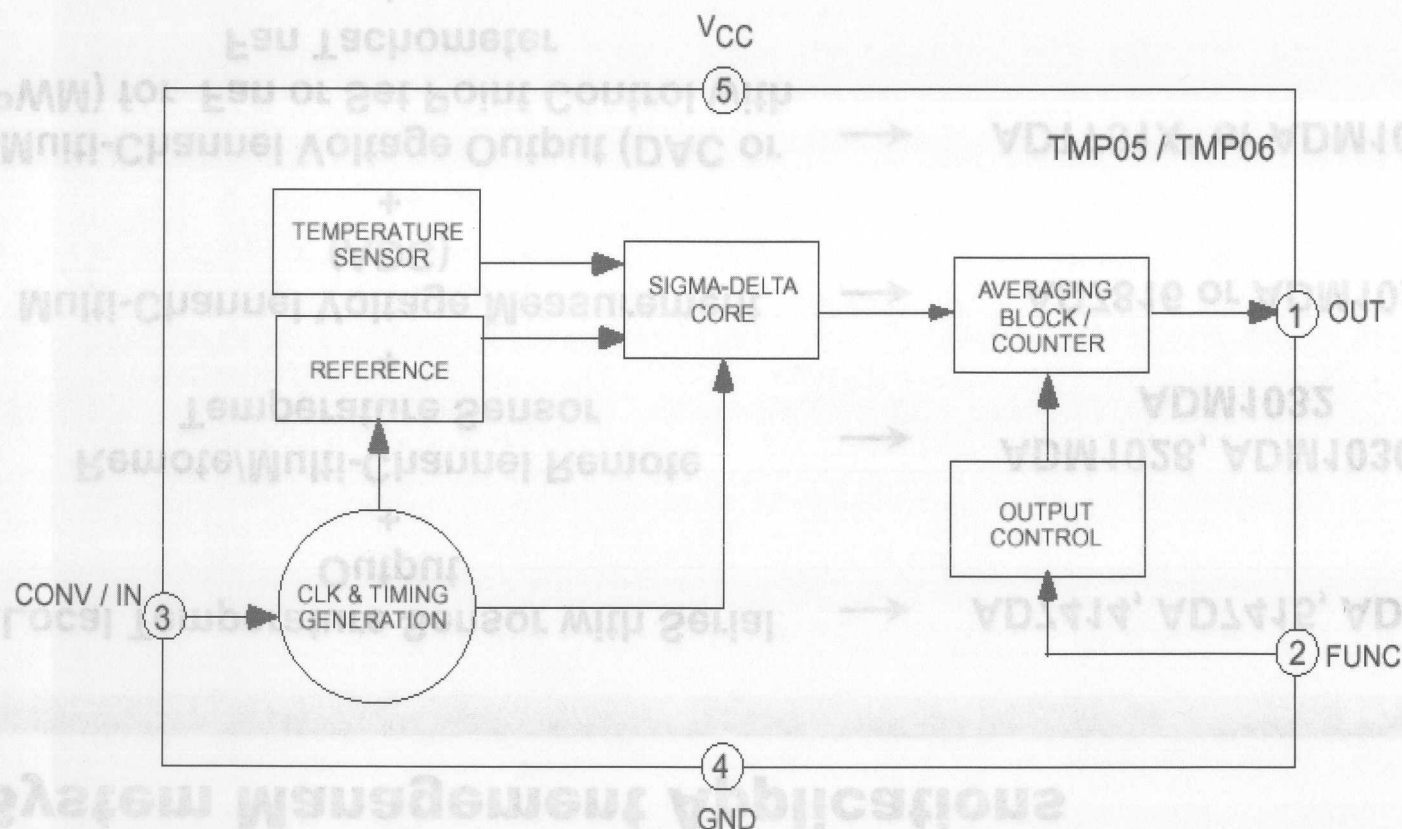
Local Temperature Sensor with Serial Output	→	One Thermal Zone
+		
Remote/Multi-Channel Remote Temperature Sensor	→	Up to Three Thermal Zones
+		
Multi-Channel Voltage Measurement (ADC)	→	Voltage Monitoring with Programmable Upper/Lower Limit Windowing
+		
Multi-Channel Voltage Output (DAC or PWM) for Fan or Set Point Control with Fan Tachometer	→	Hardware Closed Loop Control
+		
EEPROM (up to 8kB), GPIO and Power on Reset	→	Stores System Configuration Status or Variables, Spare GPIO Always Needed, POR For Hard System Reset
+		
Current Monitoring	→	Power Supply Load Monitoring and 240VI Safety

Feature Set Expansion Supports All System Management Applications



* New Products

TMP05/06 Serial Digital Output Temperature Sensor



TMP05/06 Serial Digital Output Temperature Sensor

- Small Low Cost 5-Pin SC-70 and SOT-23 Packages.
- Modulated Serial Digital Output Proportional to Temperature
- $\pm 1^\circ \text{C}$ Accuracy from 25°C to 100°C
- $\pm 3^\circ \text{C}$ over entire temperature range
- Operation from -55°C to 125°C
- Operation from 2.7 V to 5.5 V
- CMOS/TTL-Compatible Output on TMP05
- Flexible Open Drain output on TMP06

Digital Temperature Sensors

RELEASED

AD7414 SOT 6-pin (I2C/SMBus) with Alert

AD7415 SOT 5-pin (I2C/SMBus)

AD7314 μ SO-8 (SPI) Equiv to Dallas 1722

COMING

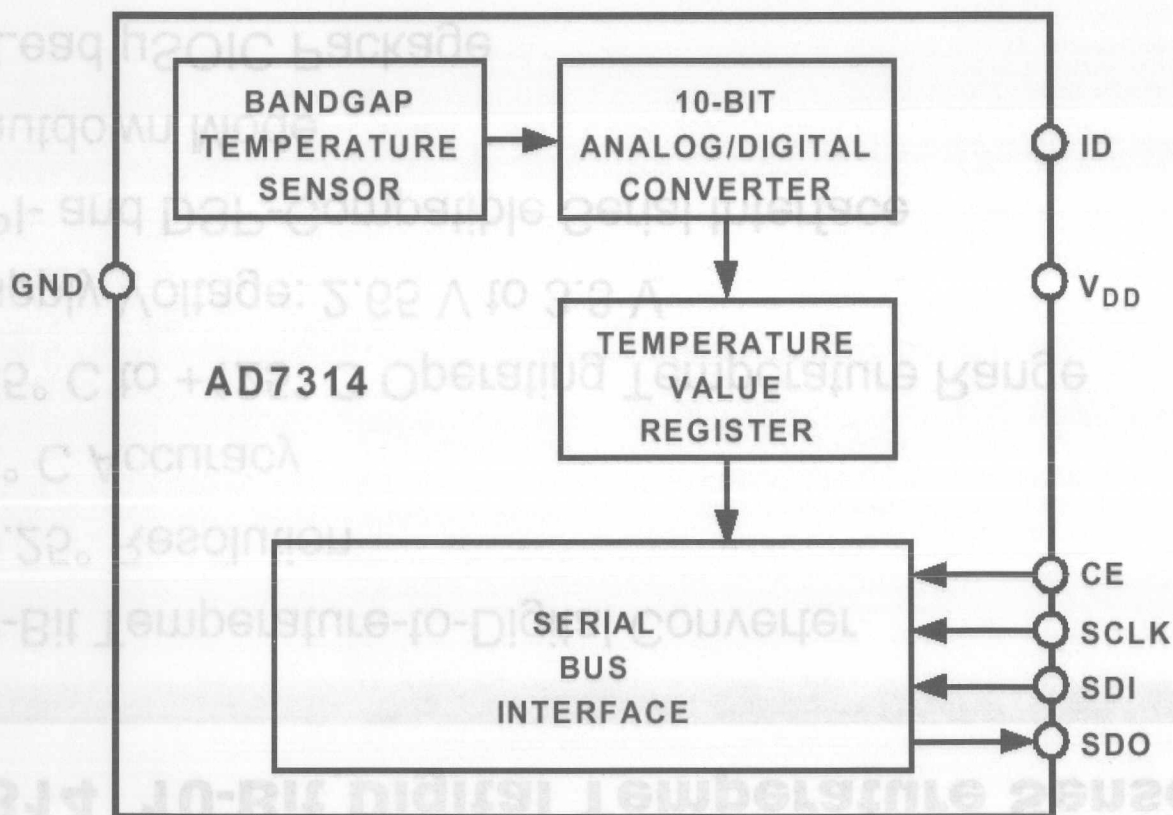
ADT7316/7/8 Temp Sensor + Quad DAC (I2C/SMBus)

ADT7411 Temp Sensor +8 Chnl ADC (I2C/SMBus)

ADT7516/7/8 Temp Sensor + Quad DAC + ADC (4Chnls)
(I2C/SMBus)

ADT7301 $\pm 0.5^\circ$ Accurate Temp Sensor (SPI)
(Pin Compatible with the AD7814)

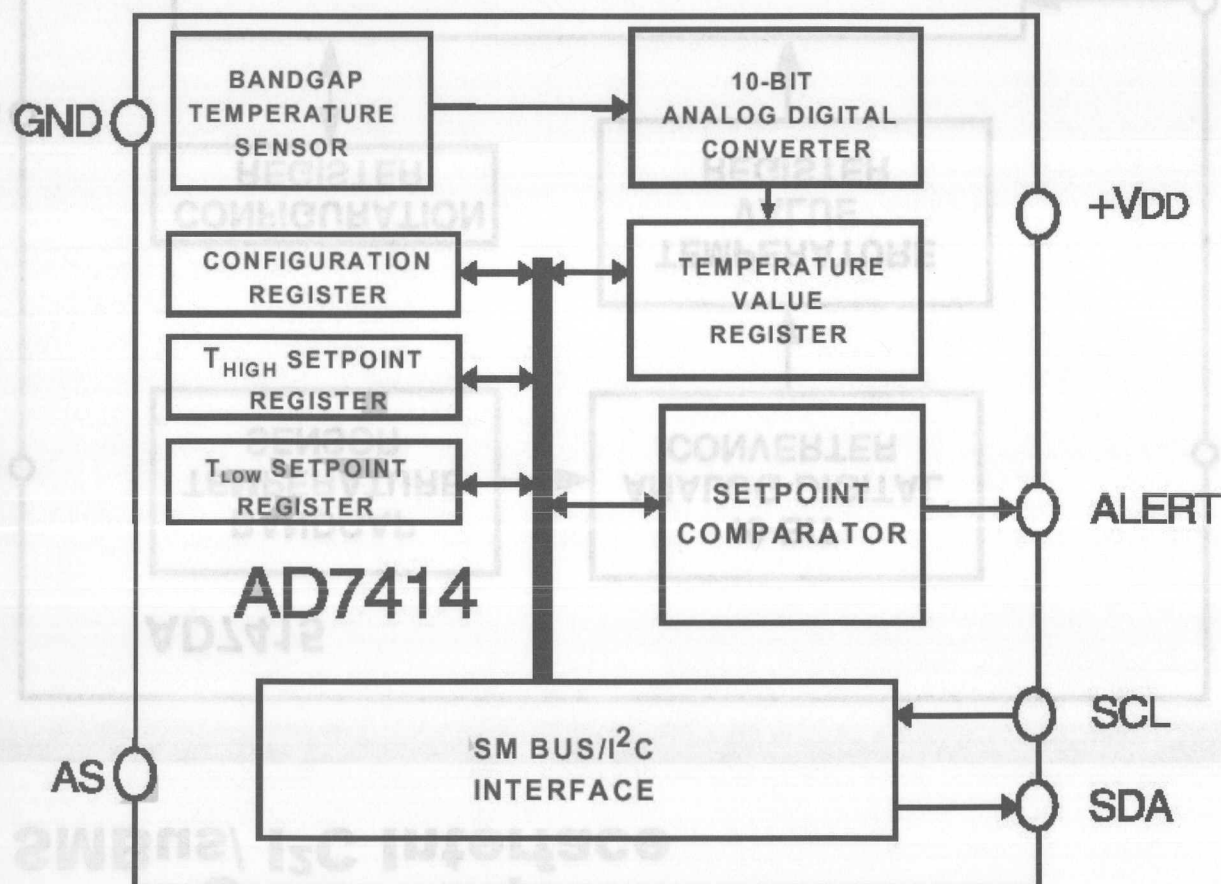
AD7314 10-Bit Digital Temperature Sensor



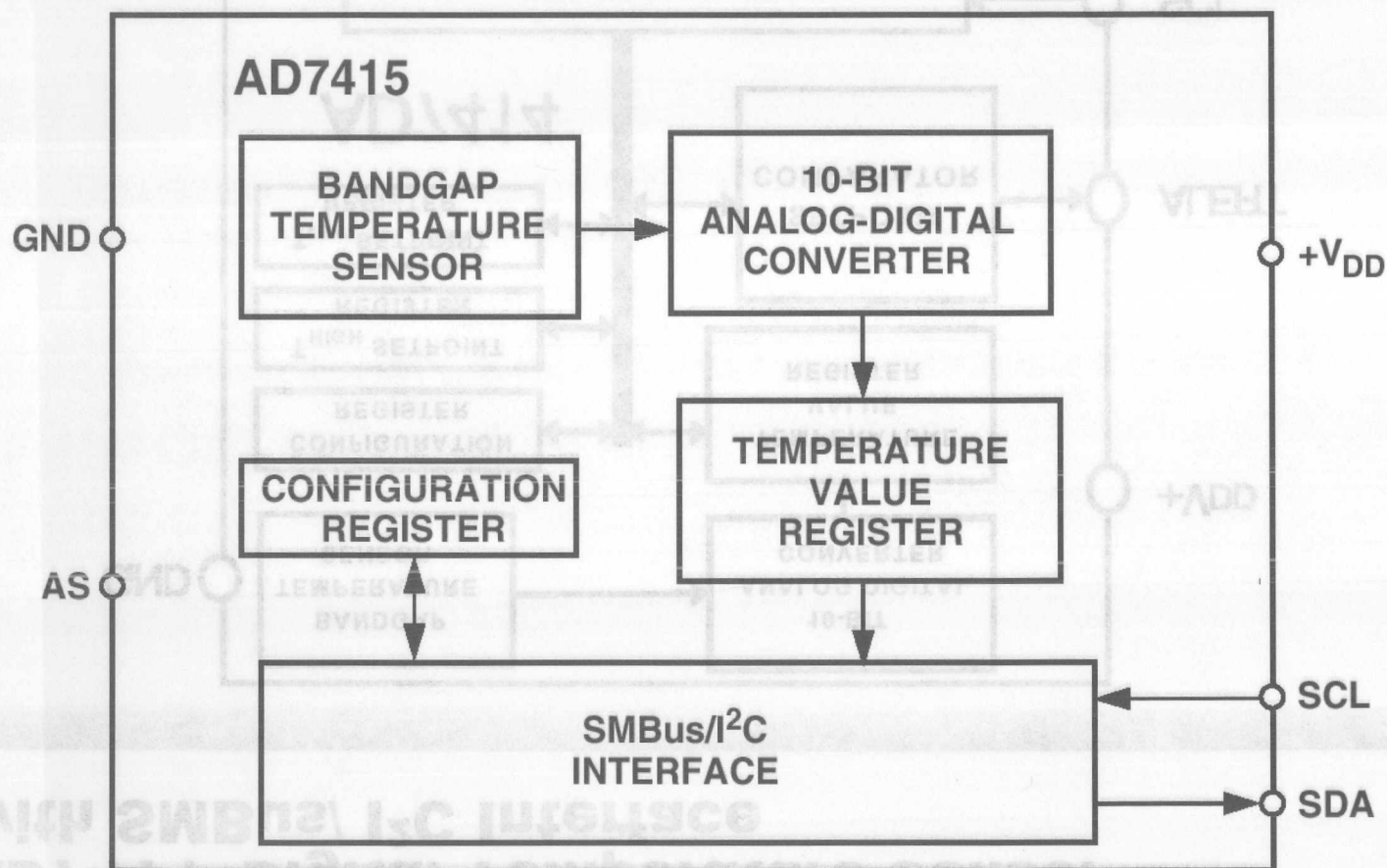
AD7314 10-Bit Digital Temperature Sensor

- 10-Bit Temperature-to-Digital Converter
- $\pm 0.25^\circ$ Resolution
- $\pm 2^\circ$ C Accuracy
- -55° C to $+125^\circ$ C Operating Temperature Range
- Supply Voltage: 2.65 V to 3.3 V
- SPI- and DSP-Compatible Serial Interface
- Shutdown Mode
- 8-Lead μ SOIC Package
- For Primary SPI Temperature Sensor Designs use the AD7814

AD7414 Digital Temperature Sensor with SMBus/ I²C Interface



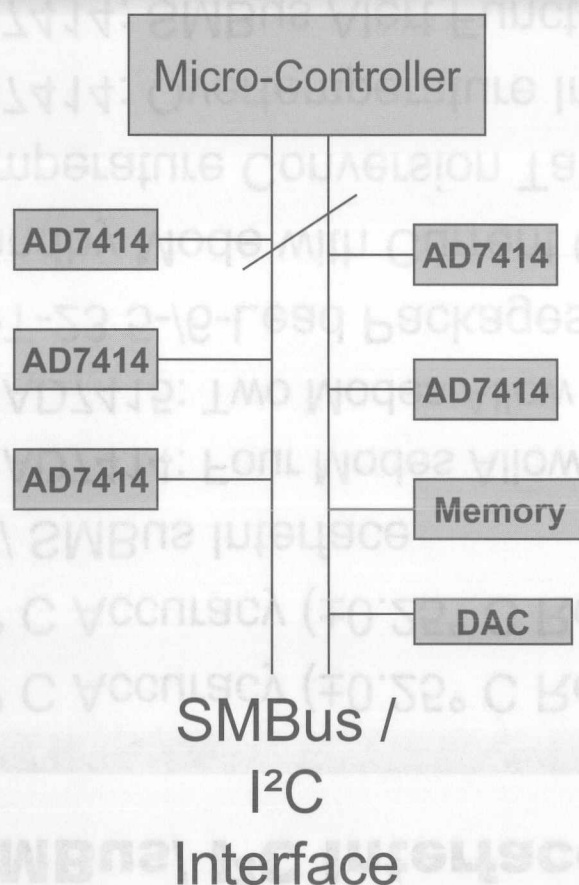
AD7415 Digital Temperature Sensor with SMBus/ I²C Interface



AD7414/15 Digital Temperature Sensors with SMBus/ I²C Interface

- $\pm 2^{\circ}\text{C}$ Accuracy ($\pm 0.25^{\circ}\text{C}$ Resolution) @ 3.3 V
- $\pm 3^{\circ}\text{C}$ Accuracy ($\pm 0.25^{\circ}\text{C}$ Resolution) @ 5.5 V
- I²C/ SMBus Interface
 - AD7414: Four Modes Allow 8 I²C Addresses
 - AD7415: Two Modes Allow 6 I²C Addresses
- SOT-23 5-/6-Lead Packages
- Standby Mode with Current Consumption of 3 mA
- Temperature Conversion Takes 28 ms (Typ)
- AD7414: Overtemperature Indication
- AD7414: SMBus Alert Function
- Only One Grade
 - -55°C to $+125^{\circ}\text{C}$ Operating Temperature Range

AD7414/15 10-Bit Temperature Sensors



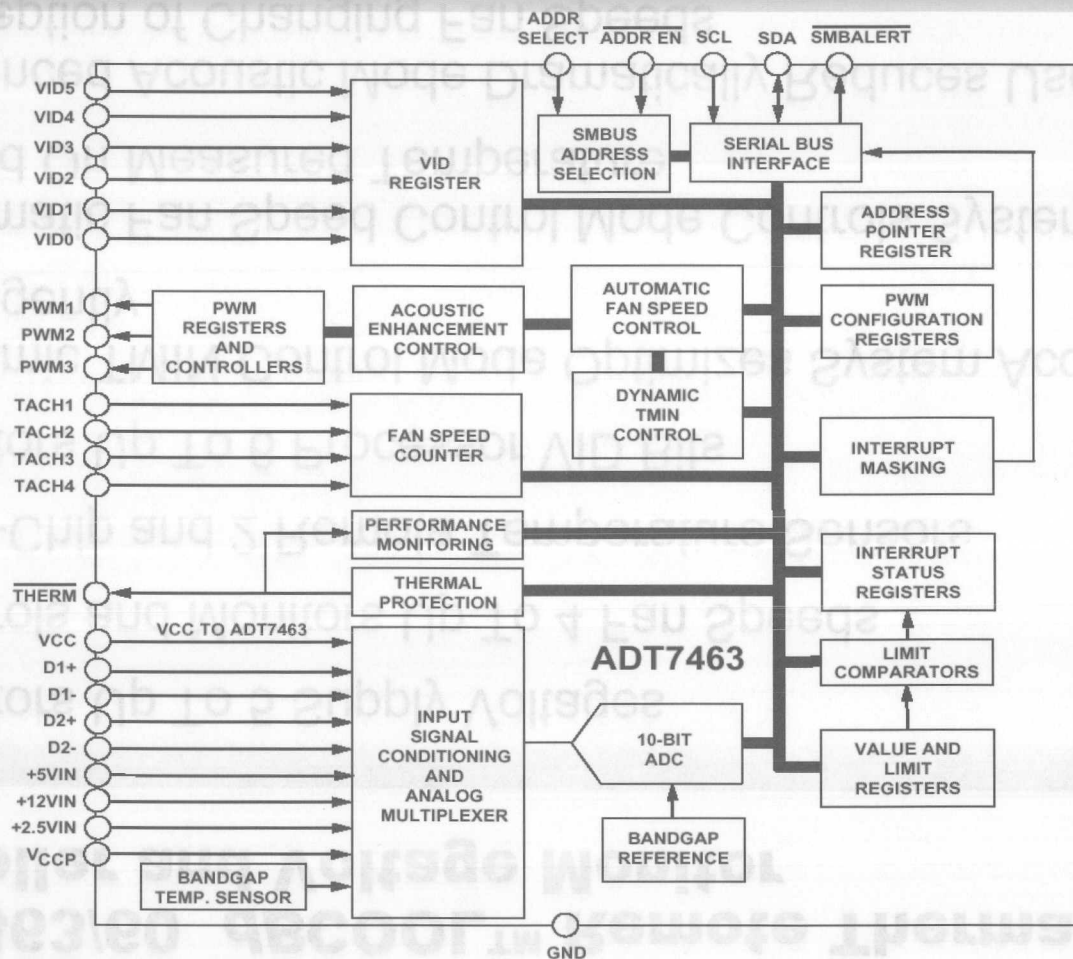
■ AD7414

- 8 Address Options
- Possible of 8 AD7414's maybe connected on the same bus

■ AD7415

- 6 Address Options
- Possible of 6 AD7415's may be connected on the same bus

ADT7463/60 dBCOOL™ Remote Thermal Controller and Voltage Monitor



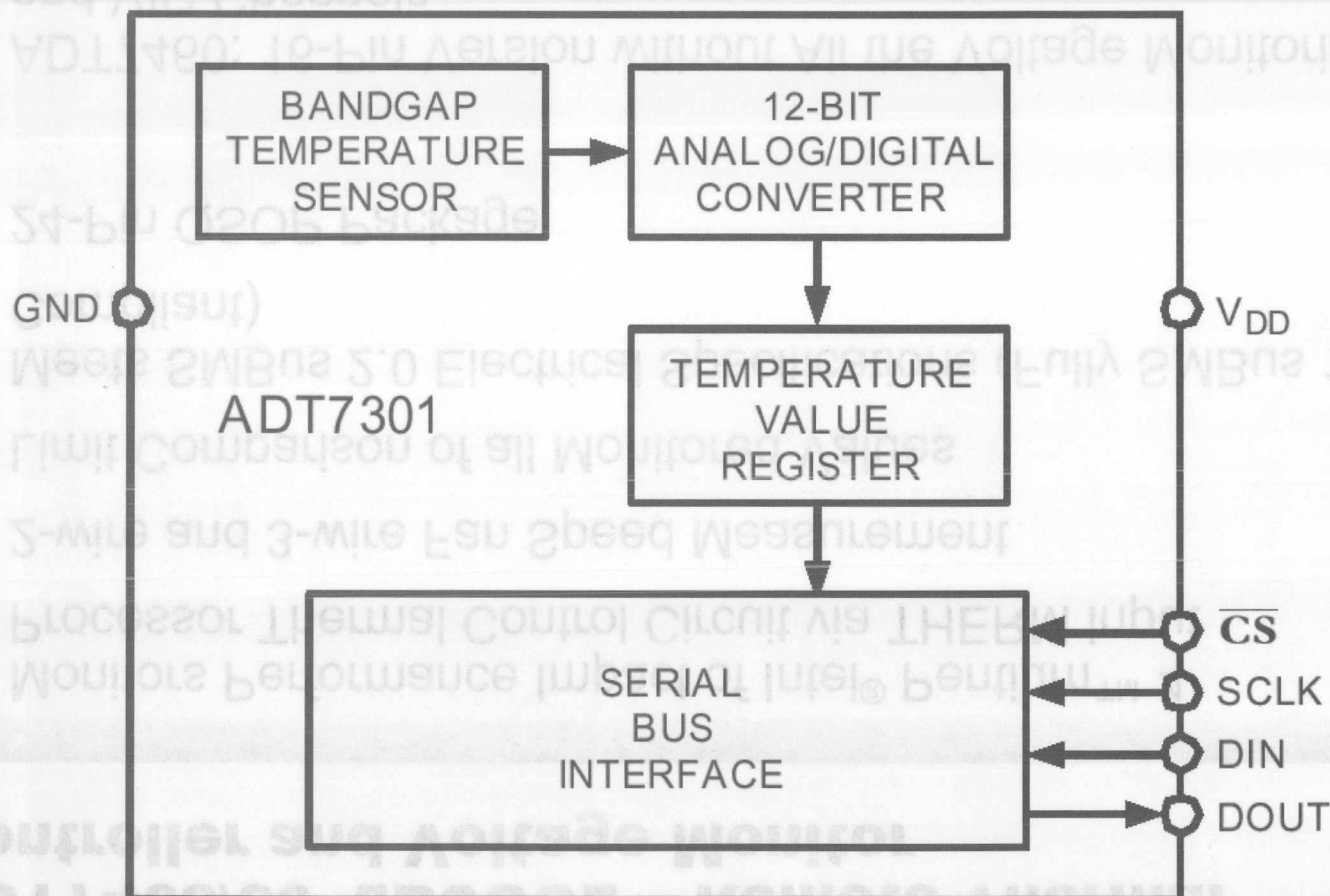
ADT7463/60 *dBCOOL™* Remote Thermal Controller and Voltage Monitor

- Monitors Up To 5 Supply Voltages
- Controls and Monitors Up To 4 Fan Speeds
- 1 On-Chip and 2 Remote Temperature Sensors
- Monitors Up To 6 Processor VID Bits
- Dynamic TMIN Control Mode Optimizes System Acoustics Intelligently
- Automatic Fan Speed Control Mode Controls System Cooling Based On Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection feature via THERM output

ADT7463/60 dBCOOL™ Remote Thermal Controller and Voltage Monitor

- Monitors Performance Impact of Intel® Pentium™ 4 Processor Thermal Control Circuit via THERM input
- 2-wire and 3-wire Fan Speed Measurement
- Limit Comparison of all Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- 24-Pin QSOP Package
- ADT7460: 16-Pin Version without All the Voltage Monitoring and VID Channels

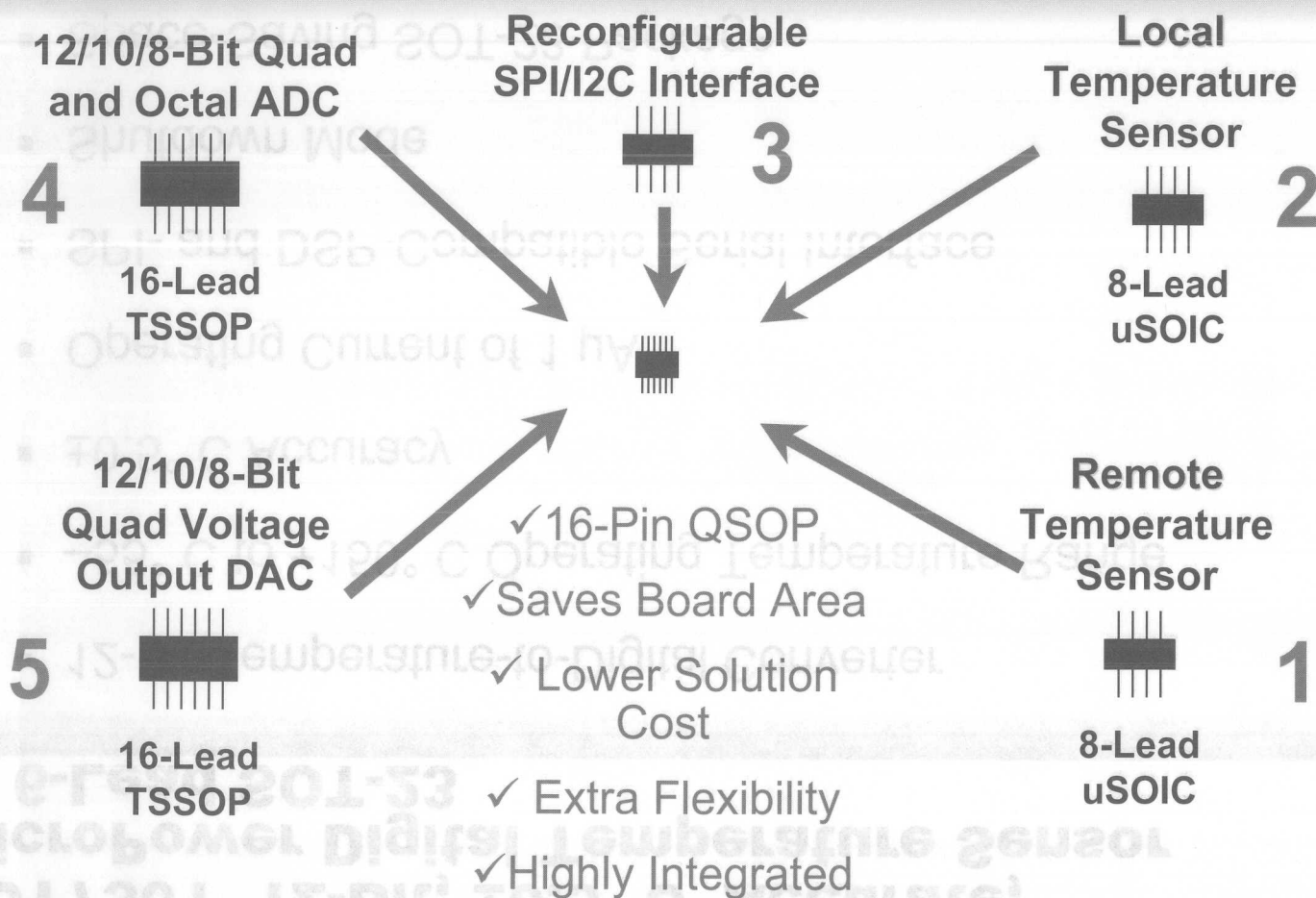
ADT7301 12-Bit, $\pm 0.5^{\circ}\text{C}$ Accurate, MicroPower Digital Temperature Sensor in 6-Lead SOT-23



ADT7301 12-Bit, $\pm 0.5^{\circ}\text{C}$ Accurate, MicroPower Digital Temperature Sensor in 6-Lead SOT-23

- 12-Bit Temperature-to-Digital Converter
- -55°C to $+150^{\circ}\text{C}$ Operating Temperature Range
- $\pm 0.5^{\circ}\text{C}$ Accuracy
- Operating Current of $1\ \mu\text{A}$
- SPI- and DSP-Compatible Serial Interface
- Shutdown Mode
- Space-Saving SOT-23 Package

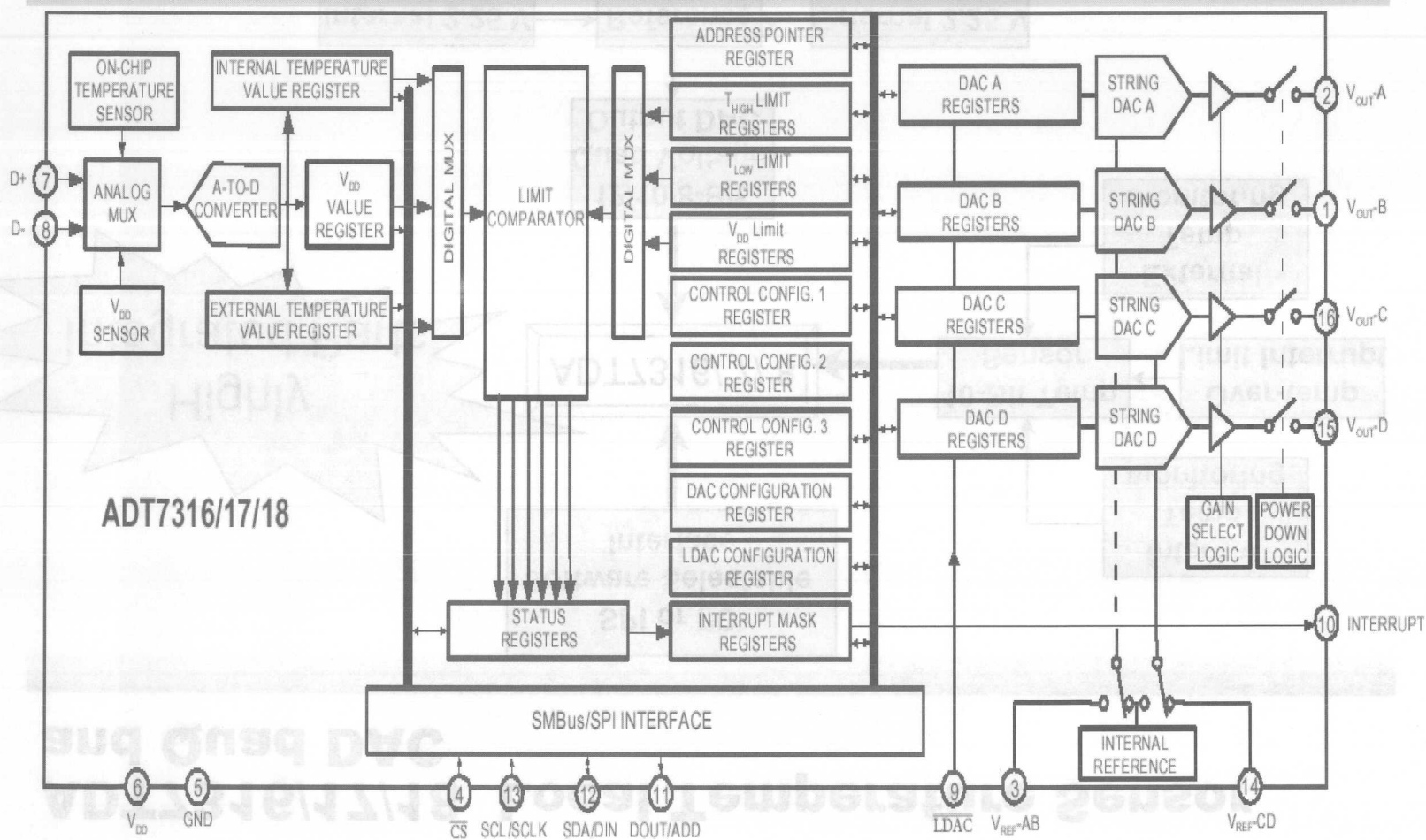
New Family of Digital Temperature Sensors with Multiple ADC and DAC Channels and a Flexible Serial Interface





All this functionality is packed into a 16-Lead QSOP

ADT7316/17/18 10-Bit Digital Temperature Sensor and Quad 12-/10-/8-Bit DAC



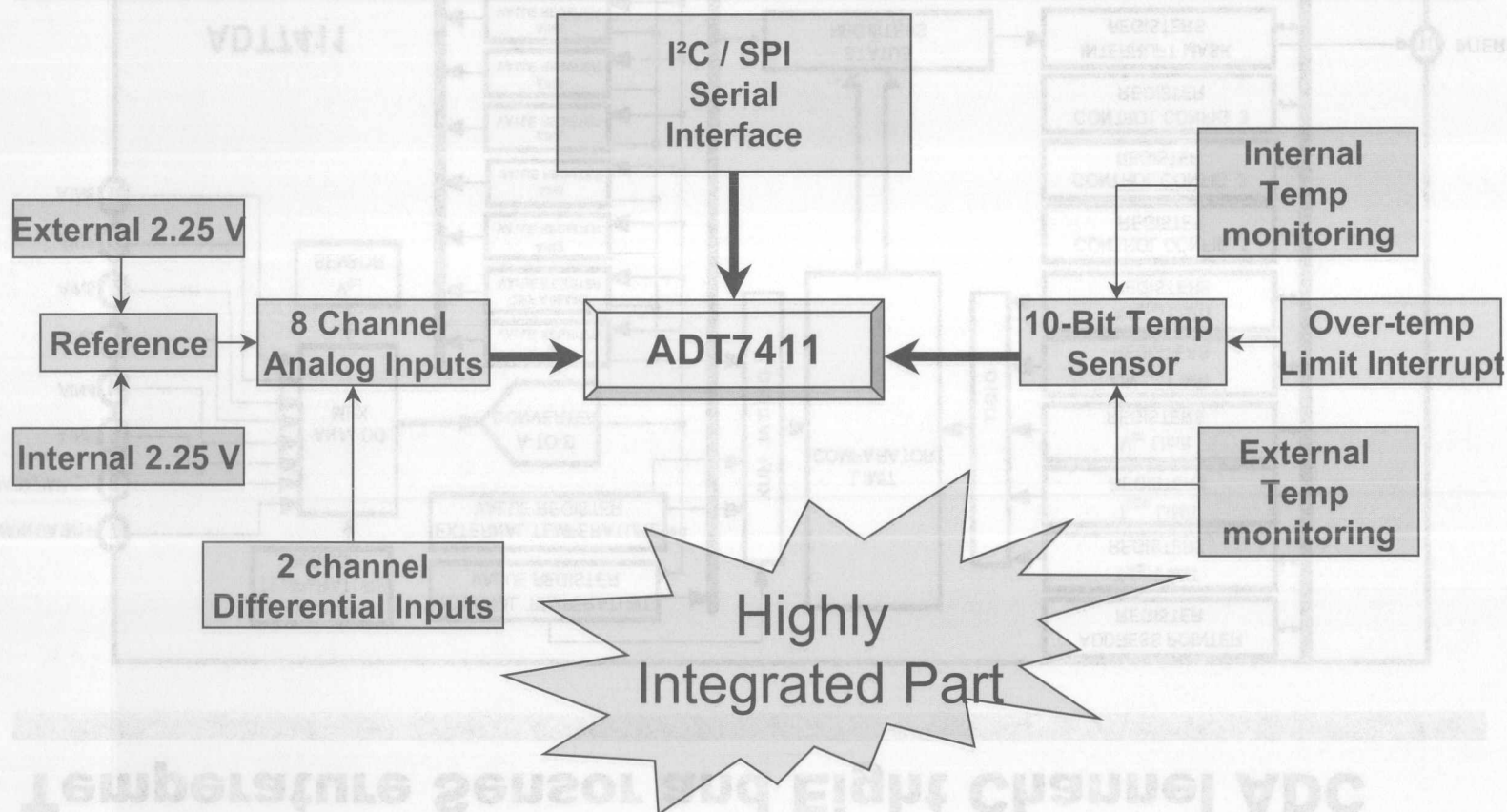
ADT7316/17/18 10-Bit Digital Temperature Sensor and Quad 12-/10-/8-Bit DAC

- ADT7316 — Four 12-Bit DACs
- ADT7317 — Four 10-Bit DACs
- ADT7318 — Four 8-Bit DACs
- Buffered Voltage Output
- Guaranteed Monotonic by Design Over All Codes
- 10-Bit Temperature to Digital Converter
- Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Temperature Sensor Accuracy of $\pm 2^{\circ}\text{C}$
- Supply Range: 2.7 V to 5.5 V
- DAC Output Range: 0 - V_{REF}

ADT7316/17/18 10-Bit Digital Temperature Sensor and Quad 12-/10-/8-Bit DAC

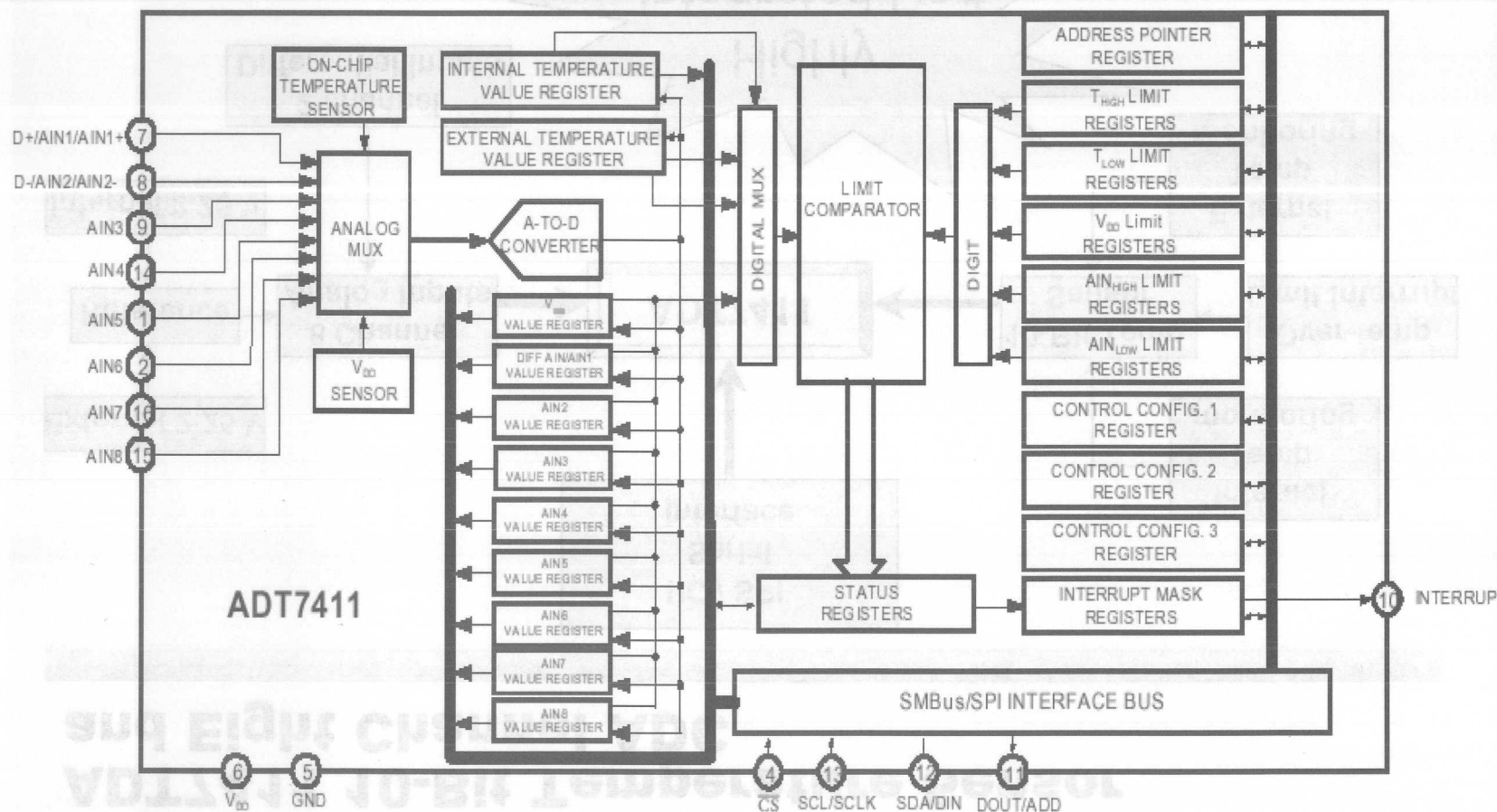
- Power-Down Current 1 μ A
- Double-Buffered Input Logic
- Internal 2.25 V_{REF} Option
- Buffered/Unbuffered Reference Input Option
- Power-On Reset to Zero Volts
- Simultaneous Update of Outputs (Function)
- On-Chip Rail-to-Rail Output Buffer Amplifier
- I²C, SPI, QSPI, MICROWIRE, and DSP-Compatible 5-Wire Serial Interface
- 16-Lead QSOP Package

ADT7411 10-Bit Temperature Sensor and Eight Channel ADC



All this functionality is packed into a 16-Lead QSOP

ADT7411 SPI/I²C® Compatible, 10-Bit Digital Temperature Sensor and Eight Channel ADC



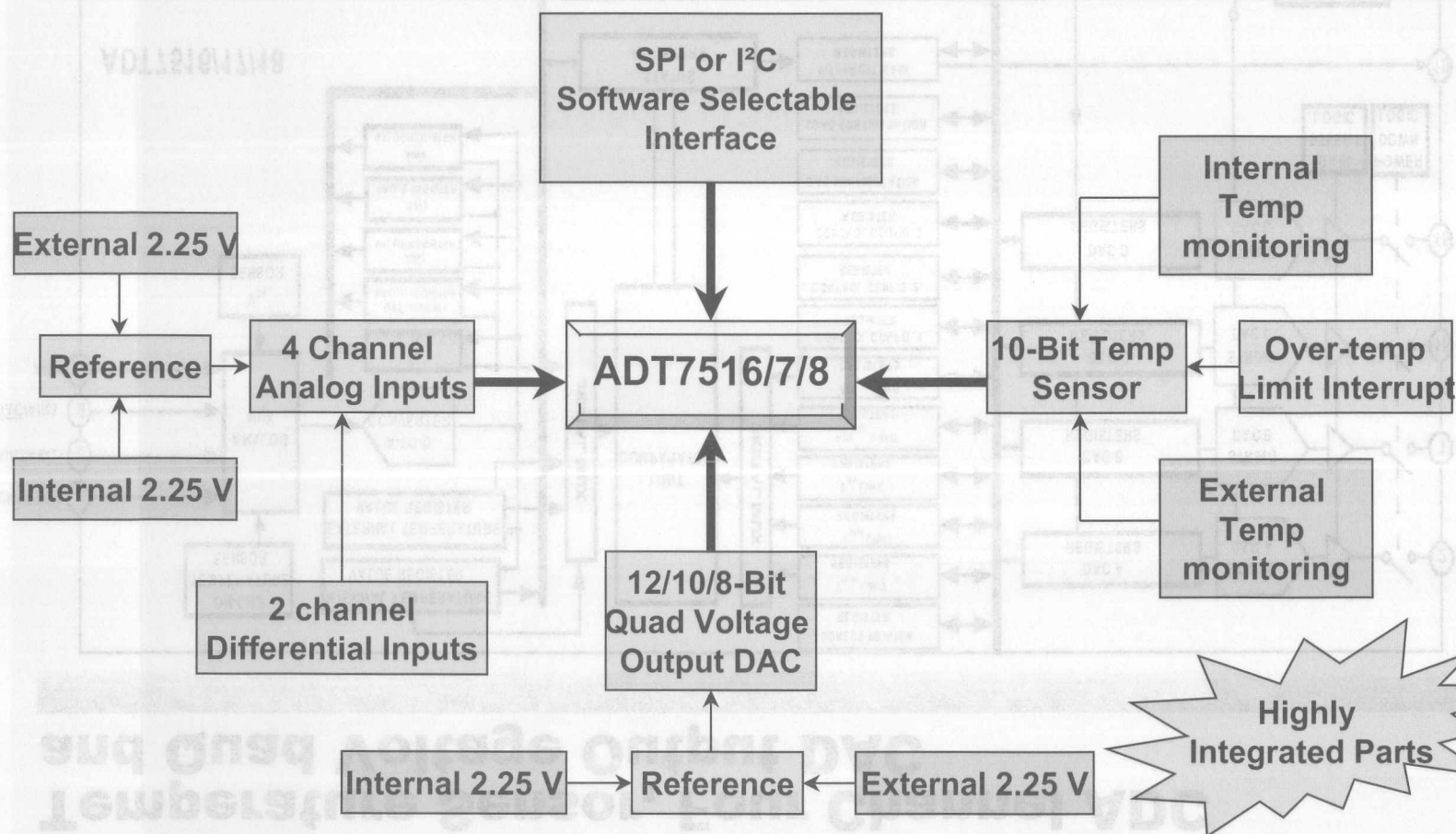
ADT7411 SPI/I²C® Compatible, 10-Bit Digital Temperature Sensor and Eight Channel ADC

- 10-Bit Temperature to Digital Converter
- 10-Bit Eight Channel ADC :
 - DC Input Bandwidth
 - Input Range: 0 V to 2.25 V and 0 V to VDD
- Temperature range: -40° C to +125° C
- Temperature Sensor Accuracy of $\pm 0.5^{\circ}$ C
- Supply Range : + 2.7 V to + 5.5 V
- Power-Down Current 1 μ A
- Internal 2.25 V V_{REF} Option
- Double-Buffered Input Logic
- Buffered / Unbuffered Reference Input Option

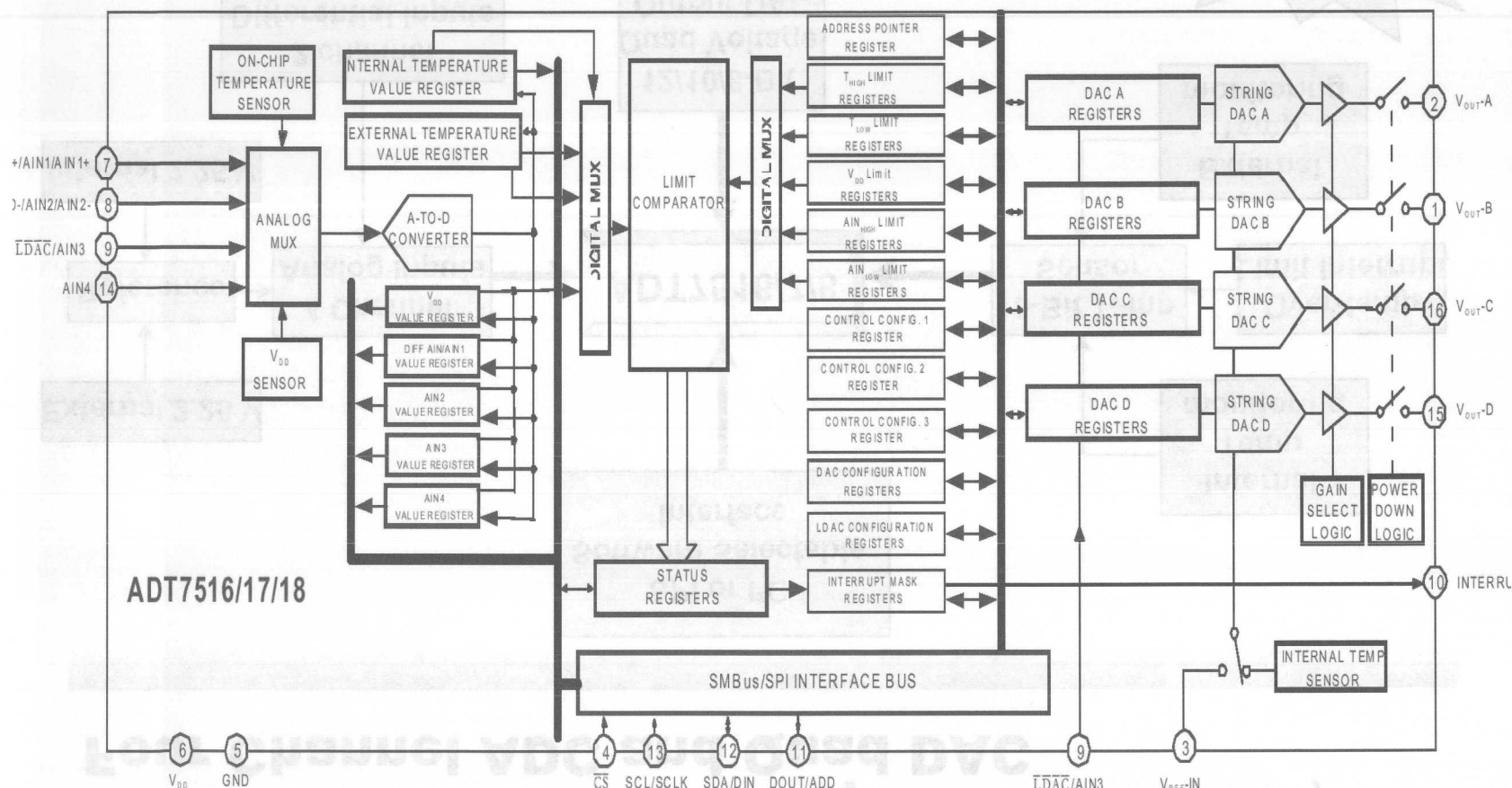
ADT7411 SPI/I²C® Compatible, 10-Bit Digital Temperature Sensor and Eight Channel ADC

- Capable of measuring internal and external temperature sensors
- Two channels can be configured as a Differential Input Channel
- Can hardware select either I²C or SPI serial interface
- Interrupt output to indicate limits been exceeded
- ADC can select between Internal 2.25 V reference or V_{DD} as a reference
- Capable of monitoring it's own V_{DD} supply
- 16-Pin QSOP Package

ADT7516/17/18 10-Bit Temperature Sensor, Four Channel ADC and Quad DAC



ADT7516/17/18 SPI/I²C® Compatible, Temperature Sensor, Four Channel ADC and Quad Voltage Output DAC



ADT7516/17/18 SPI/I²C® Compatible, Temperature Sensor, Four Channel ADC and Quad Voltage Output DAC

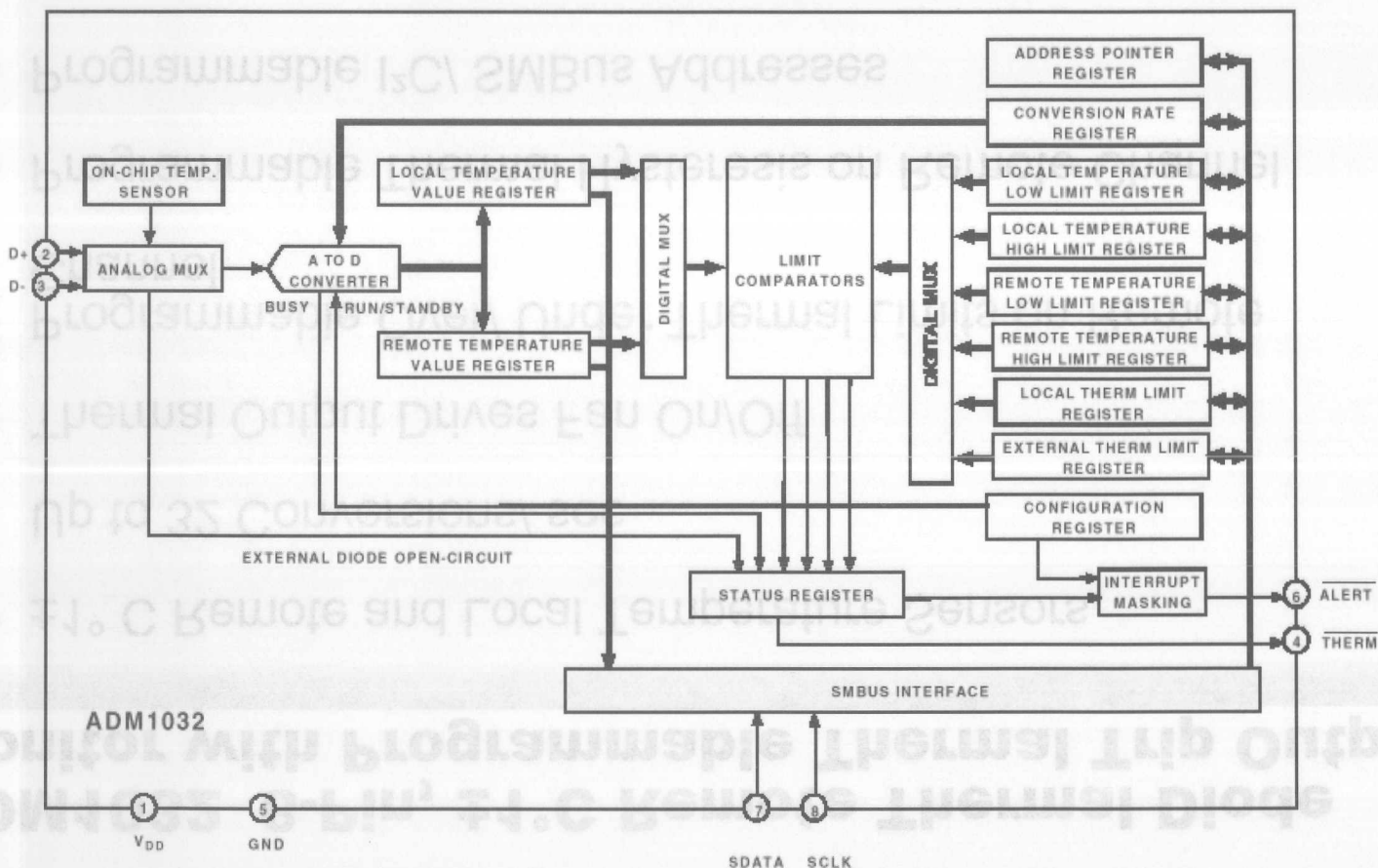
- ADT7516 - Four 12-Bit DACs
- ADT7517 - Four 10-Bit DACs
- ADT7518 - Four 8-Bit DACs
- Buffered Voltage Output
- Guaranteed Monotonic By Design Over All Codes
- 10-Bit Temperature to Digital Converter
- 10-Bit Four Channel ADC :
 - DC Input Bandwidth
 - Input Range: 0 V to 2.25 V
- DAC Output Range: 0 – 2 x V_{REF}
- On-Chip Rail-to-Rail Output Buffer Amplifier

ADT7516/17/18 SPI/I²C[®] Compatible, Temperature Sensor, Four Channel ADC and Quad Voltage Output DAC

- Temperature range: -40° C to +125° C
 - Temperature Sensor Accuracy of $\pm 0.5^{\circ}$ C
- Supply Range : + 2.7 V to + 5.5 V
 - Power-Down Current 1 μ A
- Internal 2.25 V V_{Ref} Option
- Double-Buffered Input Logic
- Buffered / Unbuffered Reference Input Option
- Power-on Reset to Zero Volts
- Simultaneous Update of Outputs
- I²C[®], SPI[™], QSPI[™], MICROWIRE[™] and DSP-
Compatible 4-wire Serial Interface
- 16-Lead QSOP Package

ADM1032 8-Pin, $\pm 1^{\circ}\text{C}$ Remote Thermal Diode Monitor with Programmable Thermal Trip Output

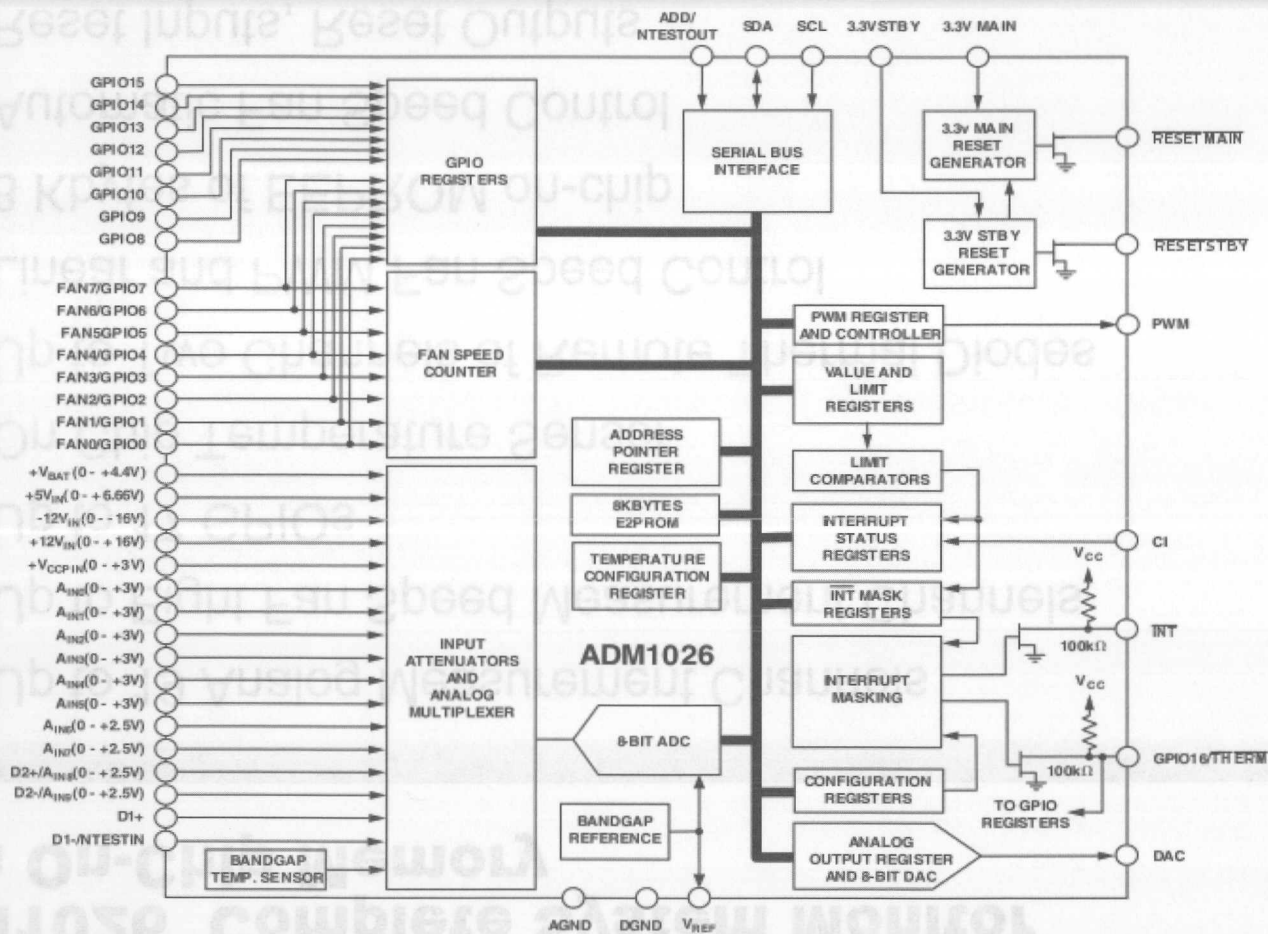
FUNCTIONAL BLOCK DIAGRAM



ADM1032 8-Pin, $\pm 1^{\circ}\text{C}$ Remote Thermal Diode Monitor with Programmable Thermal Trip Output

- $\pm 1^{\circ}\text{C}$ Remote and Local Temperature Sensors
- Up to 32 Conversions/ sec
- Thermal Output Drives Fan On/Off
- Programmable Over/ Under Thermal Limits on Remote Channel
- Programmable Thermal Hysteresis on Remote Channel
- Programmable I²C/ SMBus Addresses
- 8-Lead SOIC/ μ SOIC

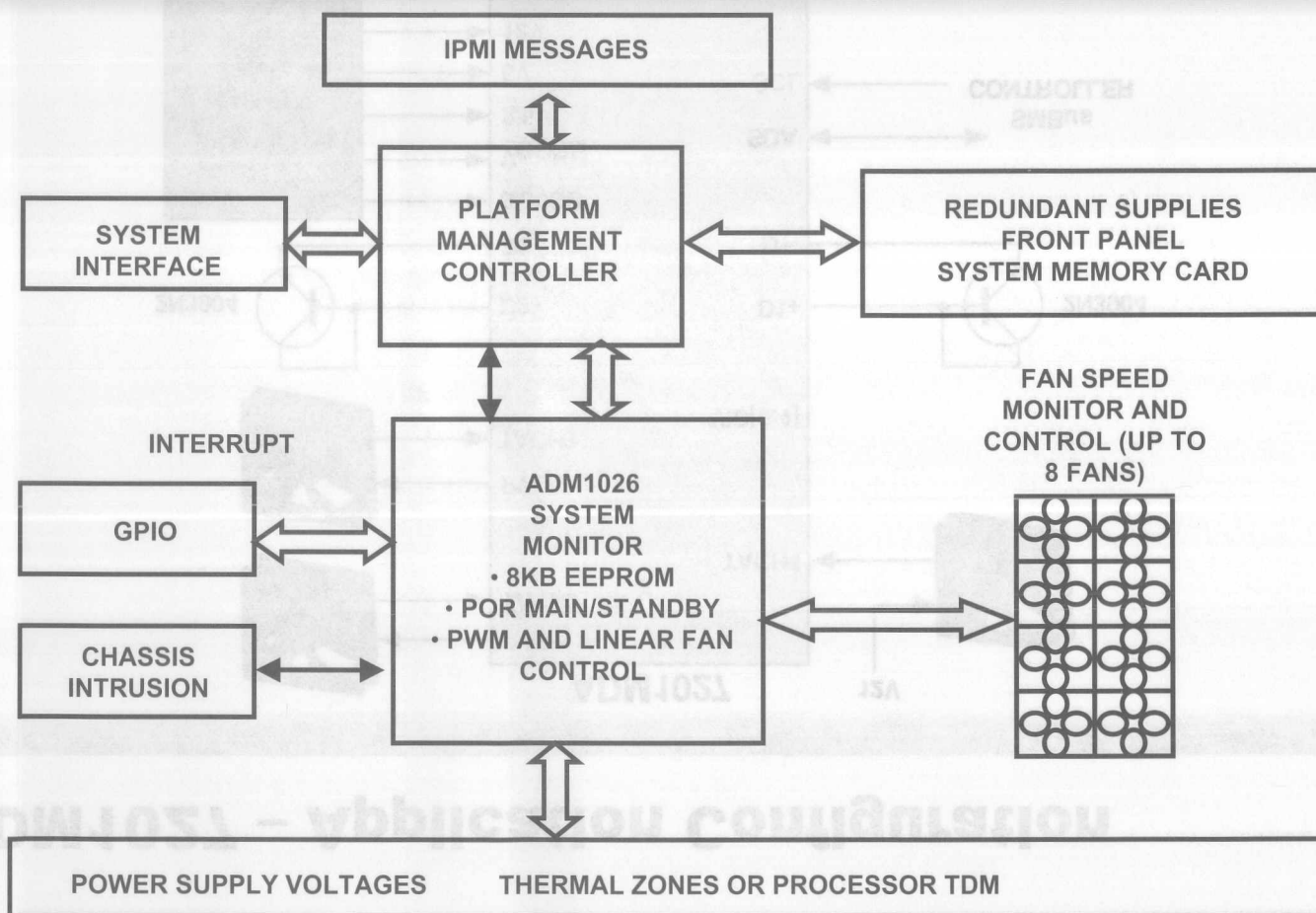
ADM1026 Complete System Monitor with On-Chip Memory



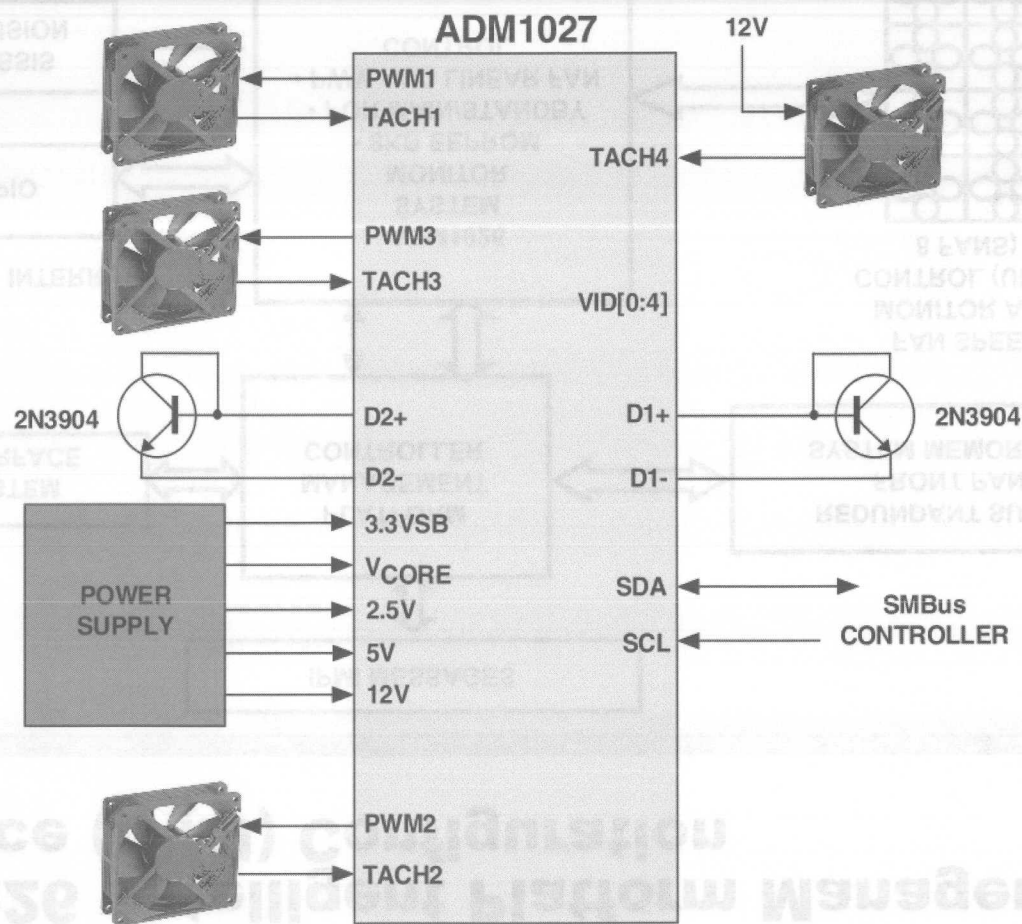
ADM1026 Complete System Monitor with On-Chip Memory

- Up to 19 Analog Measurement Channels
- Up to Eight Fan Speed Measurement Channels
- Up to 17 GPIOs
- On Chip Temperature Sensor
- Up to Two Channels of Remote Thermal Diodes
- Linear and PWM Fan Speed Control
- 8 Kbytes of EEPROM on-chip
- Automatic Fan Speed Control
- Reset Inputs, Reset Outputs
- Chassis Intrusion Detector

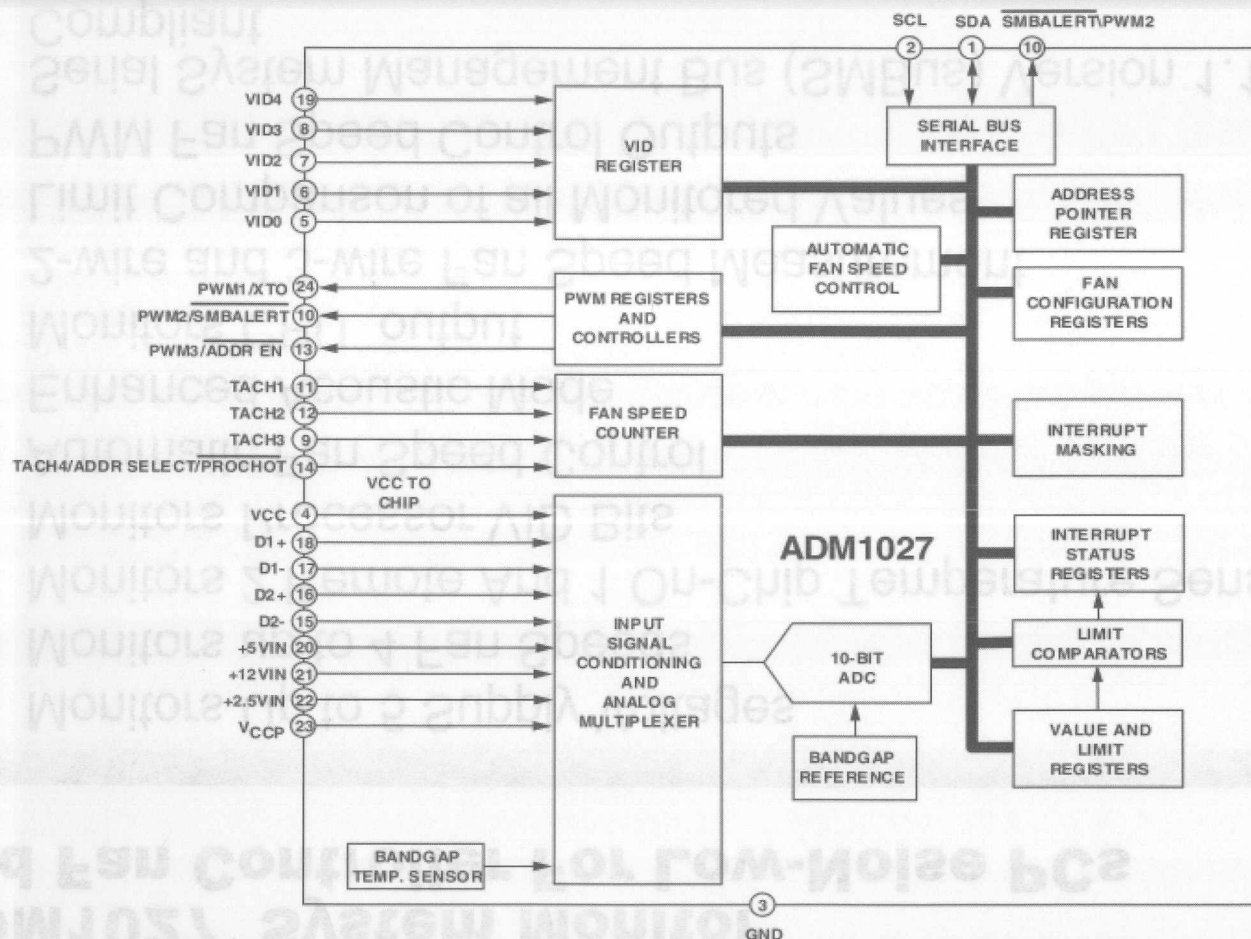
ADM1026 Intelligent Platform Management Interface (IPMI) Configuration



ADM1027 – Application Configuration



ADM1027 System Monitor and Fan Controller For Low-Noise PCs



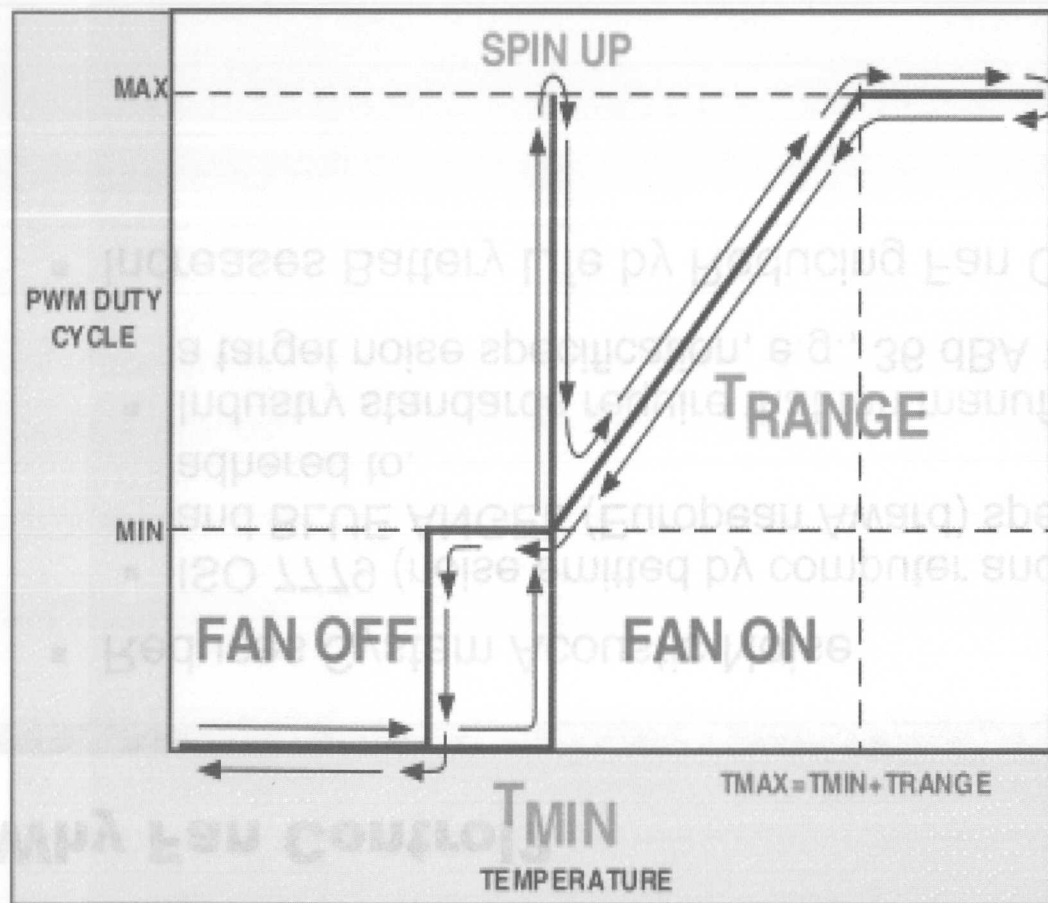
ADM1027 System Monitor and Fan Controller For Low-Noise PCs

- Monitors Up to 5 Supply Voltages
- Monitors up to 4 Fan Speeds
- Monitors 2 Remote And 1 On-Chip Temperature Sensor
- Monitors Processor VID Bits
- Automatic Fan Speed Control
- Enhanced Acoustic Mode
- Monitors CPU output
- 2-wire and 3-wire Fan Speed Measurement
- Limit Comparison of all Monitored Values
- PWM Fan Speed Control Outputs
- Serial System Management Bus (SMBus) Version 1.1 Compliant
- Meets SMBus 2.0 Electrical Specifications

Why Fan Control?

- Reduces System Acoustic Noise
 - ISO 7779 (noise emitted by computer and business equipment) and BLUE ANGEL (European Award) specifications must be adhered to.
 - Industry standards require that fan manufacturers achieve a target noise specification, e.g., 36 dBA for PC fans.
- Increases Battery Life by Reducing Fan Current Consumption

Automatic Fan Speed Control



Programmable Fan Spin-up Time

Variable Temp. To Fan Speed Slope, T_{RANGE}

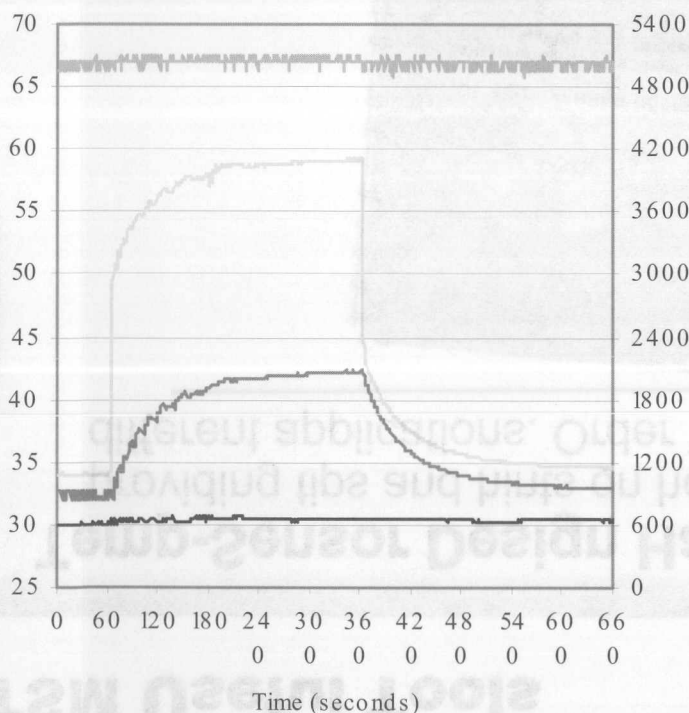
Program Fan Start Temperature, T_{MIN}

5° C Hysteresis Prevents Fan Cycling

Increase Fan Speed When Temperature Increases

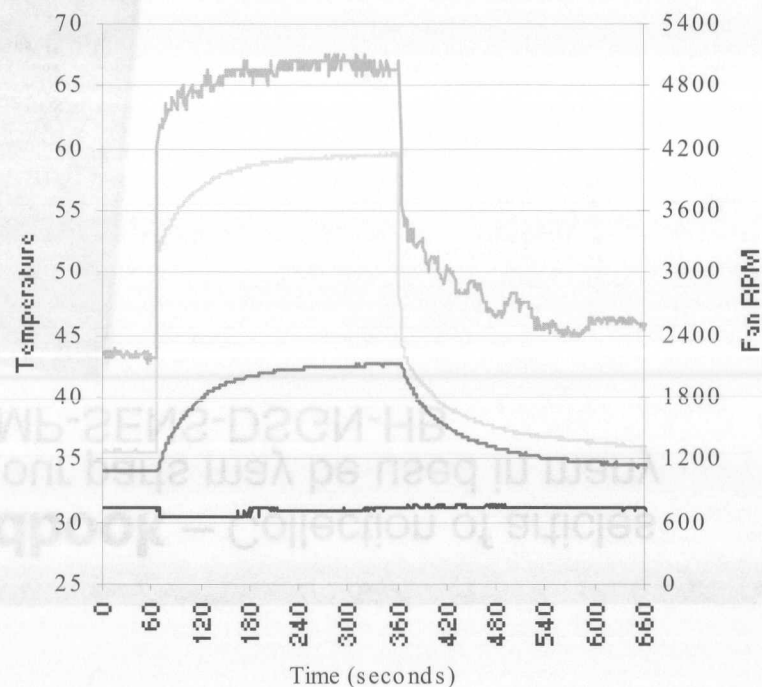
Fans on 100%

— Fan Inlet Temp — Heatsink Temp
— CPU Temp — Fan RPM



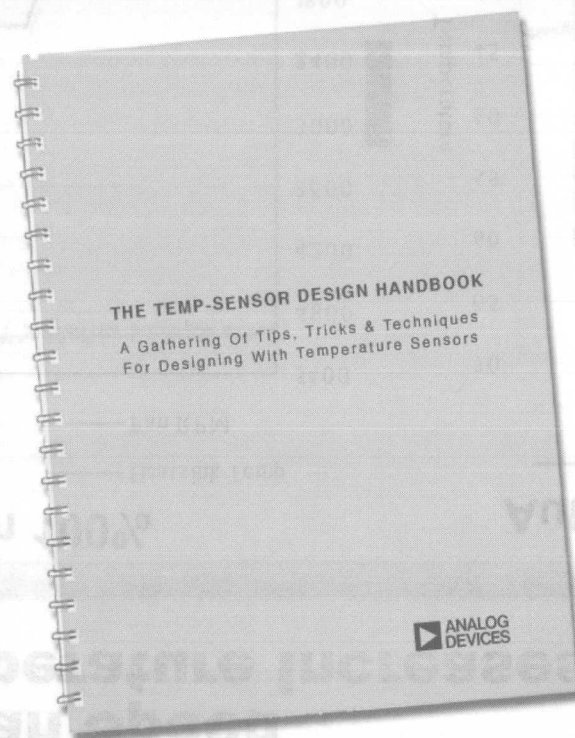
Automatic Fan Speed Control

— Fan Inlet Temp — Heatsink Temp
— CPU Temp — Fan RPM



TSM Useful Tools

Temp-Sensor Design Handbook – Collection of articles providing tips and hints on how our parts may be used in many different applications. Order TEMP-SENS-DSGN-HB

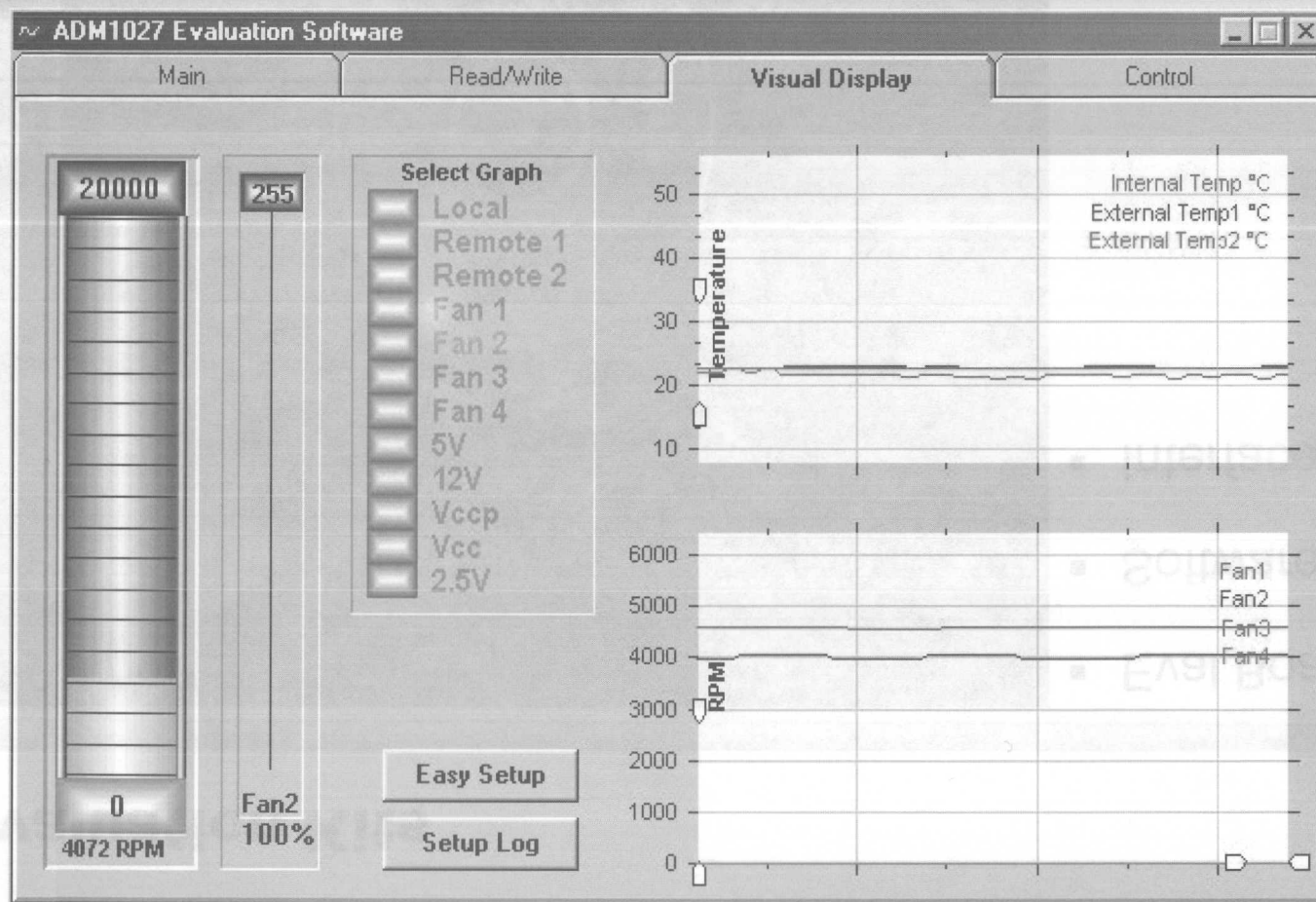


Evaluation Kits

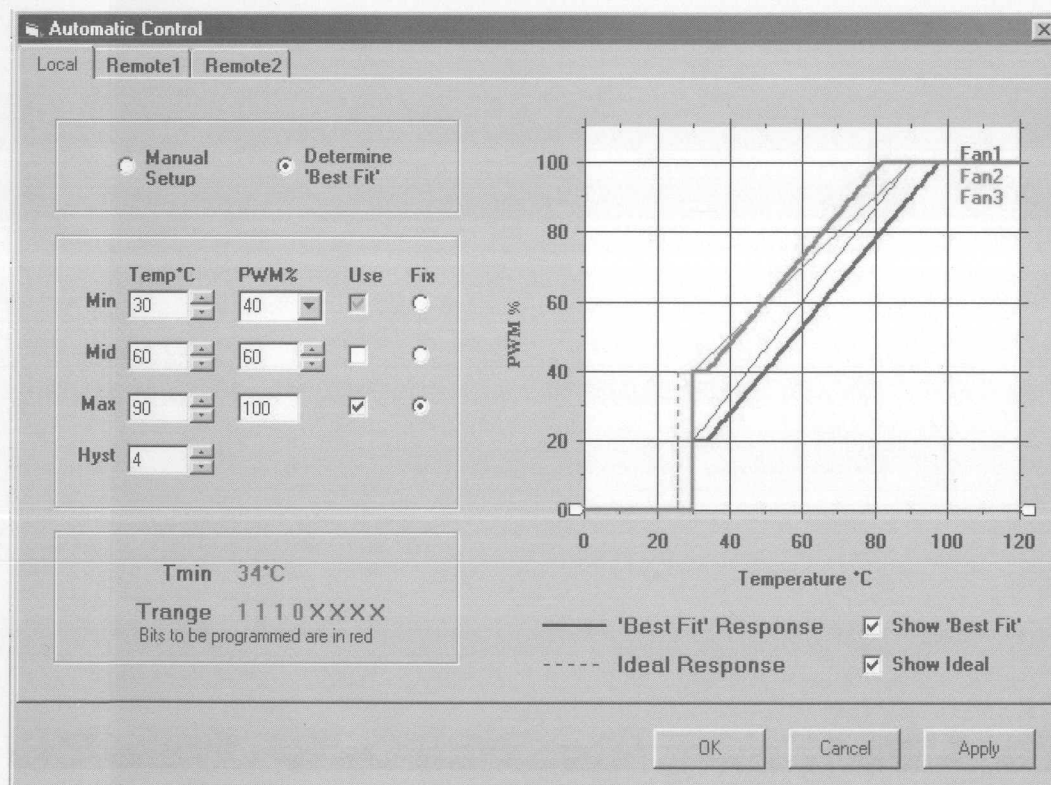
- Eval Board
- Software CD
- Interface Cable



Evaluation Software - Graphing Utility



System Characterization Software

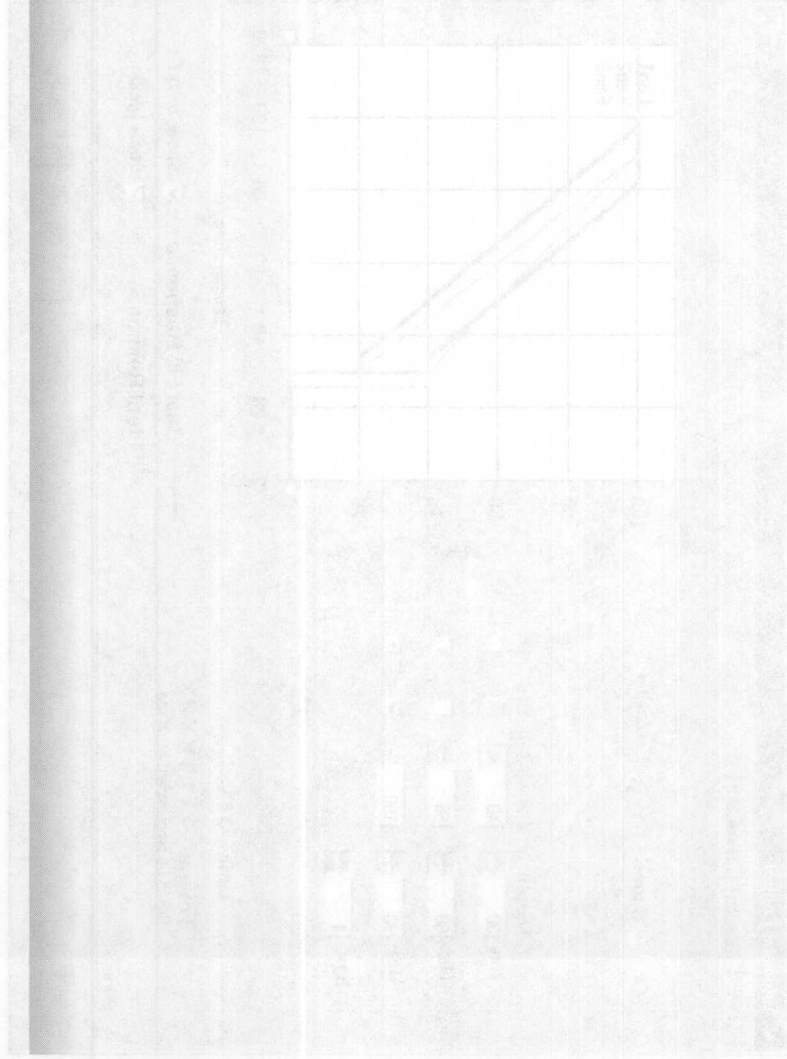


- Automatic System Profiling
- Best Fit Calculation



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- Best Fit Calculation
- Profiling
- Automatic System

System Characterization Software



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SECTION 14

Power Management Circuits

Linear Low Dropout Regulators
Switch-Mode Power Circuits

Linear Low Dropout Regulators

SECTION 14

Analog Devices anyCAP[®] LDO Regulators

- Typical LDOs lack sufficient phase margin and, to remain stable, require output capacitors with a minimum ESR. To obtain the required ESR, designers are forced to use more costly and larger caps. Additionally, the ESR of a capacitor varies with temperature, requiring further circuit design analysis. Analog Devices' anyCAP LDOs use internal pole splitting to eliminate the need for minimum ESR. Analog Devices' anyCAP LDOs are stable with any type of capacitor, including MLCCs with values as low as 0.47 μ F.

anyCAP LDOs

CONVENTIONAL LDOs

Typical LDOs vs. ADI's anyCAP LDO

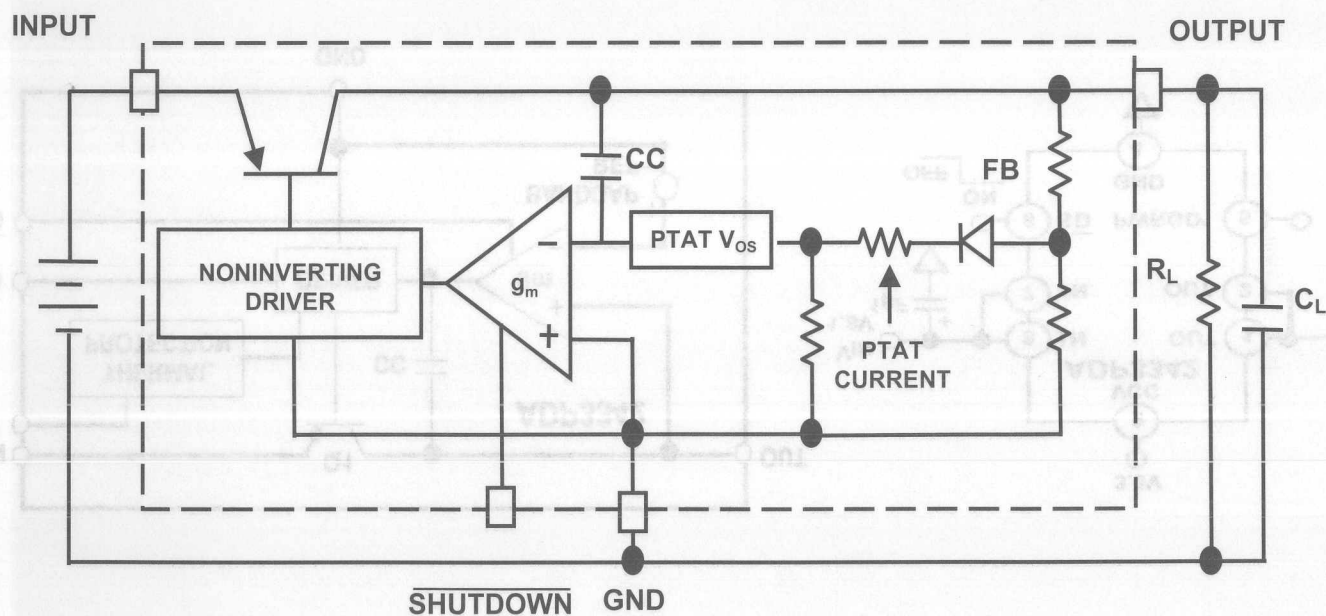
anyCAP LDOs

- No Minimum ESR Requirement
- No Stability Problems
- Less Design Effort
- Smaller Size Capacitor
- Smaller Value Capacitor
- Less Board Space
- Lower Cost Capacitor

Conventional LDOs

- Minimum ESR Required
- Can Become Unstable
- More Design Effort
- Larger Value Capacitor
- Larger Size Capacitor
- More Board Space
- Higher Cost Capacitor

anyCAP Block Diagram



ADP3342 Ultralow I_Q 300 mA anyCAP LDO Regulator

- Accuracy Over Line and Load: $\pm 4.0\%$ @ 25°C , $\pm 5\%$ Over Temperature
- Ultralow Dropout Voltage: 300 mV (Typ) @ 300 mA
- Requires Only $C_O = 1.0\ \mu\text{F}$ for Stability
- anyCAP = Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Shutdown Current: $< 2\ \mu\text{A}$
- $1.7\text{ V} \leq V_{IN} \leq 6\text{ V}$
- $2.7\text{ V} \leq V_{CC} \leq 6\text{ V}$
- $V_{OUT} = 1.2\text{ V} \pm 5\%$
- 0°C to $+100^\circ\text{C}$ Ambient Temperature Range
- Ultrasmall Thermally Enhanced 8-Lead μSOP Package

ADP3333 High-Accuracy, Ultralow I_Q , 300 mA anyCAP LDO Regulator

- High Accuracy Over Line and Load:
 - $\pm 0.8\%$ @ 25°C , $\pm 1.8\%$ over temperature
- Ultralow Dropout Voltage: 230 mV (Max) @ 300 mA
- Requires Only $C_O = 1.0\ \mu\text{F}$ for Stability
- anyCAP: Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Noise
- Low Shutdown Current: $< 1\ \mu\text{A}$
- 2.6 V to 12 V Supply Range
- -40°C to $+85^\circ\text{C}$ Ambient Temperature Range
- Ultrasmall 8-Lead μSOP Package

ADP3334 High-Accuracy, Low I_Q , 500 mA anyCAP Adjustable LDO Regulator

- High Accuracy Over Line and Load:
 - $\pm 0.9\%$ @ 25°C , $\pm 1.8\%$ over temperature
- Ultralow Dropout Voltage: 200 mV (Typ) @ 500 mA
- Requires Only $C_O = 1.0\ \mu\text{F}$ for Stability
- anyCAP = Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Noise
- Low Shutdown Current: $< 1.0\ \mu\text{A}$ (Typ)
- 2.6 V to 11 V Supply Range
- 1.5 V to 10 V Output Range
- -40°C to $+85^\circ\text{C}$ Ambient Temperature Range
- Thermally-Enhanced 8-Lead SO Package

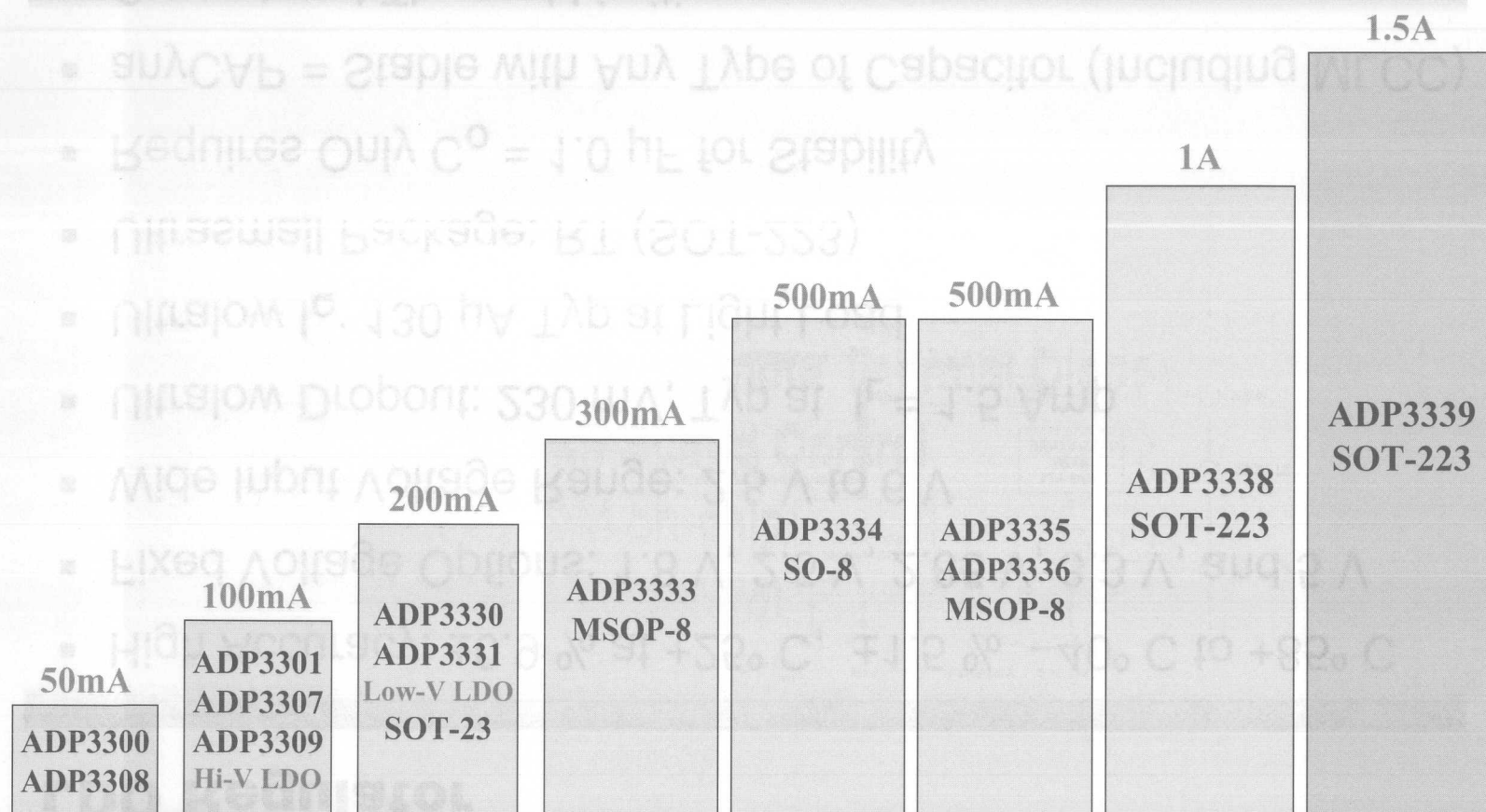
ADP3338 anyCAP 1 Amp High-Accuracy LDO Regulator

- High Accuracy: $\pm 0.8\%$ at $+25^\circ\text{C}$, $\pm 1.4\%$ -40°C to $+85^\circ\text{C}$
- Fixed Voltage Options: 1.8 V, 2.5 V, 2.85 V, 3.3 V, and 5 V
- Wide Input Voltage Range: 2.7 V to 8 V
- Ultralow Dropout: 190 mV, Typ at $I_L = 1\text{ A}$
- Ultralow I_Q : 110 μA Typ at Light Load
- Ultrasmall Package: RT (SOT-223)
- Requires Only $C_O = 1.0\text{ }\mu\text{F}$ for Stability
- anyCAP = Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Noise

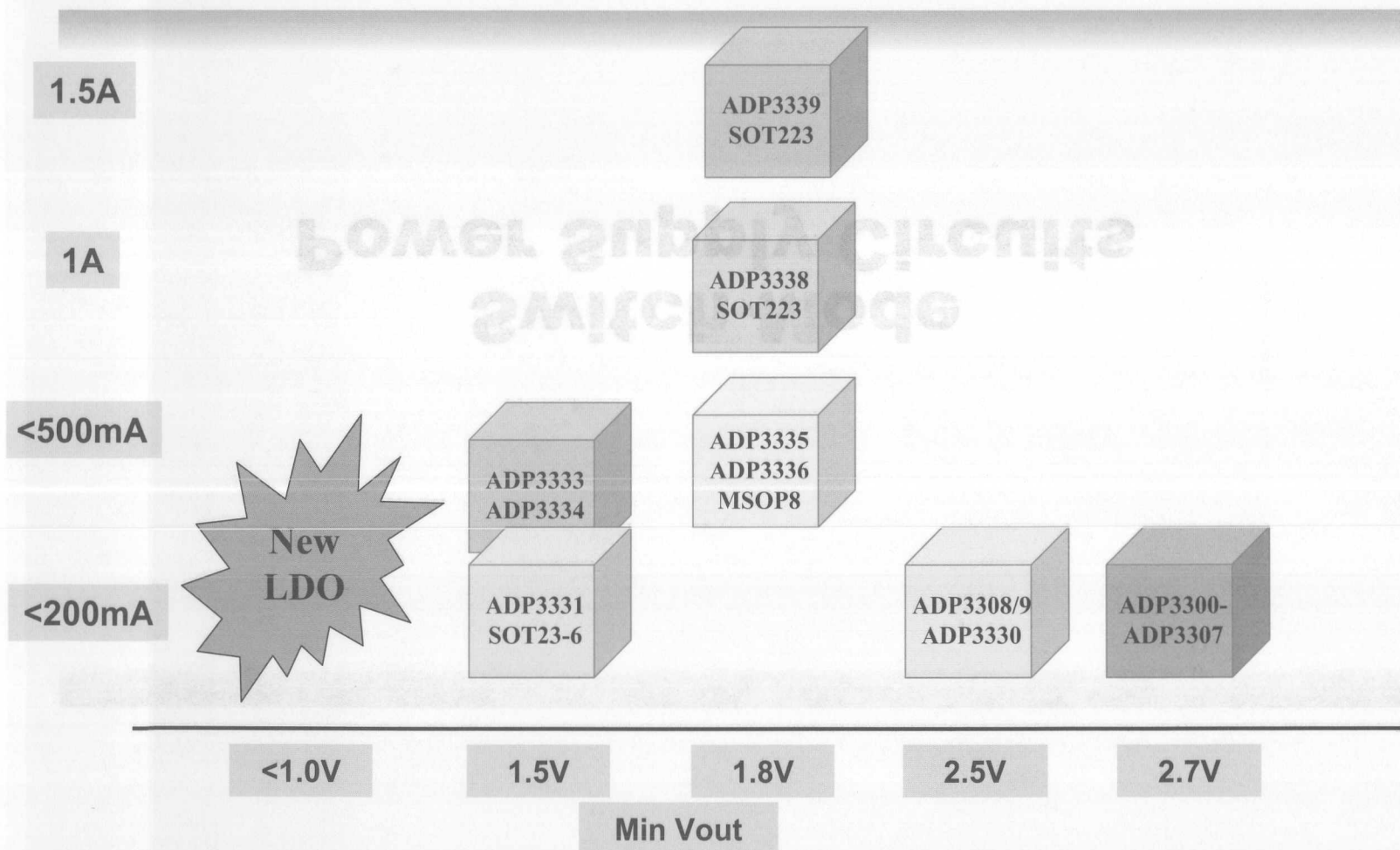
ADP3339 anyCAP® 1.5 Amp High-Accuracy LDO Regulator

- High Accuracy: $\pm 0.9\%$ at $+25^\circ\text{C}$, $\pm 1.5\%$ -40°C to $+85^\circ\text{C}$
- Fixed Voltage Options: 1.8 V, 2.5 V, 2.85 V, 3.3 V, and 5 V
- Wide Input Voltage Range: 2.8 V to 6 V
- Ultralow Dropout: 230 mV, Typ at $I_L = 1.5\text{ Amp}$
- Ultralow I_Q : 130 μA Typ at Light Load
- Ultrasmall Package: RT (SOT-223)
- Requires Only $C_O = 1.0\text{ }\mu\text{F}$ for Stability
- anyCAP = Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Noise

LDO Product Road Map



LDO Coverage Iout & Vout min





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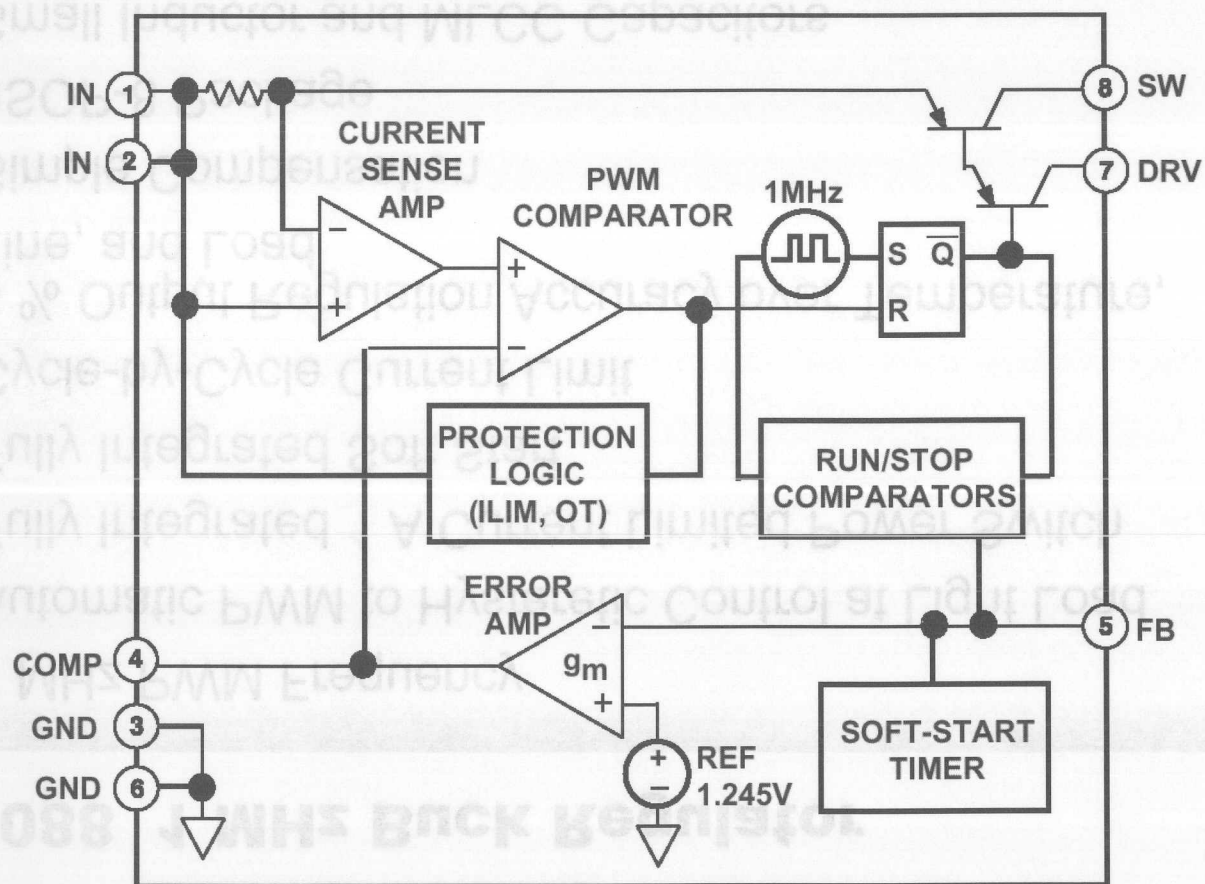
Switch-Mode Power Supply Circuits



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14-14

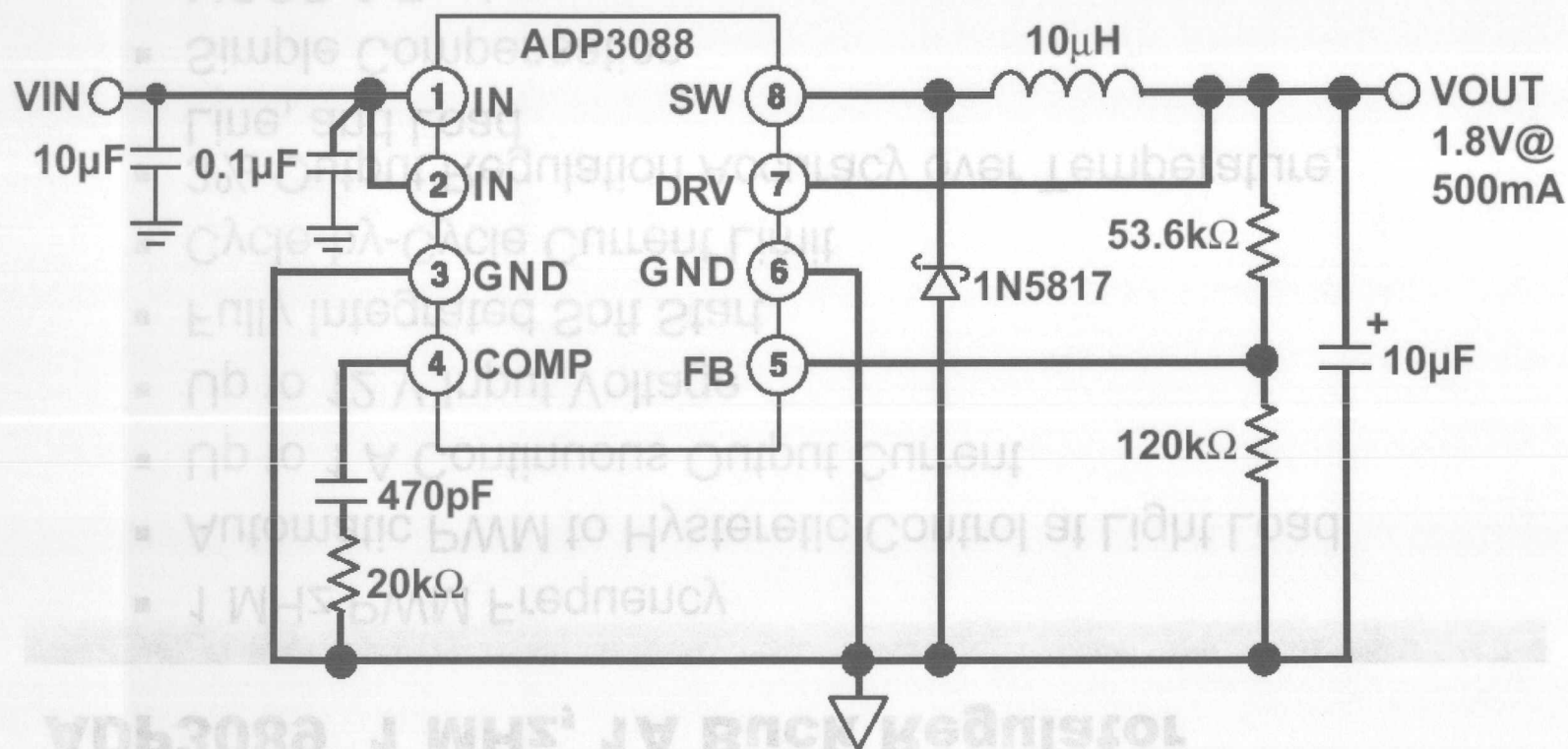
ADP3088 1 MHz Buck Regulator



ADP3088 1 MHz Buck Regulator

- 1 MHz PWM Frequency
- Automatic PWM to Hysteretic Control at Light Load
- Fully Integrated 1 A Current Limited Power Switch
- Fully Integrated Soft Start
- Cycle-by-Cycle Current Limit
- 3 % Output Regulation Accuracy over Temperature, Line, and Load
- Simple Compensation
- μ SOP-8 Package
- Small Inductor and MLCC Capacitors
- Low Quiescent Current while Pulse Skipping
- Thermal Shutdown

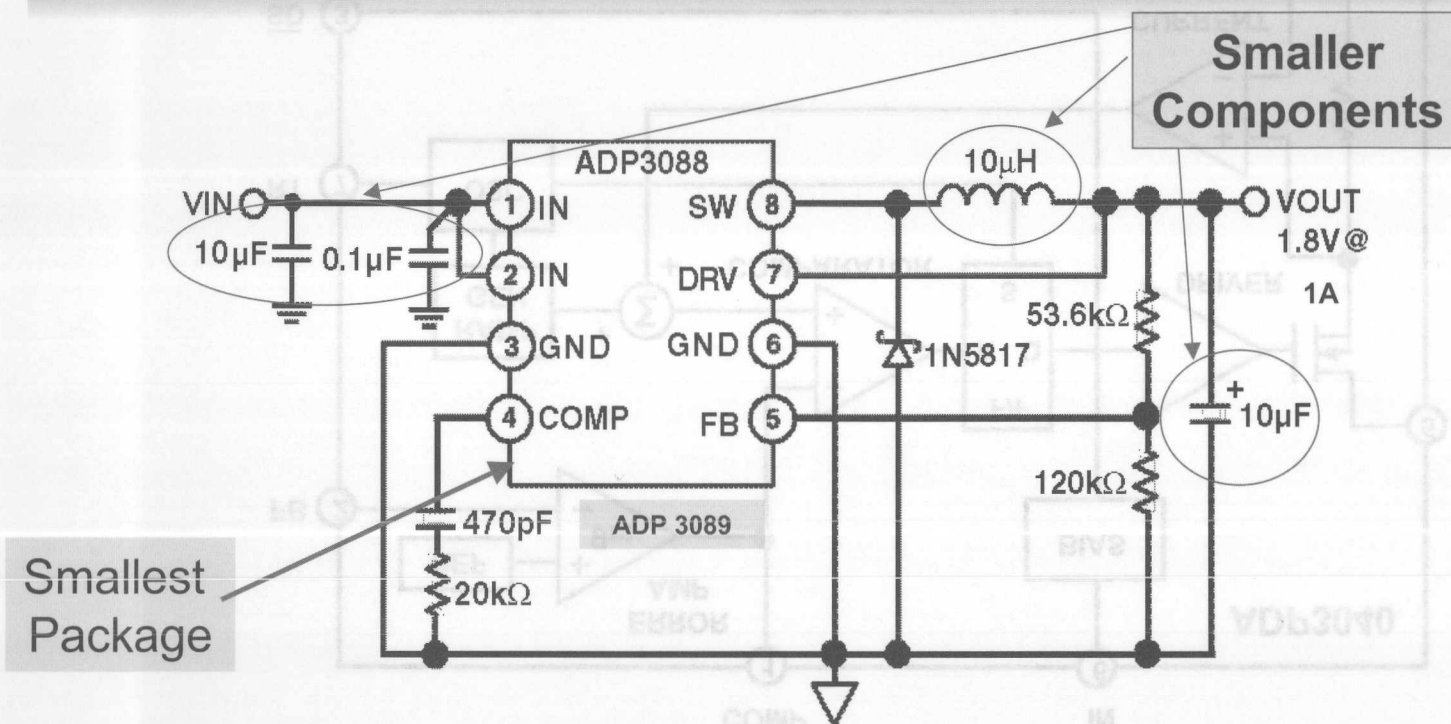
ADP3088 Typical Application



ADP3089 1 MHz, 1A Buck Regulator

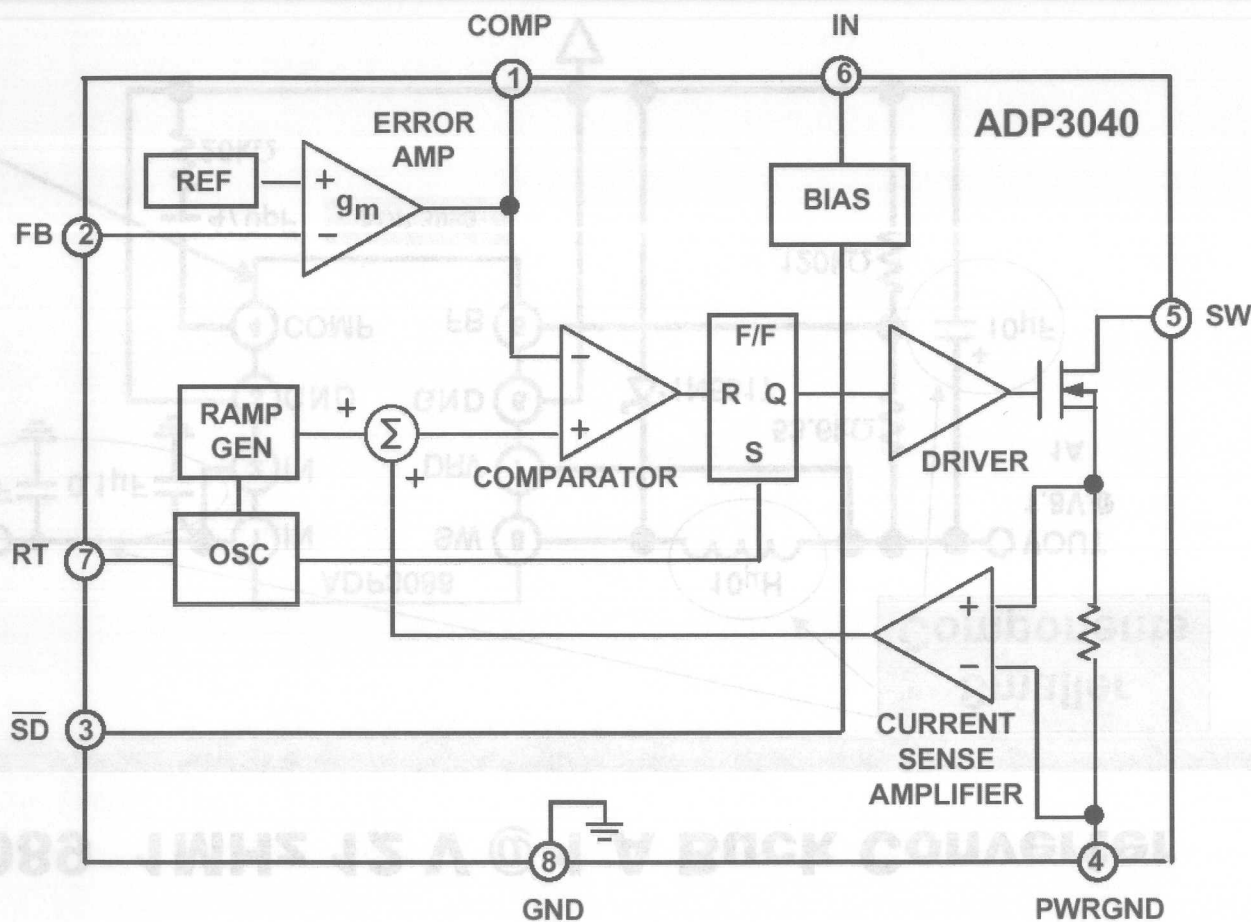
- 1 MHz PWM Frequency
- Automatic PWM to Hysteretic Control at Light Load
- Up to 1 A Continuous Output Current
- Up to 12 V Input Voltage
- Fully Integrated Soft Start
- Cycle-by-Cycle Current Limit
- 3% Output Regulation Accuracy over Temperature, Line, and Load
- Simple Compensation
- MSOP-8 Package
- Small Inductor and MLCC Capacitors
- Low Quiescent Current while Pulse Skipping
- Thermal Shutdown

ADP3089 1MHz 12 V @ 1 A Buck Converter



High Frequency + Smallest Package = Smallest Footprint
= \$pace \$aving + Cost \$aving

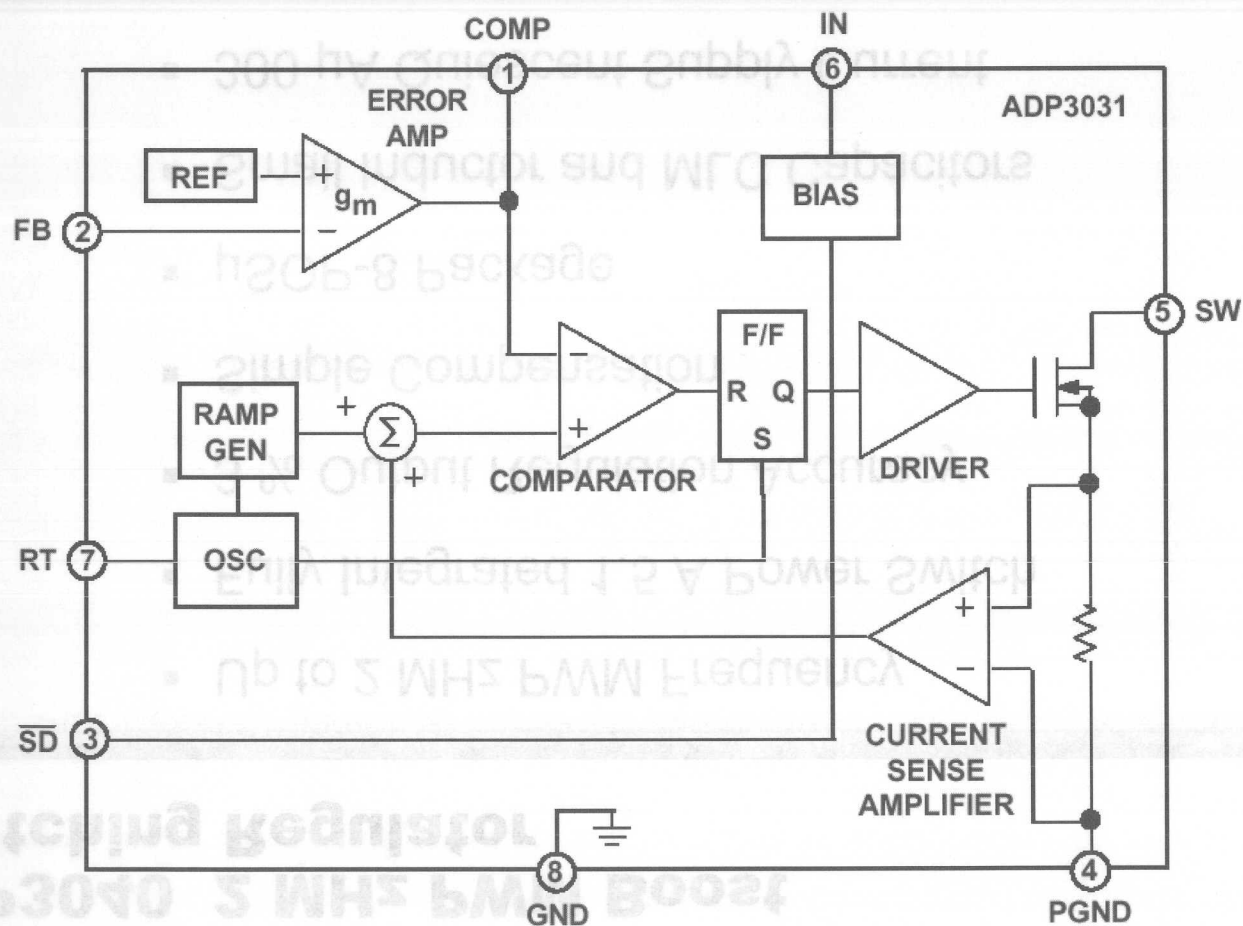
ADP3040 2 MHz PWM Boost Switching Regulator



ADP3040 2 MHz PWM Boost Switching Regulator

- Up to 2 MHz PWM Frequency
- Fully Integrated 1.5 A Power Switch
- 3 % Output Regulation Accuracy
- Simple Compensation
- μ SOP-8 Package
- Small Inductor and MLC Capacitors
- 300 μ A Quiescent Supply Current
- 90 % Efficiency
- Undervoltage Lockout

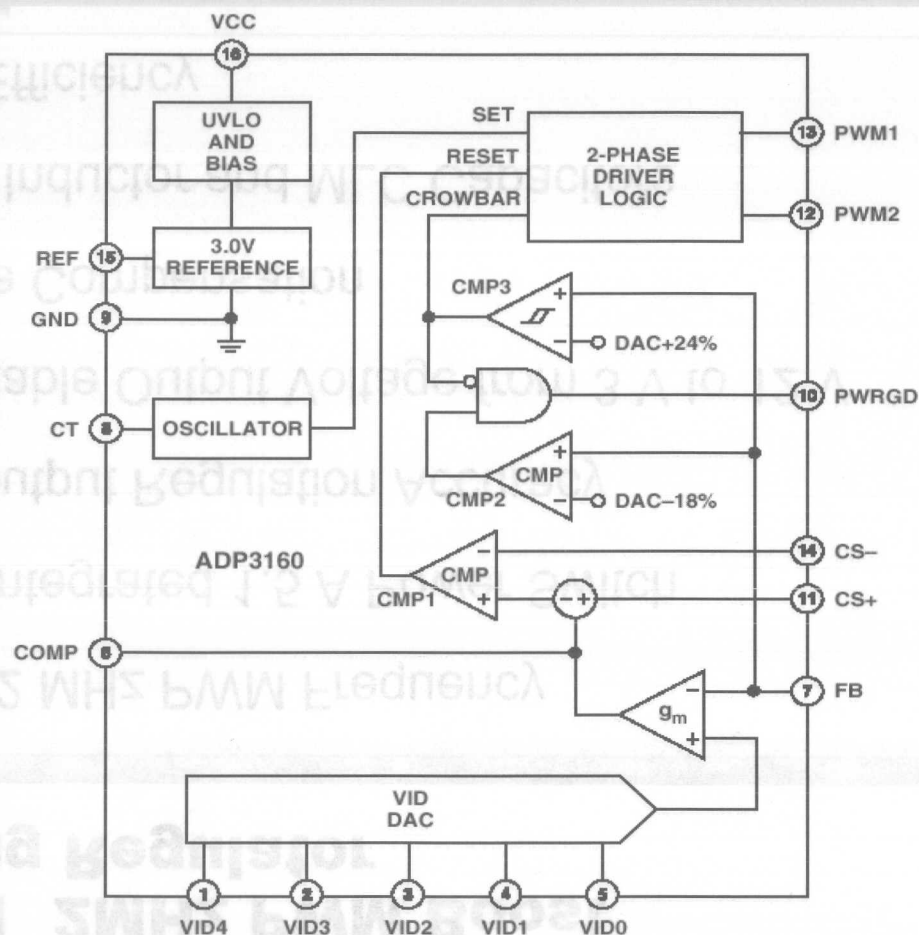
ADP3031 2MHz PWM Boost Switching Regulator



ADP3031 2MHz PWM Boost Switching Regulator

- Up to 2 MHz PWM Frequency
- Fully Integrated 1.5 A Power Switch
- 3 % Output Regulation Accuracy
- Adjustable Output Voltage from 3 V to 12 V
- Simple Compensation
- Small Inductor and MLC Capacitors
- 90% Efficiency
- Under-voltage Lockout
- Shutdown

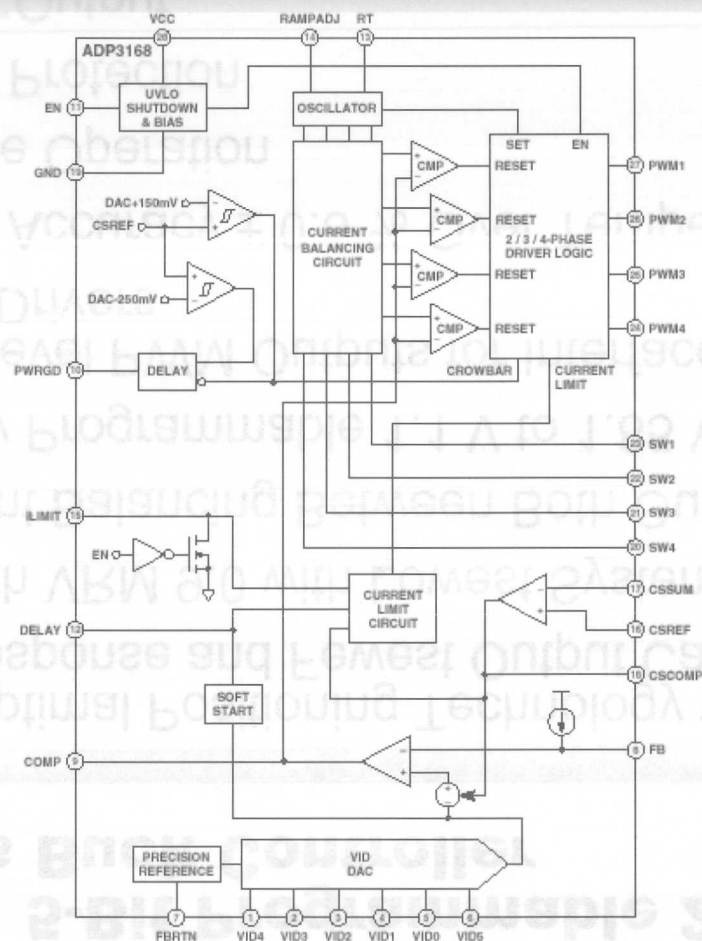
ADP3160/67 5-Bit Programmable 2-Phase Synchronous Buck Controller



ADP3160/67 5-Bit Programmable 2-Phase Synchronous Buck Controller

- ADOPT™ Optimal Positioning Technology for Superior Load Transient Response and Fewest Output Capacitors
- Complies with VRM 9.0 with Lowest System Cost
- Active Current Balancing Between Both Output Phases
- 5-Bit Digitally Programmable 1.1 V to 1.85 V Output
- Dual Logic-Level PWM Outputs for Interface to External High-Power Drivers
- Total Output Accuracy $\pm 0.8\%$ Over Temperature
- Current-Mode Operation
- Short Circuit Protection
- Power-Good Output
- Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components

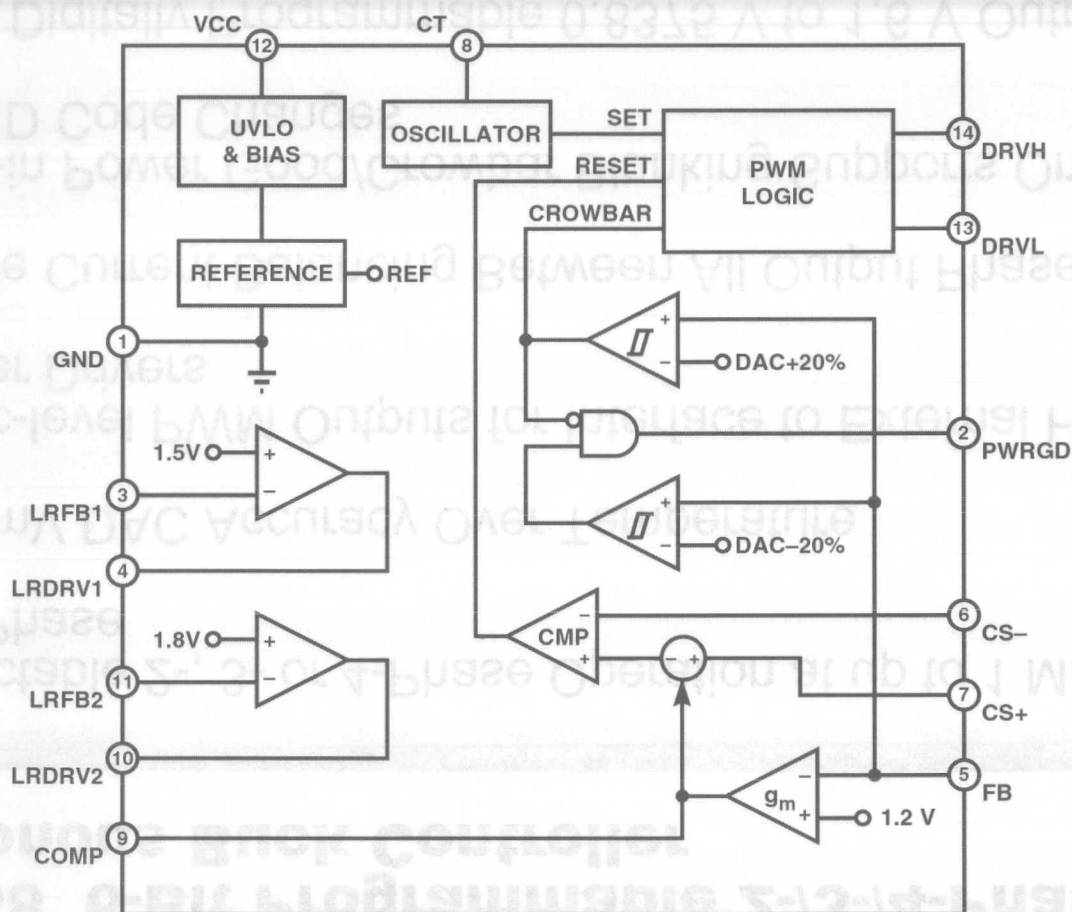
ADP3168 6-Bit Programmable 2-/3-/4-Phase Synchronous Buck Controller



ADP3168 6-Bit Programmable 2-/3-/4-Phase Synchronous Buck Controller

- Selectable 2-, 3- or 4-Phase Operation at up to 1 MHz per Phase
- ± 10 mV DAC Accuracy Over Temperature
- Logic-level PWM Outputs for Interface to External High-power Drivers
- Active Current Balancing Between All Output Phases
- Built-in Power Good/Crowbar Blanking Supports On-the-fly VID Code Changes
- 6-Bit Digitally Programmable 0.8375 V to 1.6 V Output
- Programmable Short Circuit Protection with Programmable Latch-off Delay

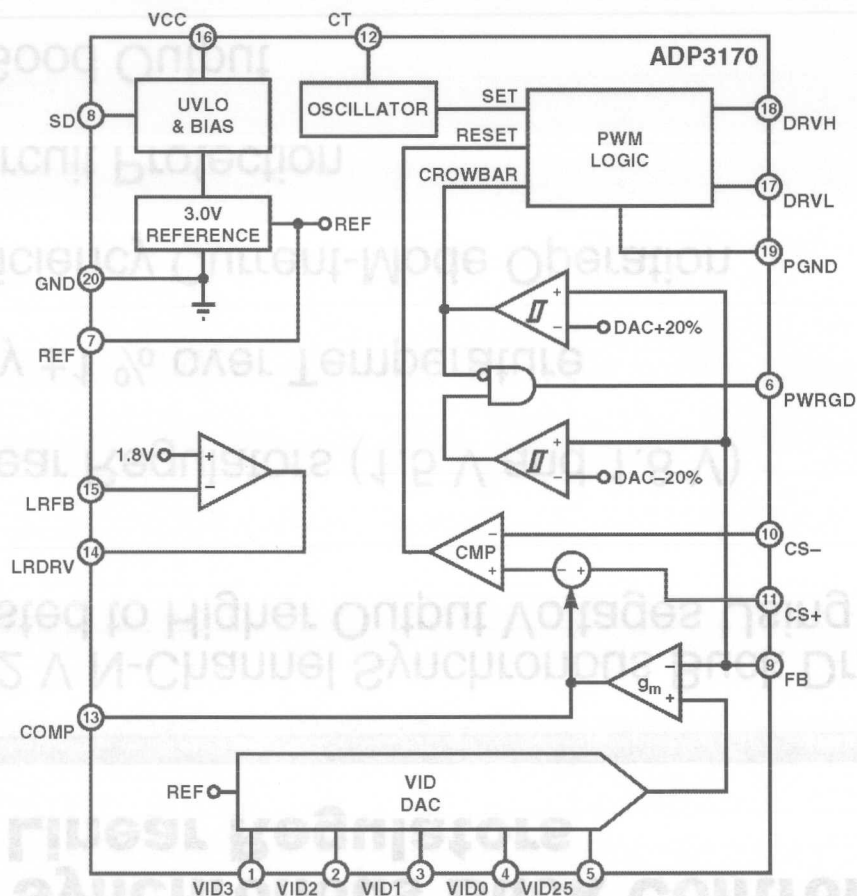
ADP3171 Synchronous Buck Controller with Dual Linear Regulators



ADP3171 Synchronous Buck Controller with Dual Linear Regulators

- Fixed 1.2 V N-Channel Synchronous Buck Driver — Can Be Adjusted to Higher Output Voltages Using a Resistor Divider
- Two Linear Regulators (1.5 V and 1.8 V)
- Accuracy $\pm 1\%$ over Temperature
- High Efficiency Current-Mode Operation
- Short Circuit Protection
- Power Good Output
- Overvoltage Protection Crowbar — Protects Switching Output with No Additional Components

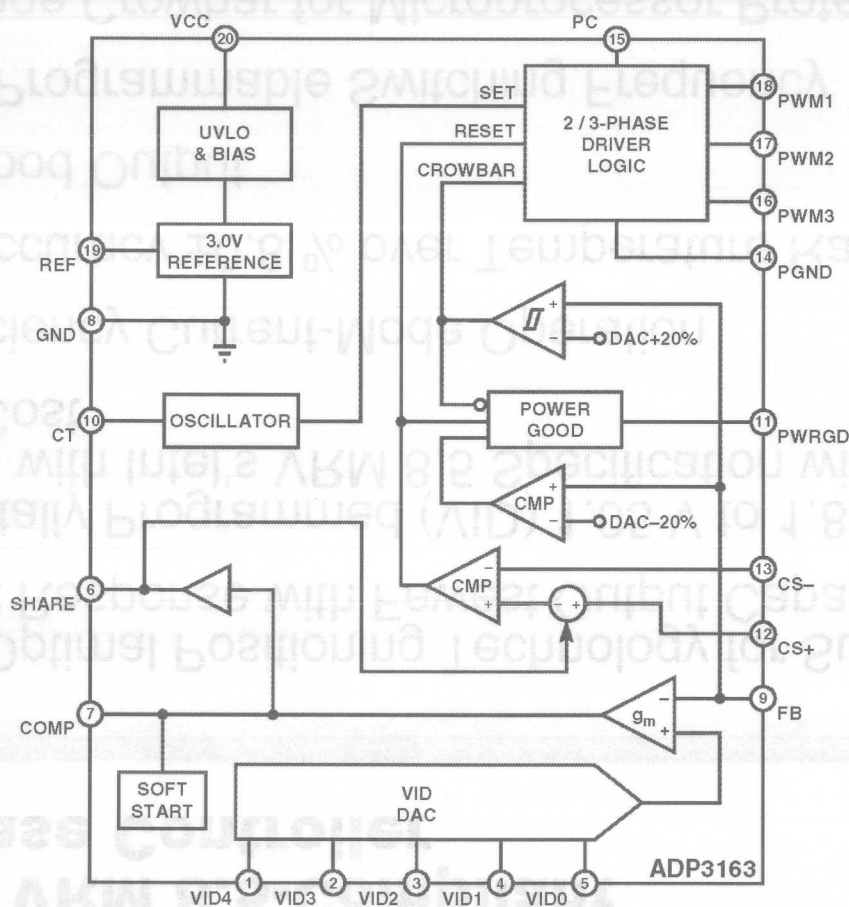
ADP3170 VRM 8.5-Compliant Single-Phase Controller



ADP3170 VRM 8.5-Compliant Single-Phase Controller

- ADOPT Optimal Positioning Technology for Superior Transient Response with Fewest Output Capacitors
- 5-Bit Digitally Programmed (VID) 1.05 V to 1.825 V Output Complies with Intel's VRM 8.5 Specification with Lowest System Cost
- High Efficiency Current-Mode Operation
- Output Accuracy $\pm 0.8\%$ over Temperature Range
- Power Good Output
- 500 kHz Programmable Switching Frequency
- Overvoltage Crowbar for Microprocessor Protection
- Short Circuit Protected with User-Defined Current Limit
- On-board 1.8 V Linear Regulator

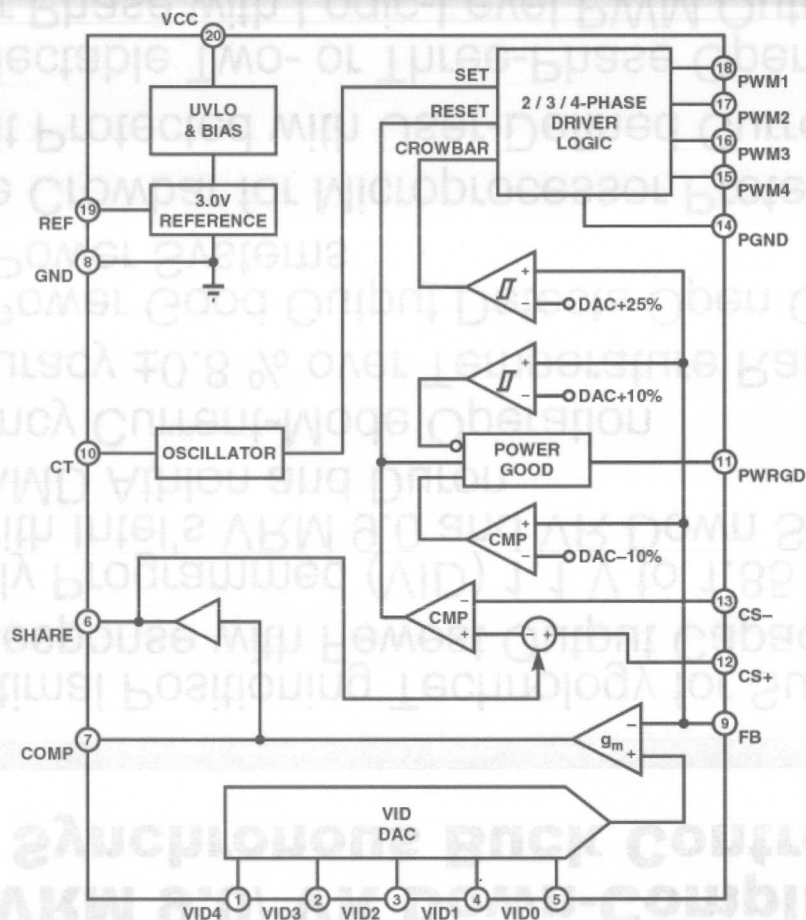
ADP3163 VRM 9.0/ VR Down-Compliant 2-/3-Phase Synchronous Buck Controller



ADP3163 VRM 9.0/ VR Down-Compliant 2-/3-Phase Synchronous Buck Controller

- ADOPT Optimal Positioning Technology for Superior Transient Response with Fewest Output Capacitors
- 5-Bit Digitally Programmed (VID) 1.1 V to 1.85 V Output Complies with Intel's VRM 9.0 and VR Down Specifications as well as AMD Athlon and Duron
- High Efficiency Current-Mode Operation
- Output Accuracy $\pm 0.8\%$ over Temperature Range
- Enhanced Power Good Output Detects Open Outputs in Multi-VRM Power Systems
- Overvoltage Crowbar for Microprocessor Protection
- Short Circuit Protected with User-Defined Current Limit
- Digitally Selectable Two- or Three-Phase Operation at up to 500 kHz per Phase with Logic-Level PWM Outputs for Interface to External High-Power Drivers
- Active Current Balancing between All Phases
- Accurate Multiple VRM Module Current Sharing

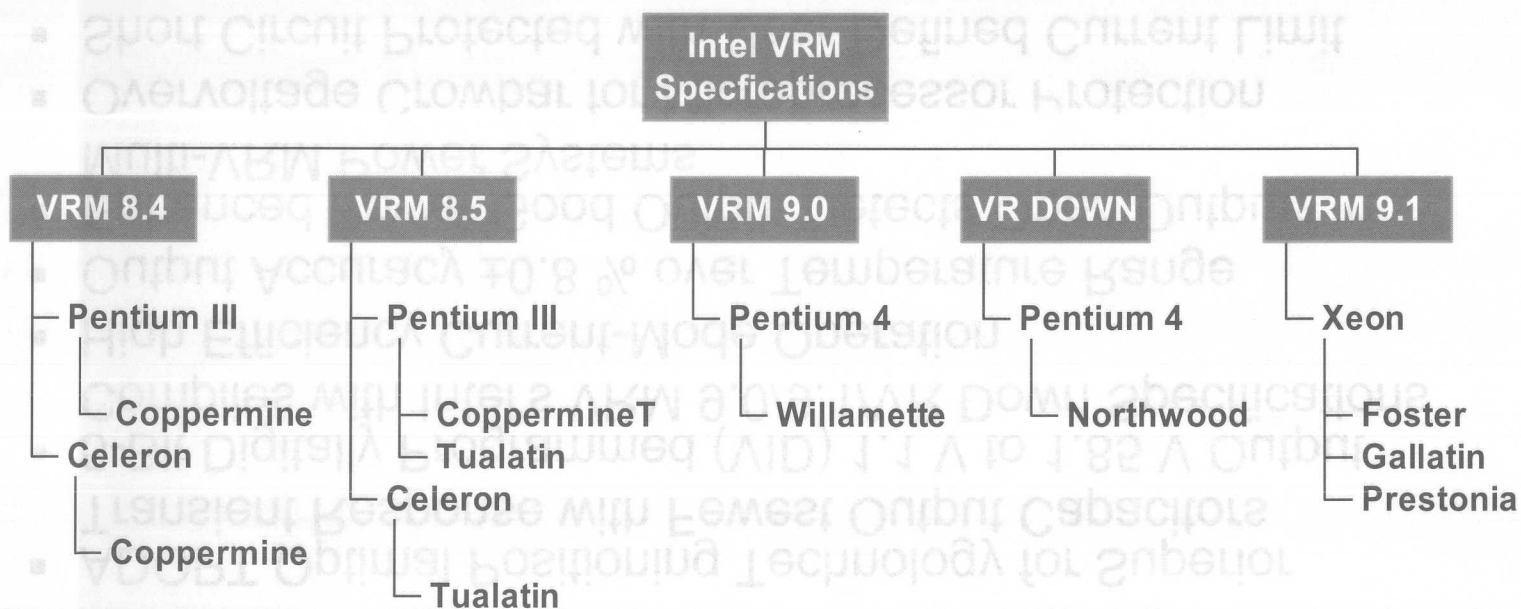
ADP3164 VRM 9.0/ 9.1/ VR Down-Compliant 4-Phase Synchronous Buck Controller



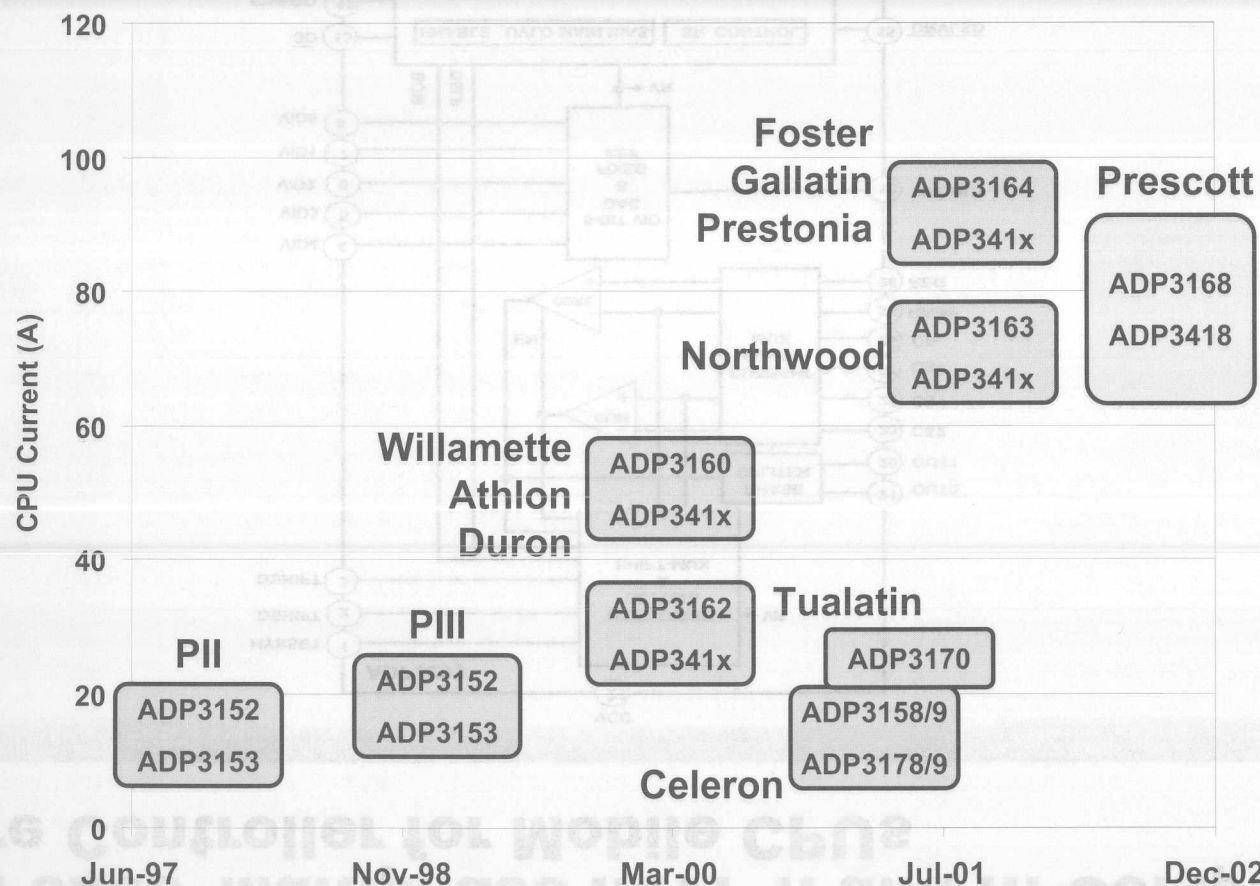
ADP3164 VRM 9.0/ 9.1/ VR Down-Compliant 4-Phase Synchronous Buck Controller

- ADOPT Optimal Positioning Technology for Superior Transient Response with Fewest Output Capacitors
- 5-Bit Digitally Programmed (VID) 1.1 V to 1.85 V Output Complies with Intel's VRM 9.0/9.1/VR Down Specifications
- High Efficiency Current-Mode Operation
- Output Accuracy $\pm 0.8\%$ over Temperature Range
- Enhanced Power Good Output Detects Open Outputs in Multi-VRM Power Systems
- Overvoltage Crowbar for Microprocessor Protection
- Short Circuit Protected with User-Defined Current Limit
- 4-Phase Operation at up to 500 kHz per Phase
- Logic-Level PWM Outputs for Interface to External High-Power Drivers
- Active Current Balancing between All Phases
- Accurate Multiple VRM Module Current Sharing

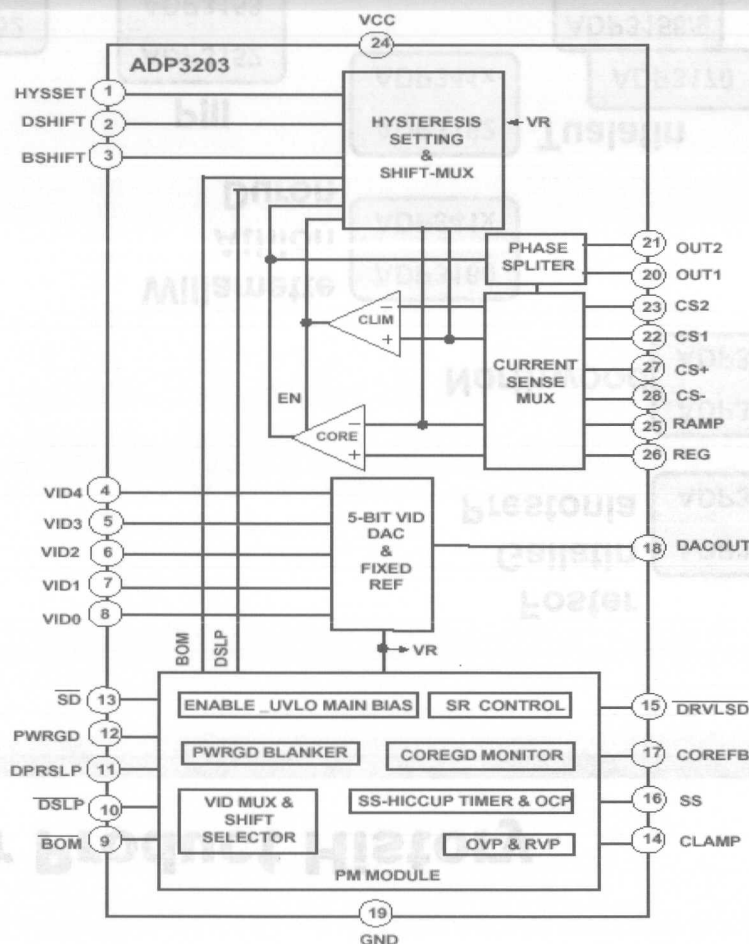
Intel's VRM Specifications



CPU Power Product History



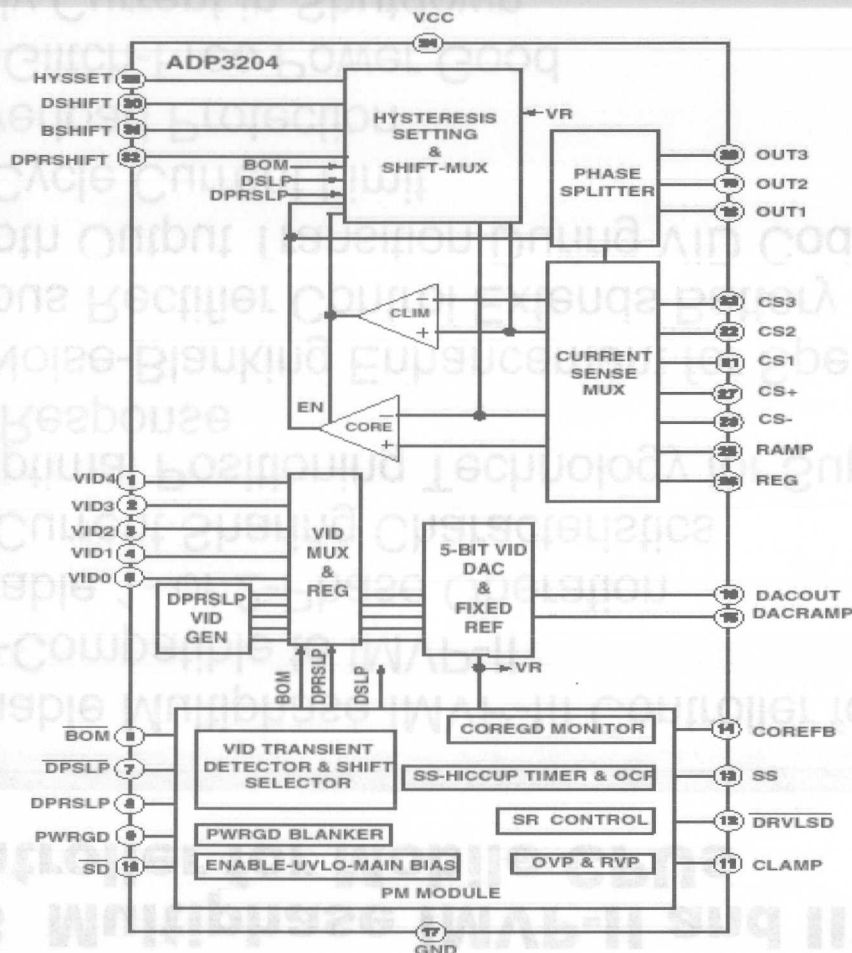
ADP3203 Multiphase IMVP-II and III-Compliant Core Controller for Mobile CPUs



ADP3203 Multiphase IMVP-II and III-Compliant Core Controller for Mobile CPUs

- Programmable Multiphase IMVP-III Controller for Mobile CPUs
- Backward-Compatible to IMVP-II
- Pin Selectable 1- or 2-Phase Operation
- Excellent Current Sharing Characteristics
- ADOPT Optimal Positioning Technology for Superior Load Transient Response
- Adaptive Noise-Blanking Enhancement for Speed and Stability
- Synchronous Rectifier Control Extends Battery Life
- Fast Smooth Output Transition During VID Code Change
- Cycle-by-Cycle Current Limit
- Hiccup Overload Protection
- Transient-Glitch-Free Power Good
- Low Supply Current in Shutdown
- Soft Start Eliminates Power-On In-Rush Current Surge
- Highly Redundant Overvoltage and Reverse-Voltage Protection

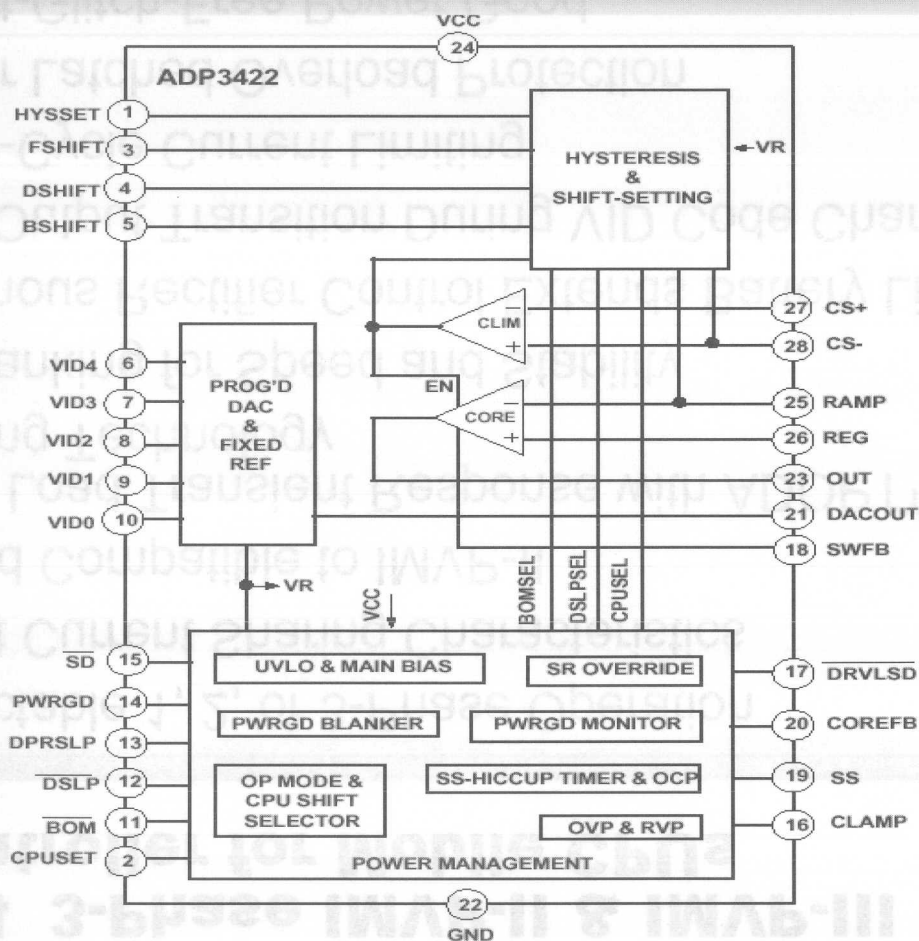
ADP3204 3-Phase IMVP-II & IMVP-III Core Controller for Mobile CPUs



ADP3204 3-Phase IMVP-II & IMVP-III Core Controller for Mobile CPUs

- Pin Selectable 1, 2, or 3-Phase Operation
- Excellent Current Sharing Characteristics
- Backward Compatible to IMVP-II
- Superior Load Transient Response with ADOPT™ Optimal Positioning Technology
- Noise-Blanking for Speed and Stability
- Synchronous Rectifier Control Extends Battery Life
- Smooth Output Transition During VID Code Change
- Cycle-by-Cycle Current Limiting
- Hiccup or Latched Overload Protection
- Transient-Glitch-Free Power Good
- Soft Start Eliminates Power-On In-Rush Current Surge
- Two-Level Over-Voltage and Reverse-Voltage Protection

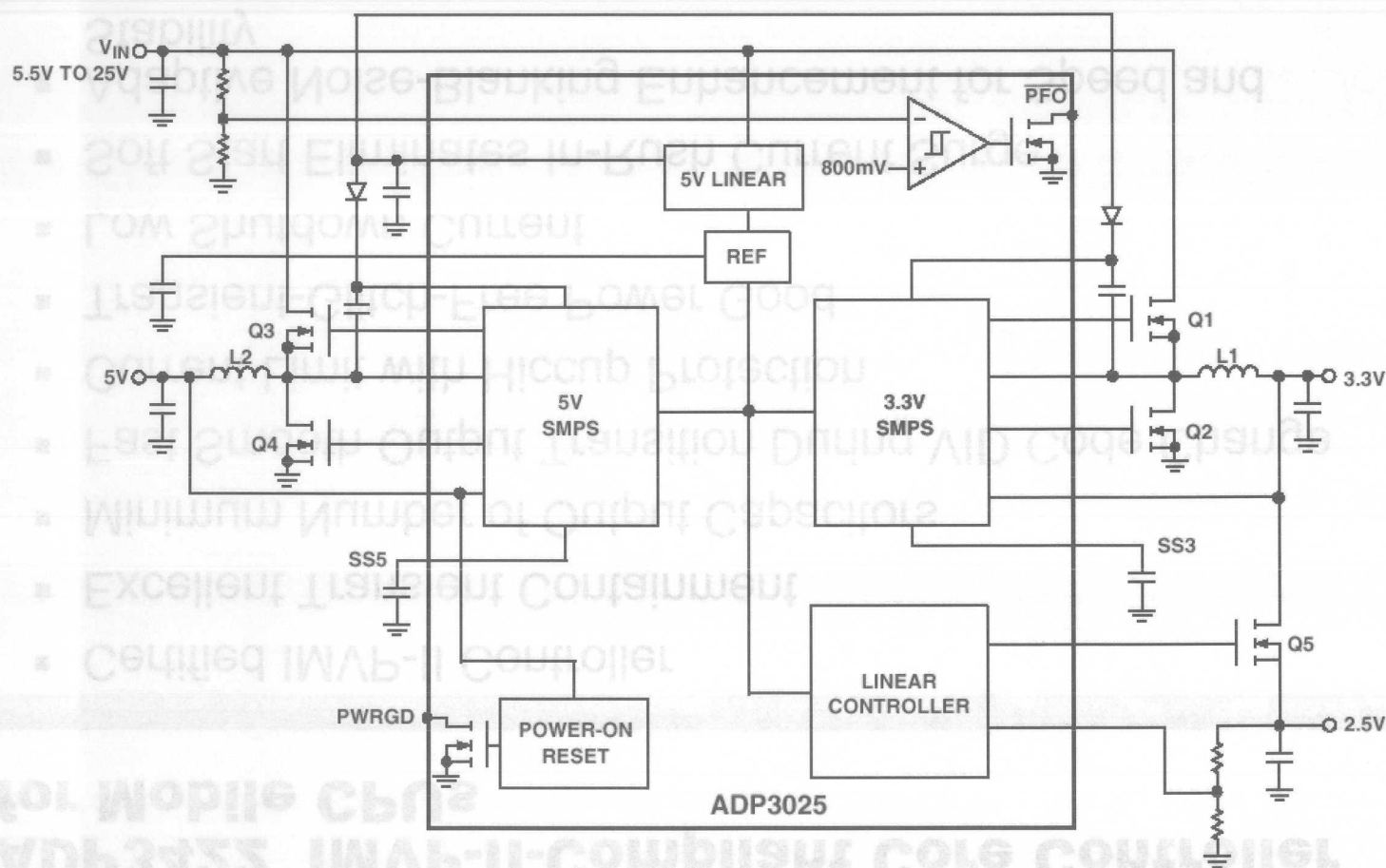
ADP3422 IMVP-II-Compliant Core Controller for Mobile CPUs



ADP3422 IMVP-II-Compliant Core Controller for Mobile CPUs

- Certified IMVP-II Controller
- Excellent Transient Containment
- Minimum Number of Output Capacitors
- Fast Smooth Output Transition During VID Code Change
- Current Limit with Hiccup Protection
- Transient-Glitch-Free Power Good
- Low Shutdown Current
- Soft Start Eliminates In-Rush Current Surge
- Adaptive Noise-Blanking Enhancement for Speed and Stability
- Highly Redundant Overvoltage and Reverse-Voltage Protection
- Controls Synchronous Rectifier for Improved Battery Life

ADP3025 High-Efficiency Notebook Computer Power Supply Controller



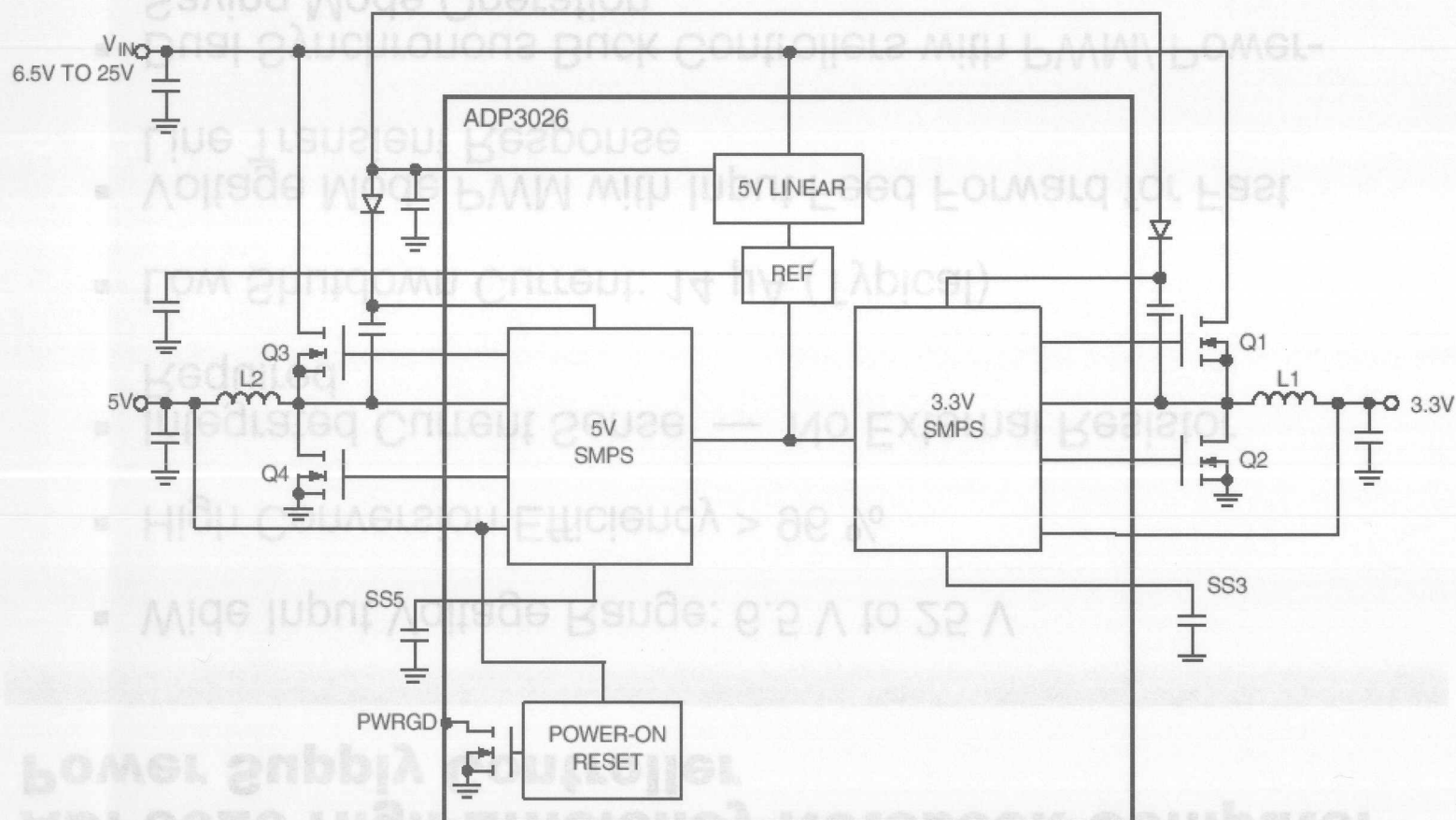
ADP3025 High-Efficiency Notebook Computer Power Supply Controller

- Wide Input Voltage Range: 4.5 V to 25 V
- High Conversion Efficiency > 96 %
- Integrated Current Sense — No External Resistor Required
- Low Shutdown Current: 14 μ A (Typical)
- Voltage Mode PWM with Input Feed Forward for Fast Line Transient Response
- Programmable PWM Frequency
- Dual Synchronous Buck Controllers with Selectable PWM/Power-Saving Mode Operation
- Built-In Gate Drive Boost Circuit for Driving External N-Channel MOSFETs

ADP3025 High-Efficiency Notebook Computer Power Supply Controller

- Two Independently Programmable Output Voltages
 - Fixed 3.3 V or Adjustable (800 mV to $V_{IN} - 0.5 \text{ V}$)
 - Fixed 5 V or Adjustable (800 mV to $V_{IN} - 0.5 \text{ V}$)
- Integrated Linear Regulator Controller
- Extensive Circuit Protection Functions
- 38-Lead TSSOP Package
- APPLICATIONS
 - Notebook Computers and PDAs
 - Portable Instruments
 - General Purpose DC-DC Converters

ADP3026 High-Efficiency Notebook Computer Power Supply Controller



ADP3026 High-Efficiency Notebook Computer Power Supply Controller

- Wide Input Voltage Range: 6.5 V to 25 V
- High Conversion Efficiency > 96 %
- Integrated Current Sense — No External Resistor Required
- Low Shutdown Current: 14 μ A (Typical)
- Voltage Mode PWM with Input Feed Forward for Fast Line Transient Response
- Dual Synchronous Buck Controllers with PWM/ Power-Saving Mode Operation
- Built-In Gate Drive Boost Circuit for Driving External N-Channel MOSFETs

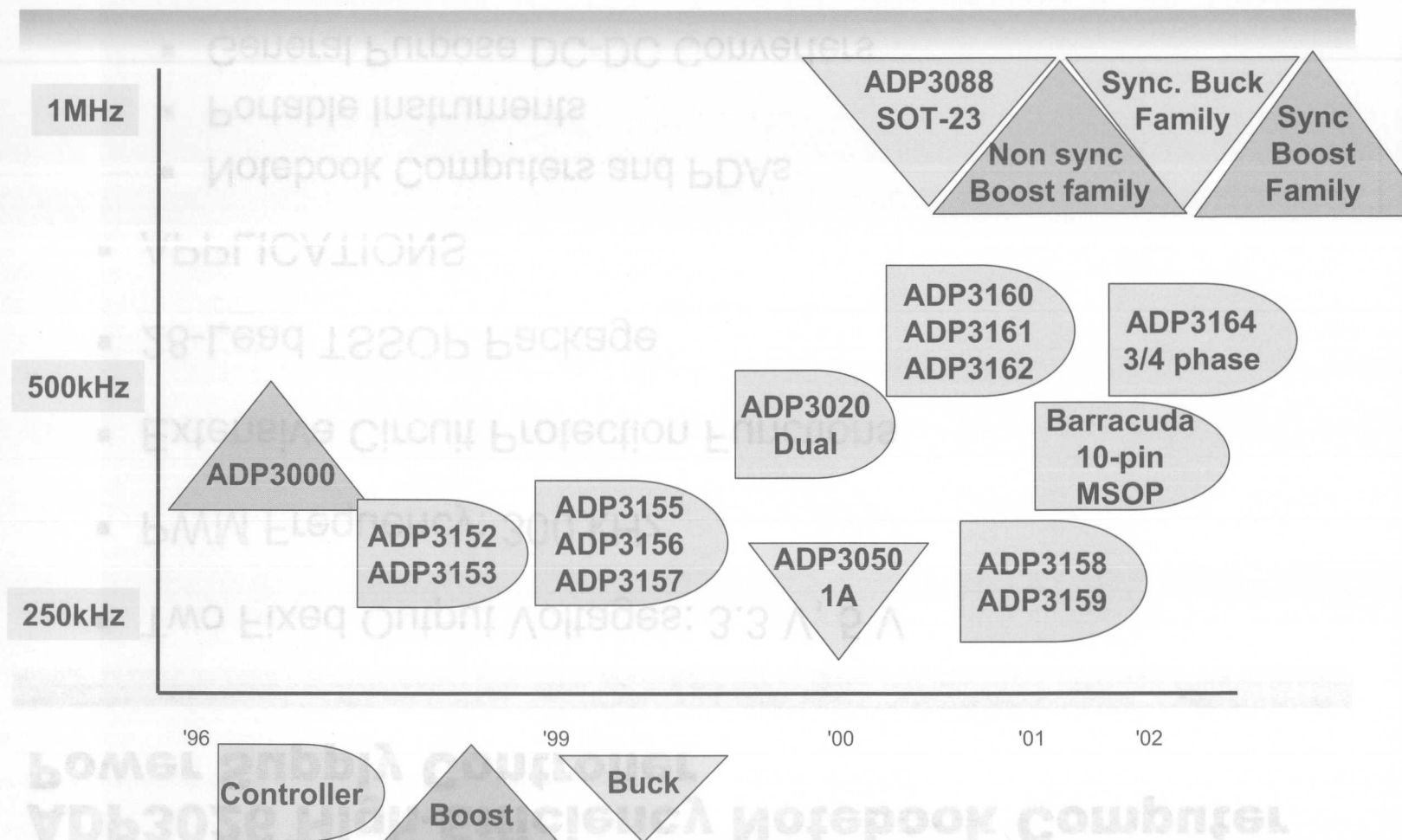
ADP3026 High-Efficiency Notebook Computer Power Supply Controller

- Two Fixed Output Voltages: 3.3 V, 5 V
- PWM Frequency: 300 kHz
- Extensive Circuit Protection Functions
- 28-Lead TSSOP Package

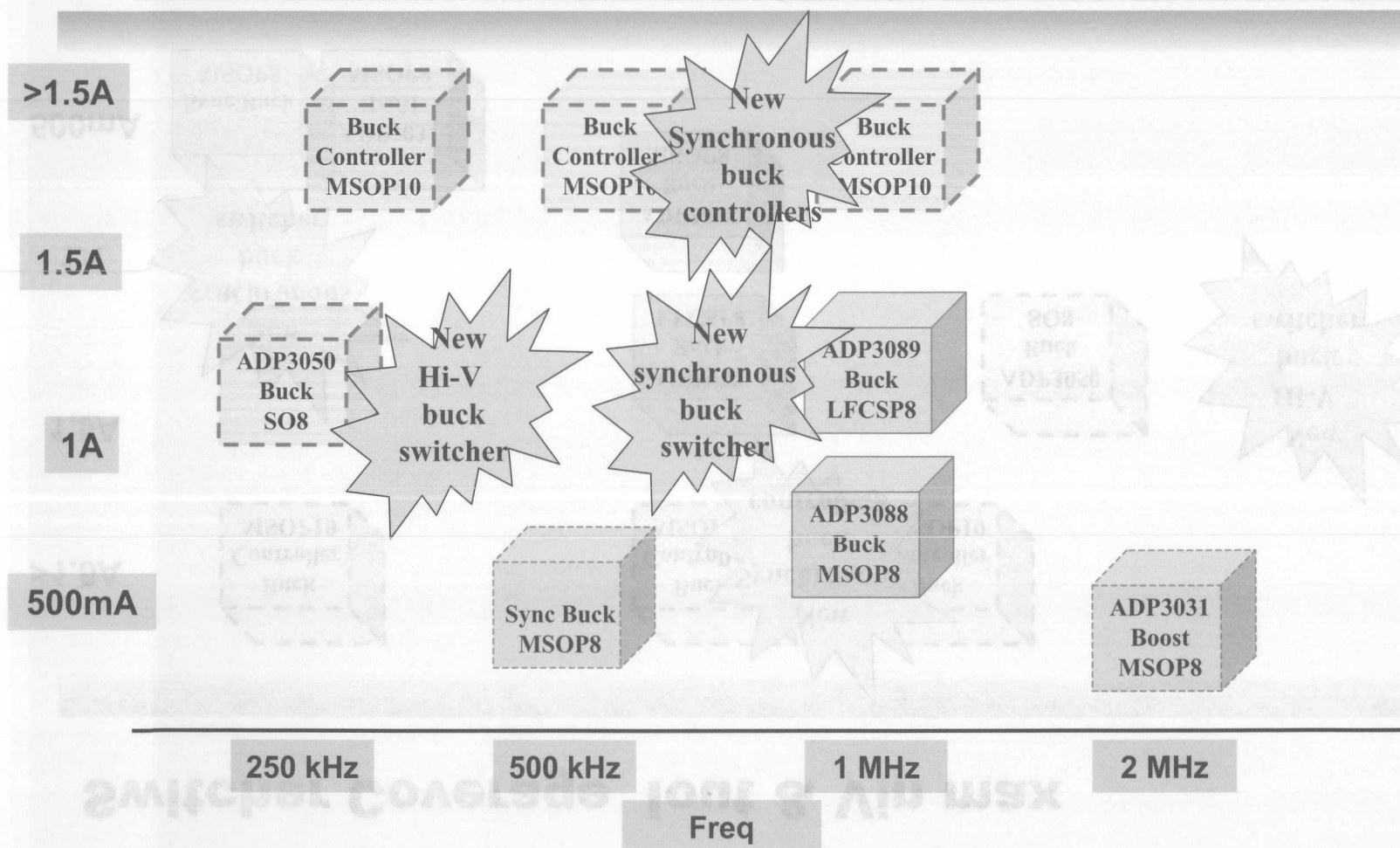
APPLICATIONS

- Notebook Computers and PDAs
- Portable Instruments
- General Purpose DC-DC Converters

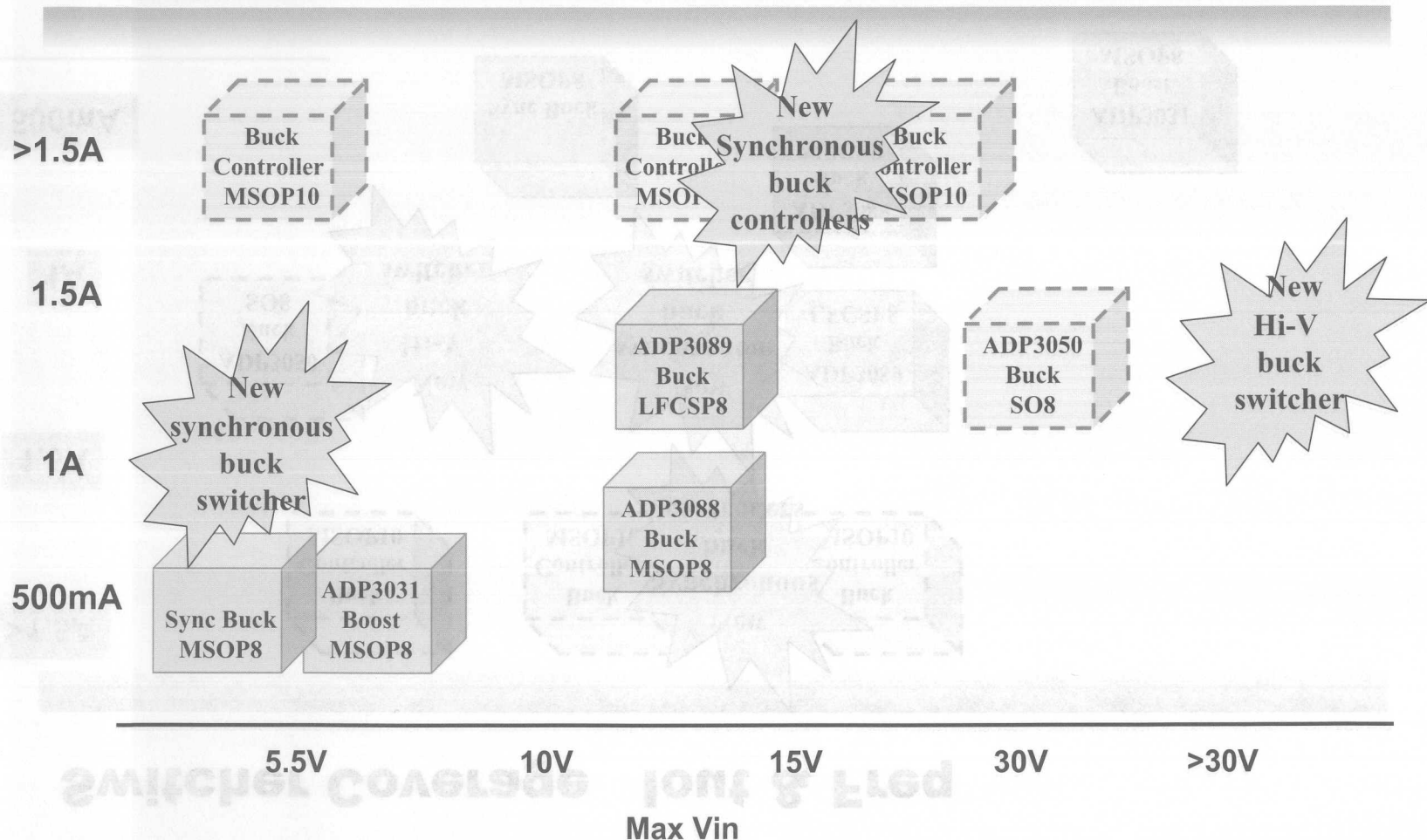
Switching Regulators and Controllers Road Map



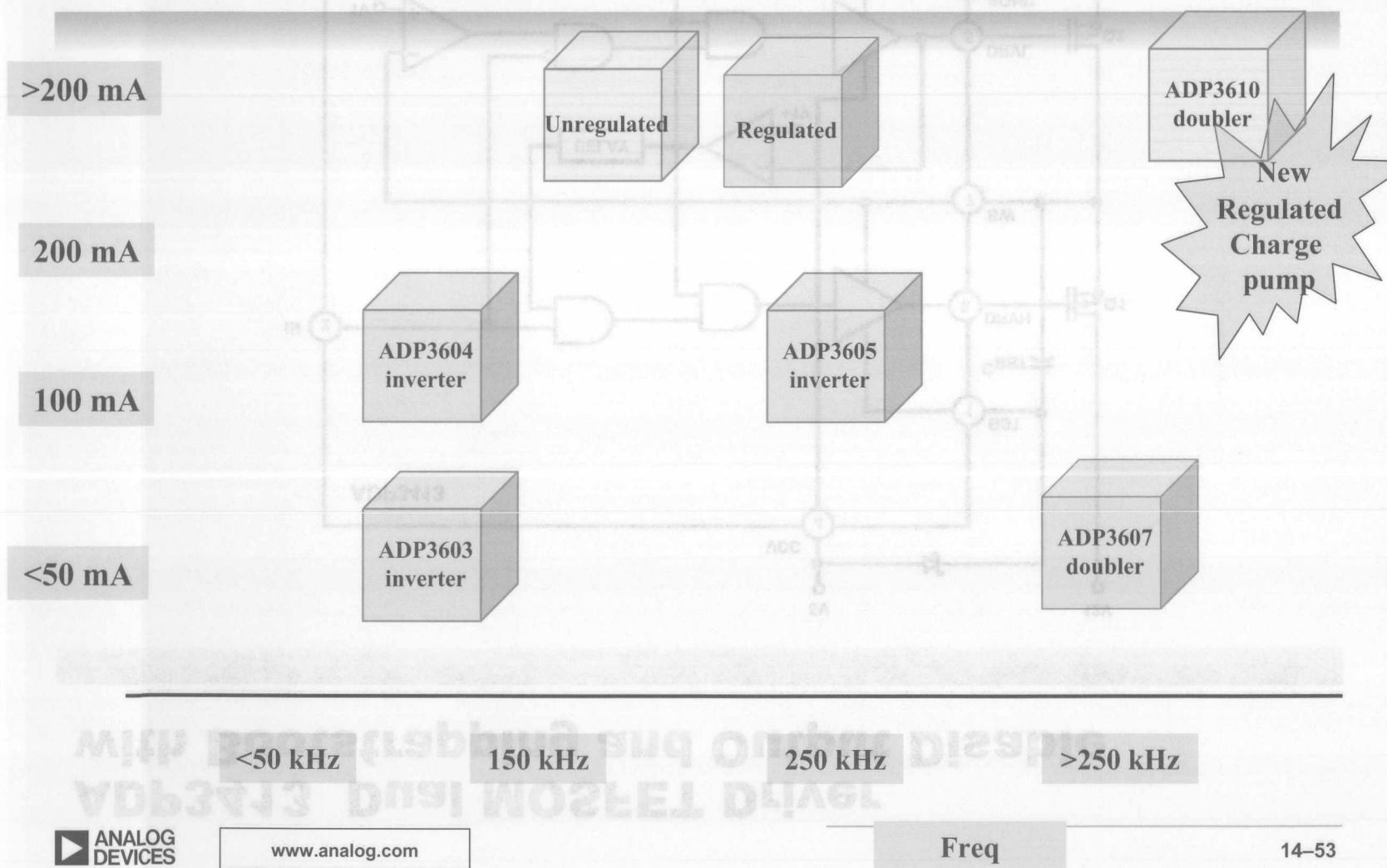
Switcher Coverage Iout & Freq



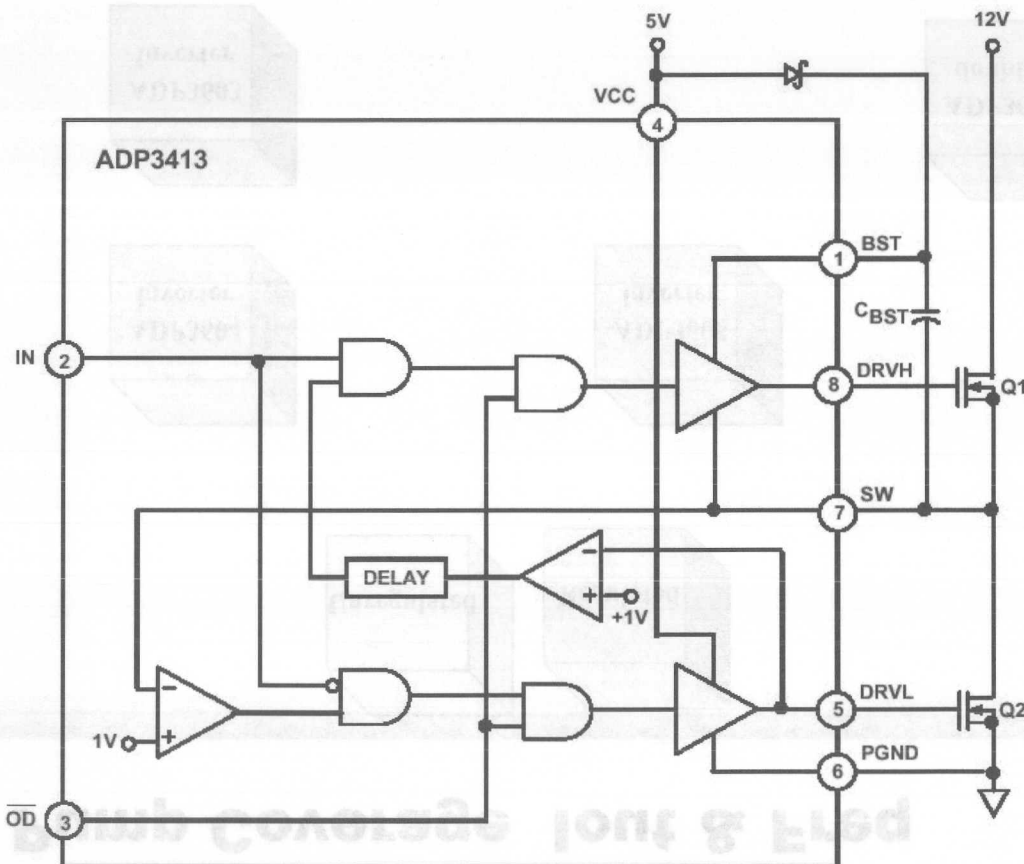
Switcher Coverage Iout & Vin max



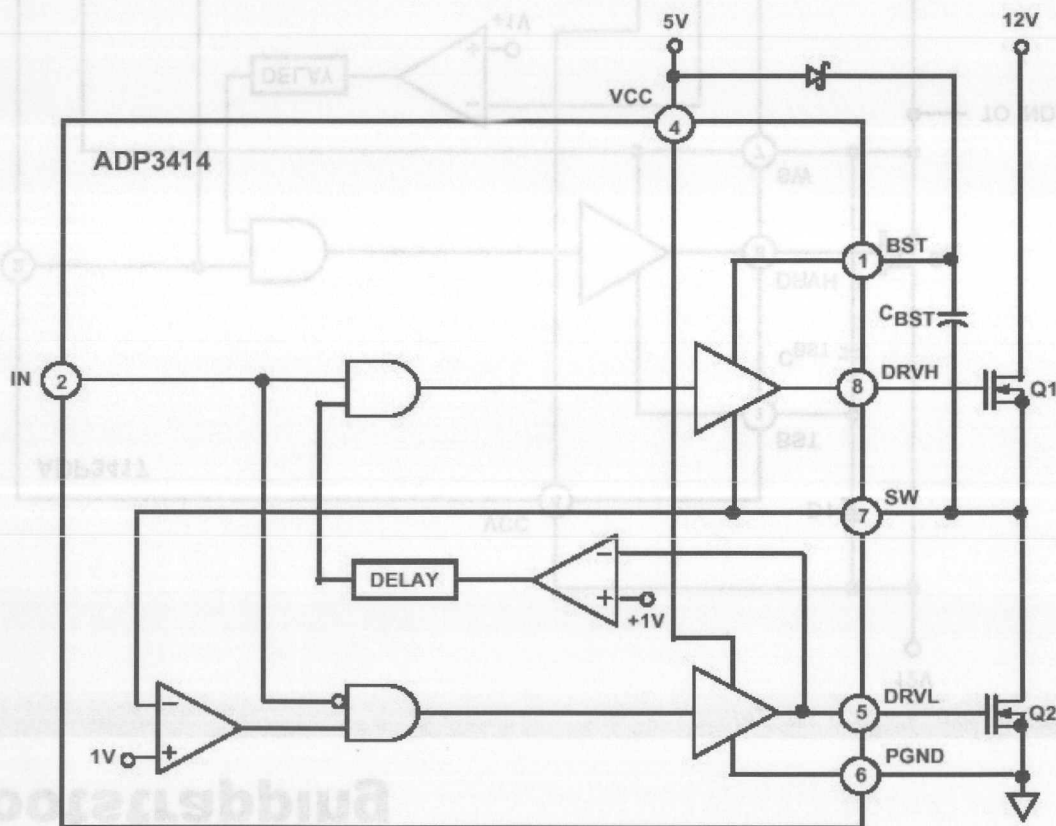
Charge Pump Coverage Iout & Freq



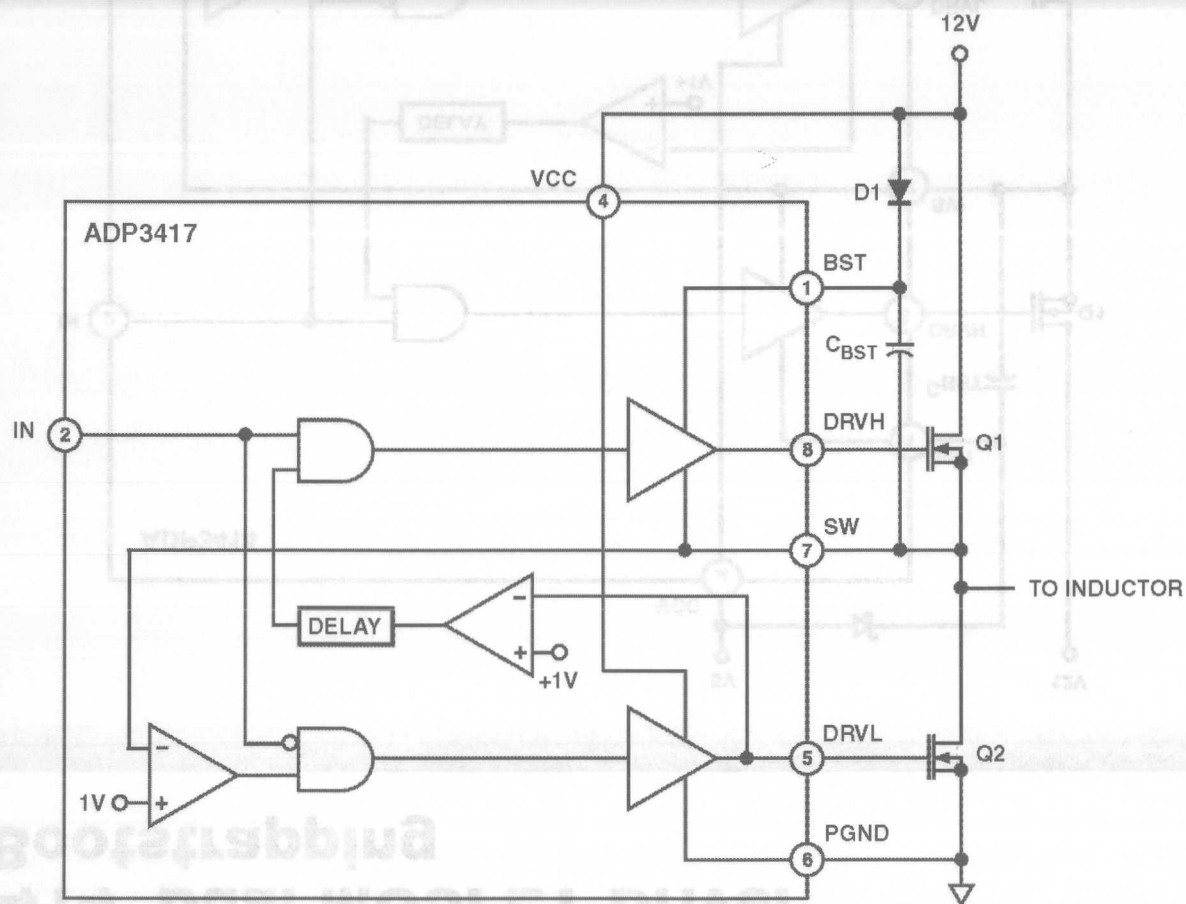
ADP3413 Dual MOSFET Driver with Bootstrapping and Output Disable



ADP3414 Dual MOSFET Driver with Bootstrapping



ADP3417 12 V Dual MOSFET Driver with Bootstrapping



ADP3413/14/17 Dual MOSFET Drivers with Bootstrapping

- All-In-One Synchronous Buck Drivers
- Bootstrapped High-Side Driver
- One PWM Signal Generates Both Drives
- Anticross Conduction Protection Circuitry
- Undervoltage Lockout
- ADP3413: Dual Driver with Output Disable
- ADP3414: Dual Driver
- ADP3417: 12 V Dual Driver

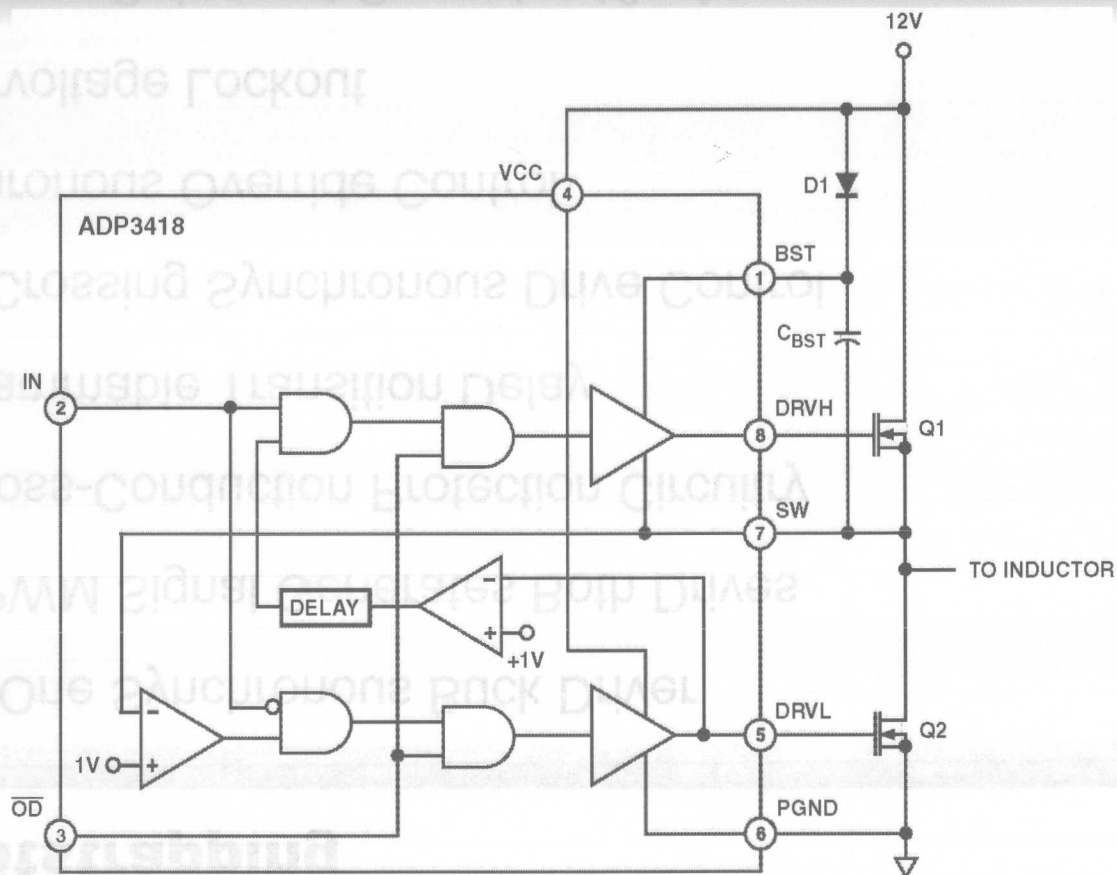
DOI: 10.1002/anie.201500015



ADP3415 Dual MOSFET Driver with Bootstrapping

- All-In-One Synchronous Buck Driver
- One PWM Signal Generates Both Drives
- Anticross-Conduction Protection Circuitry
- Programmable Transition Delay
- Zero-Crossing Synchronous Drive Control
- Synchronous Override Control
- Undervoltage Lockout
- Shutdown Quiescent Current $< 10 \mu\text{A}$

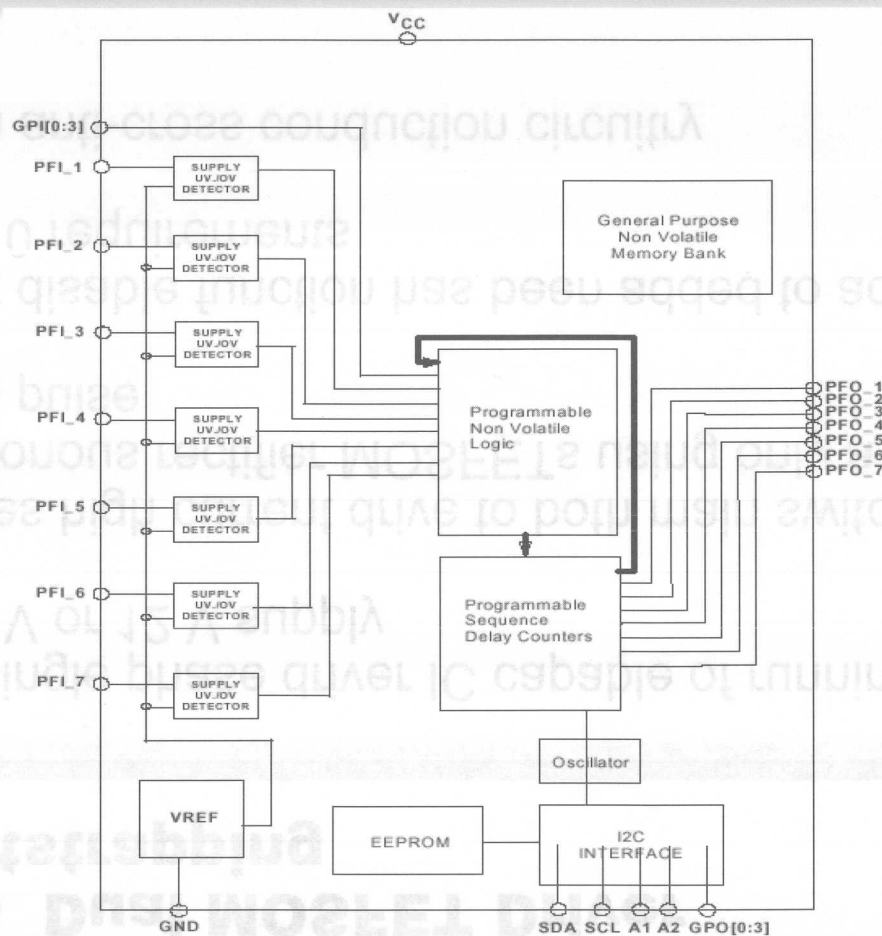
ADP3418 Dual MOSFET Driver with Bootstrapping



ADP3418 Dual MOSFET Driver with Bootstrapping

- 8-pin single phase driver IC capable of running directly off a 5 V or 12 V supply
- Supplies high current drive to both main switch and synchronous rectifier MOSFETs using only a single control pulse
- Output disable function has been added to address Intel VRM 10 requirements
- Built-in anti-cross conduction circuitry

ADM1060 Communications System Supervisory/Sequencing Circuit



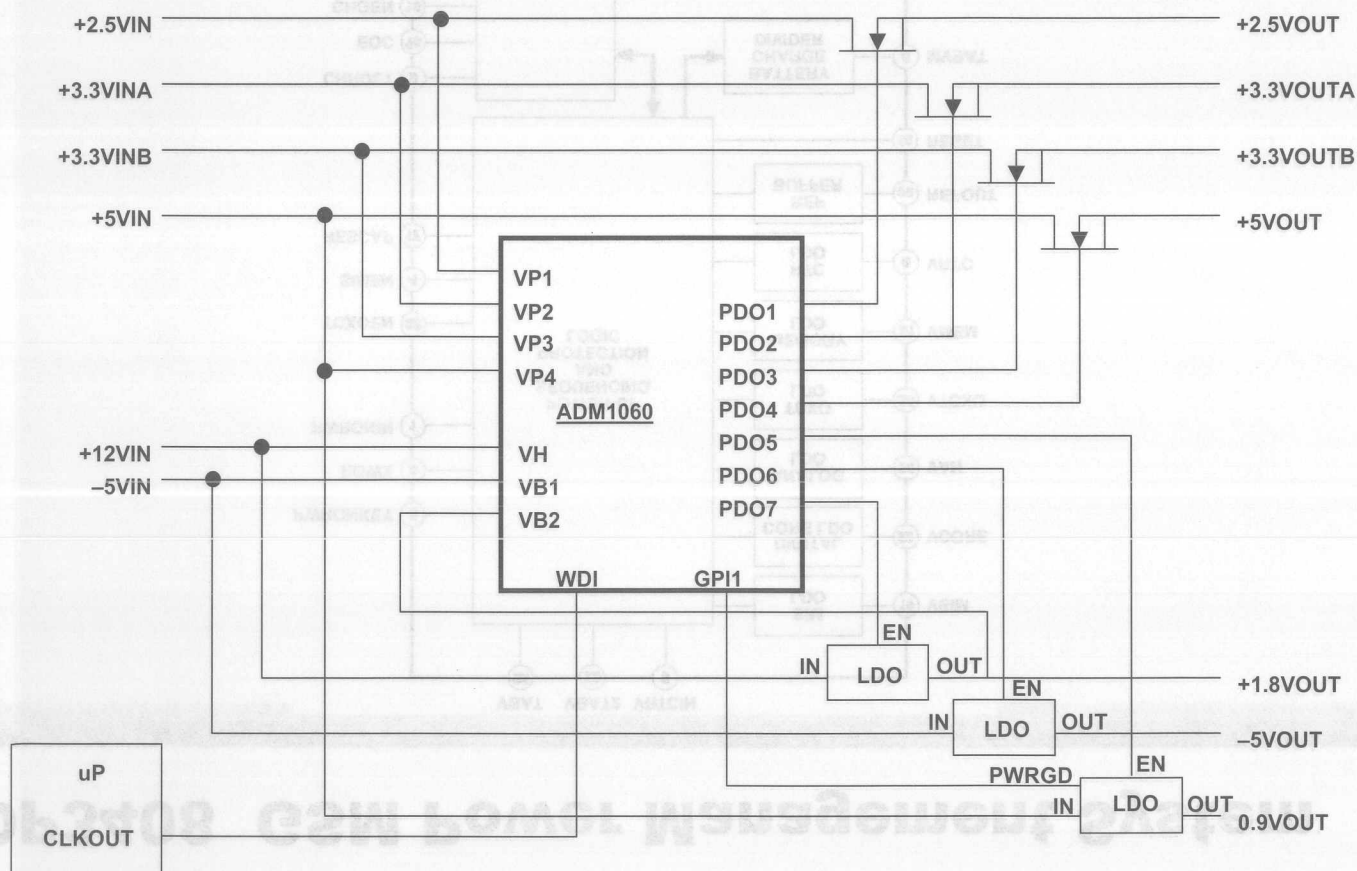
ADM1060 Communications System Supervisory/Sequencing Circuit

- Seven Programmable Supply Fault Detectors
 - +12 V
 - Programmable –5 V to 0 V
 - Five programmable 0 V to 5 V
 - Programmable power fail input thresholds (0.9 V to 5.5 V, 19.5 mV resolution)
- Precision ($\pm 2.5\%$) Monitoring of the Inputs
- Four General-Purpose Logic Inputs
- Nine Programmable Driver Outputs
- I²C-Compatible SMBus
- Device Powered by Highest of V_H or V_{P_N} Inputs
- Watchdog Detector
- 512 Bytes of EEPROM

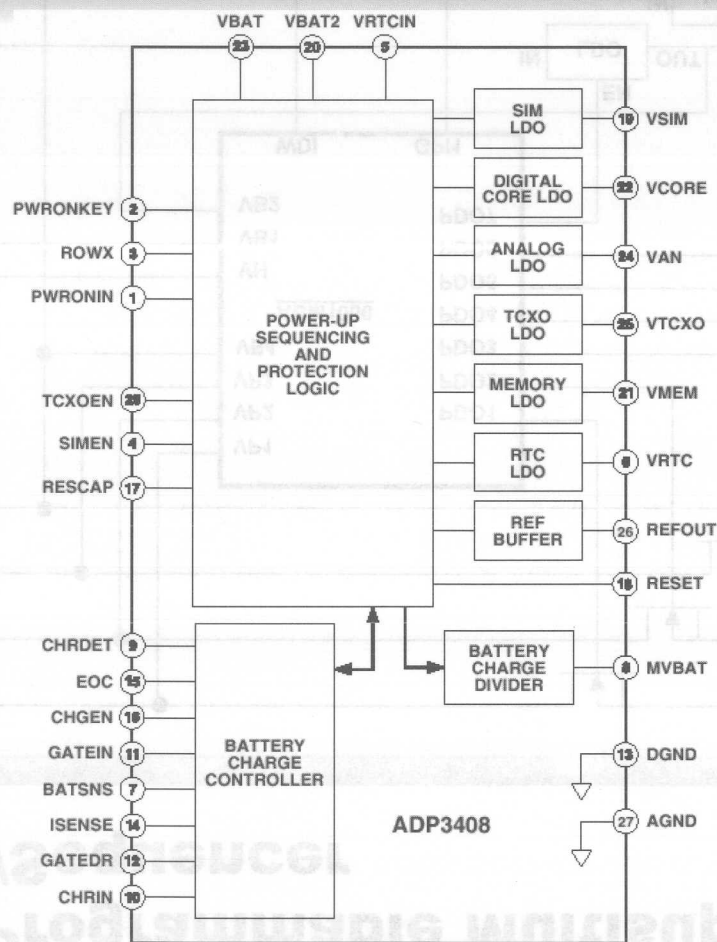
ADM1060 Communications System Supervisory/Sequencing Circuit

- Programmable Sequencing of Seven Power Fail Outputs and Four General-Purpose Outputs for Both Power-Up and Power-Down
- Programmable Output Drive of Seven Power Fail Outputs
 - Open collector
 - Open collector with internal pull-up to VCC
 - Open collector with internal pull-up to PFI_X
 - Internally charged pumped high drive (for use with external N-channel FETS)
- Applications
 - Central office systems
 - Servers
 - Routers
 - Multisupply boards

ADM1060 Programmable Multisupply Supervisor/Sequencer



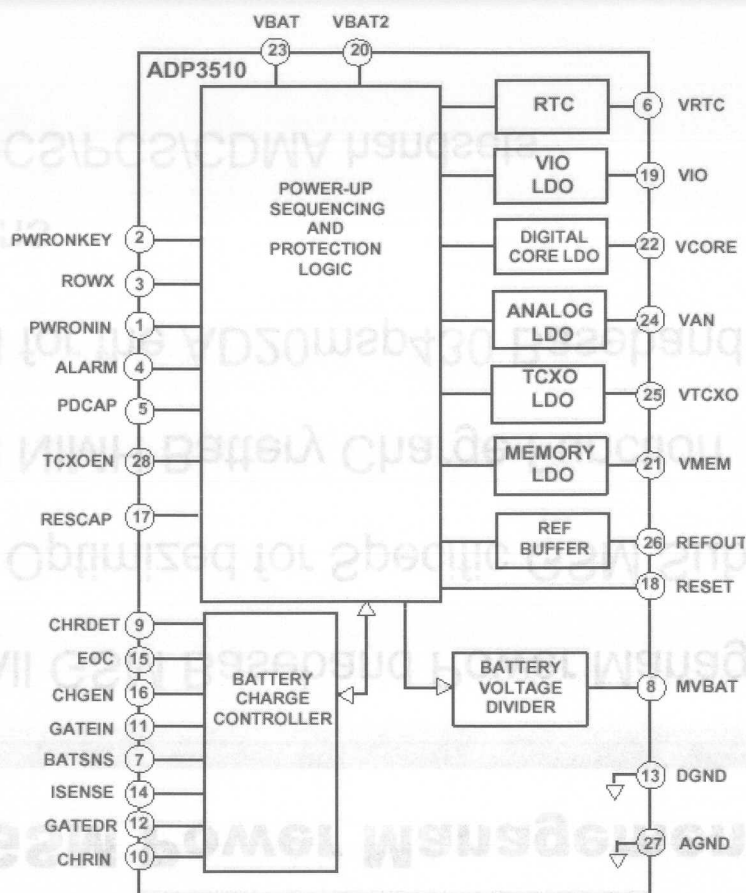
ADP3408 GSM Power Management System



ADP3408 GSM Power Management System

- Handles All GSM Baseband Power Management
- Six LDOs Optimized for Specific GSM Subsystems
- Li-Ion and NiMH Battery Charge Function
- Optimized for the AD20msp430 Baseband Chipset
- Applications
 - GSM/DCS/PCS/CDMA handsets

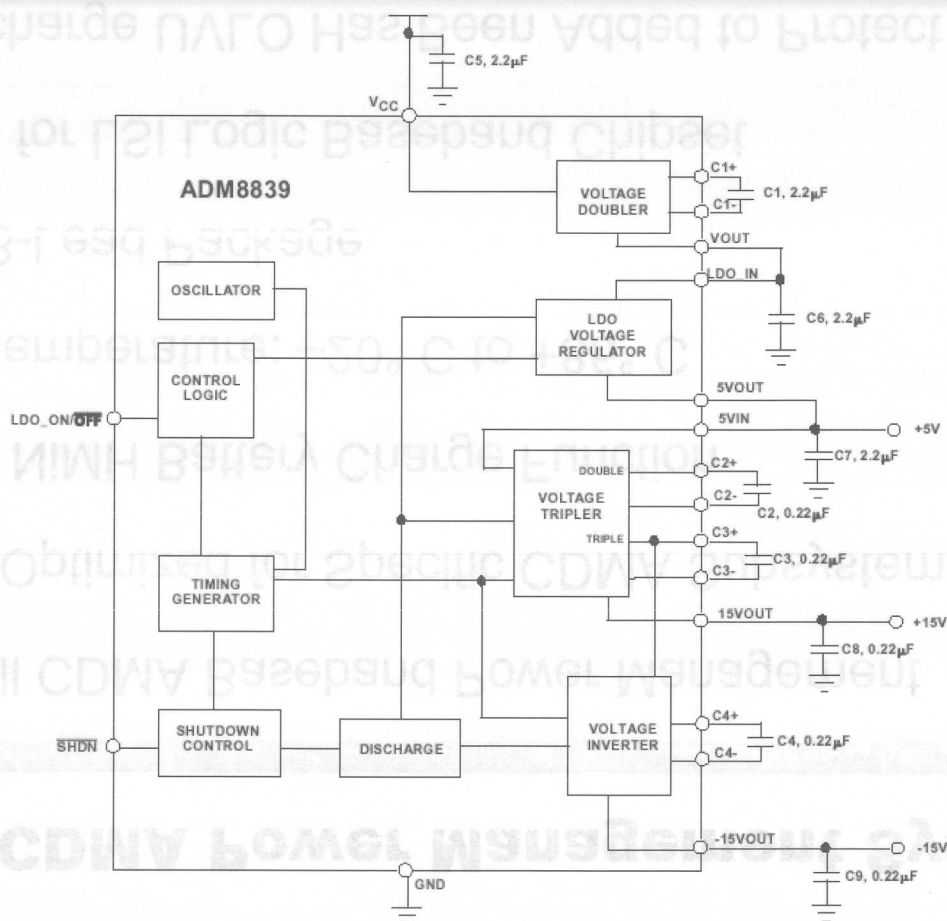
ADP3510 CDMA Power Management System



ADP3510 CDMA Power Management System

- Handles all CDMA Baseband Power Management
- Six LDOs Optimized for Specific CDMA Subsystems
- Li-Ion and NiMH Battery Charge Function
- Ambient Temperature: -20°C to $+85^{\circ}\text{C}$
- TSSOP 28-Lead Package
- Optimized for LSI Logic Baseband Chipset
- Deep Discharge UVLO Has Been Added to Protect the Battery from Fatal Discharge Damage

ADM8839 Charge Pump Regulator for Color TFT Panel

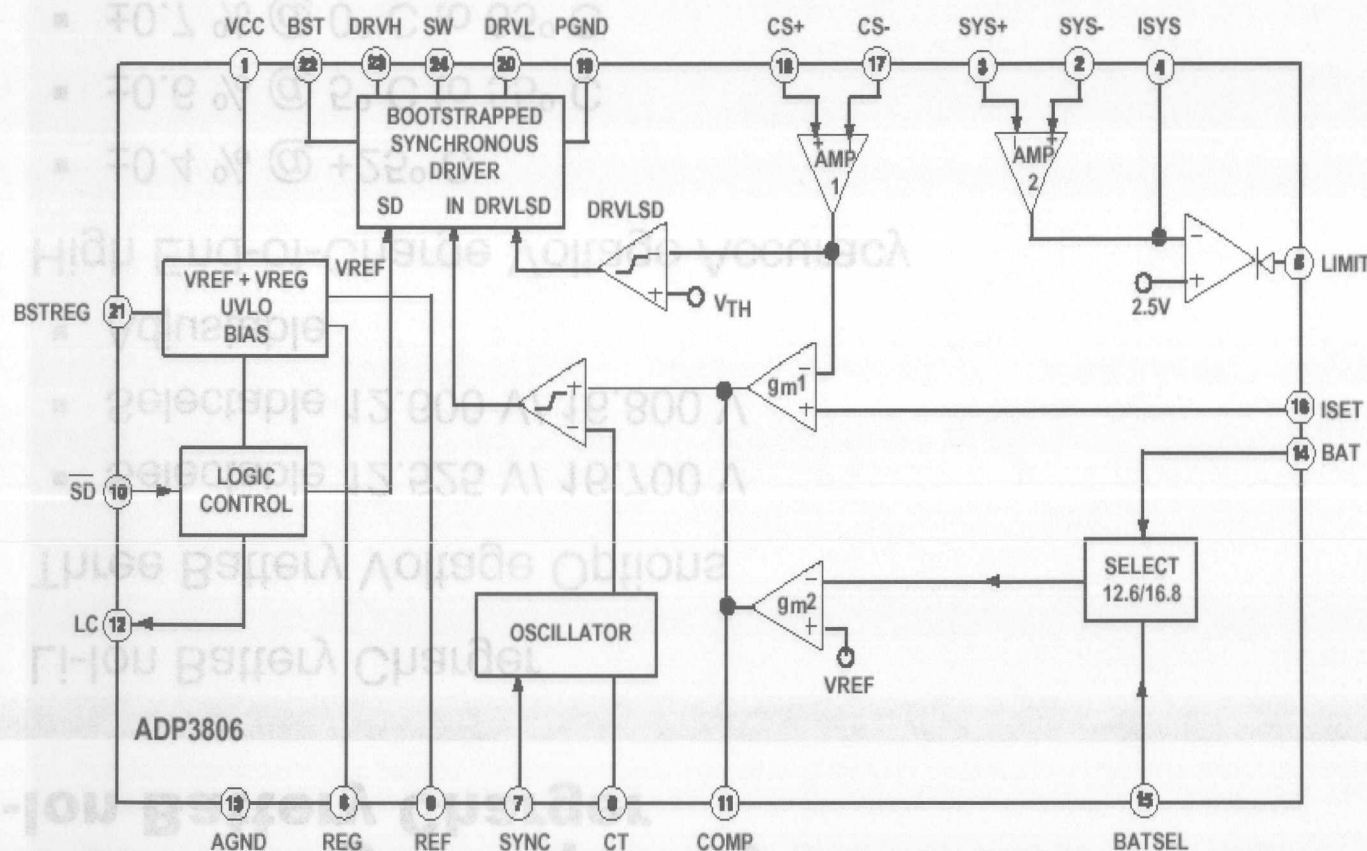


ADM8839 Charge Pump Regulator for Color TFT Panel

- 3 Voltages (5 V, 15 V, -15 V) from one 3 V Supply
- Power Efficiency optimised for use with TFT in mobile phones
- Low Quiescent Current
- Low Shutdown Current (<1 μ A)
- Shutdown Function
- Option to use external LDO

BATTERY CHARGERS

ADP3806 High-Frequency Switched-Mode Li-Ion Battery Charger



ADP3806 High-Frequency Switched-Mode Li-Ion Battery Charger

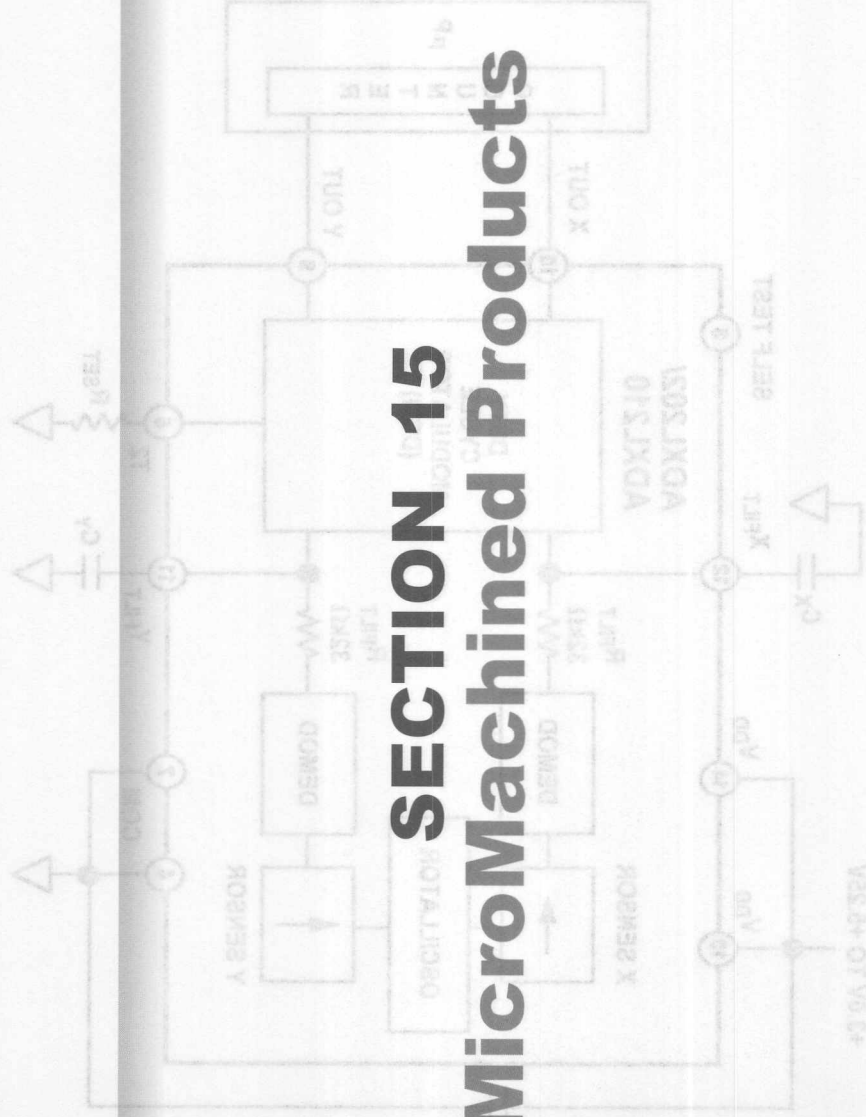
- Li-Ion Battery Charger
- Three Battery Voltage Options
 - Selectable 12.525 V/ 16.700 V
 - Selectable 12.600 V/ 16.800 V
 - Adjustable
- High End-of-Charge Voltage Accuracy
 - $\pm 0.4\%$ @ $+25^{\circ}\text{C}$
 - $\pm 0.6\%$ @ 5°C to 55°C
 - $\pm 0.7\%$ @ 0°C to 85°C
- Programmable Charge Current with Rail-to-Rail Sensing

ADP3806 High-Frequency Switched-Mode Li-Ion Battery Charger

- System Current Sense with Reverse Input Protection
- Softstart Charge Current
- Undervoltage Lockout
- Bootstrapped Synchronous Drive for External NMOS
- Programmable Oscillator Frequency
- Oscillator SYNC Pin
- Low Current Flag
- Trickle Charge

- Tickle Charge
- Low Current Flag
- Oscillator SYNC Pin
- Programmable Oscillator Frequency
- Bootstrapped Synchronous Drive for External I/MOS
- Undervoltage Lockout
- Softstart Charge Current
- System Current Sense with Reverse Input Protection

Li-Ion Battery Charger ADP3806 High-Frequency Switched-Mode

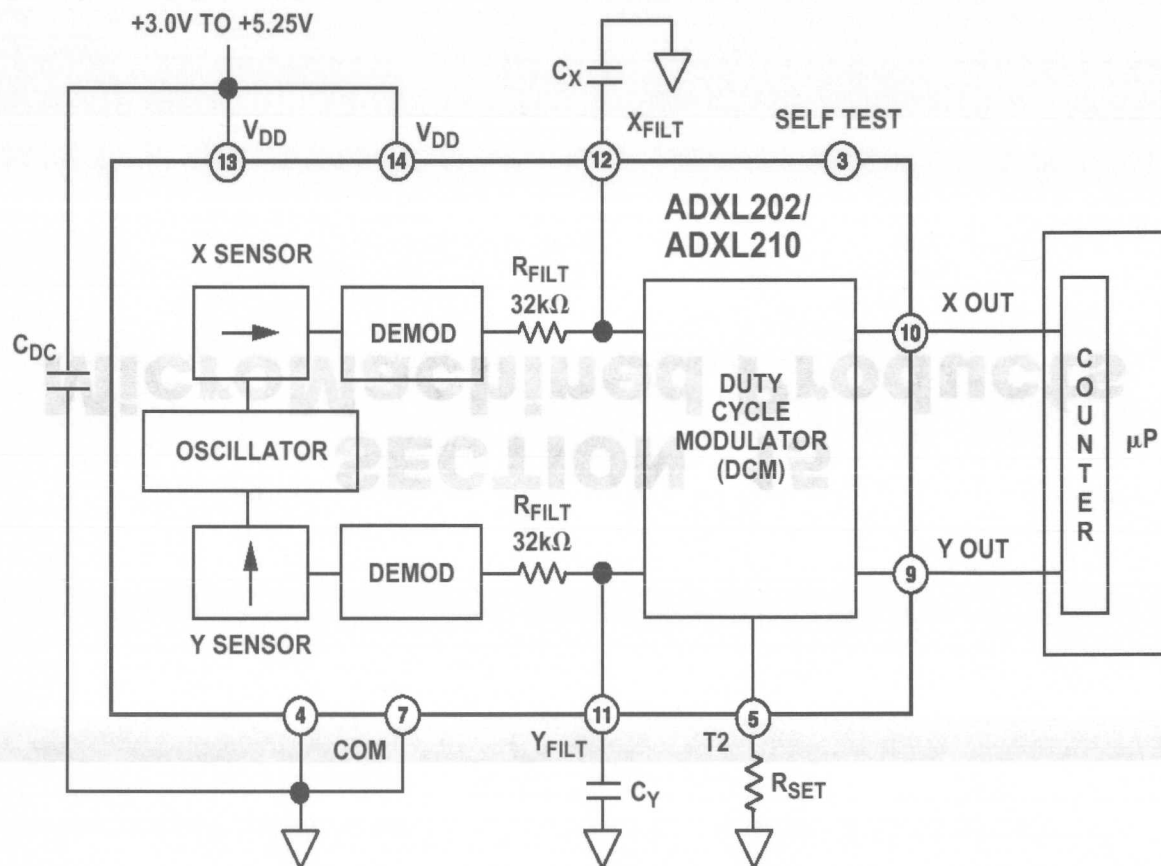


SECTION 15

MicroMachined Products

Accelerometer with Duty Cycle Output
ADXL505E Low-Cost $\pm 5g$ Dual-Axis

ADXL202E Low-Cost ± 2 g Dual-Axis Accelerometer with Duty Cycle Output



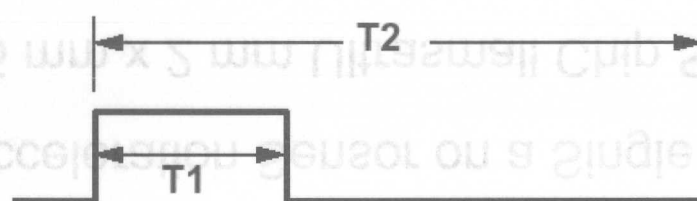
ADXL202E Low-Cost ± 2 g Dual-Axis Accelerometer with Duty Cycle Output

- 2-Axis Acceleration Sensor on a Single IC Chip
- 5 mm x 5 mm x 2 mm Ultrasmall Chip Scale Package
- 2 mg Resolution at 60 Hz
- Low-Power: <0.6 mA
- Direct Interface to Low-Cost Microcontrollers via Duty Cycle Output
- BW Adjustment with Single Capacitor
- 3 V to 5.25 V Single Supply Operation
- 1000 g Shock Survival

ADXL202E Low-Cost ± 2 g Dual-Axis Accelerometer with Duty Cycle Output

Features

- 5 mg resolution
- Duty cycle output
- 0.6 mA current consumption
- 3 V to 5.25 V single supply
- BW adjustment with single capacitor

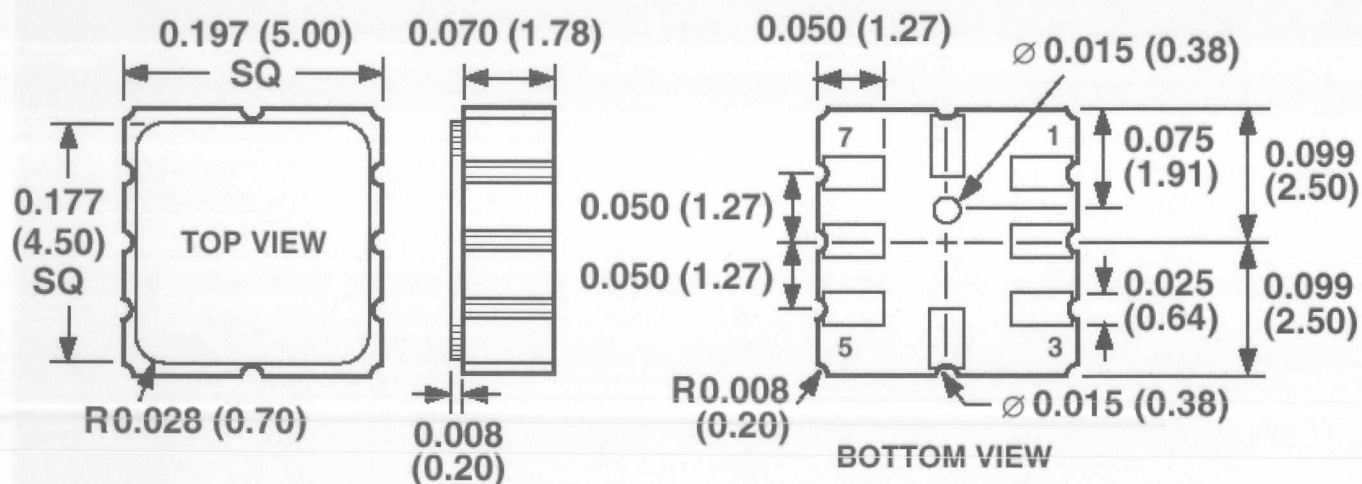


$$A(g) = (T_1/T_2 - 0.5)/12.5\%$$

$$0g = 50\% \text{ DUTY CYCLE}$$

$$T_2 = R_{SET}/125M\Omega$$

8-Terminal Ceramic Leadless Chip Carrier (E-8)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS

CONTROLLING DIMENSIONS ARE IN MILLIMETERS



8-Terminal Ceramic Resistor Chip Carrier (E-8)

SECTION 16

Modules



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16-2

High Performance “Multichip” ADC Solutions

SECTION 16



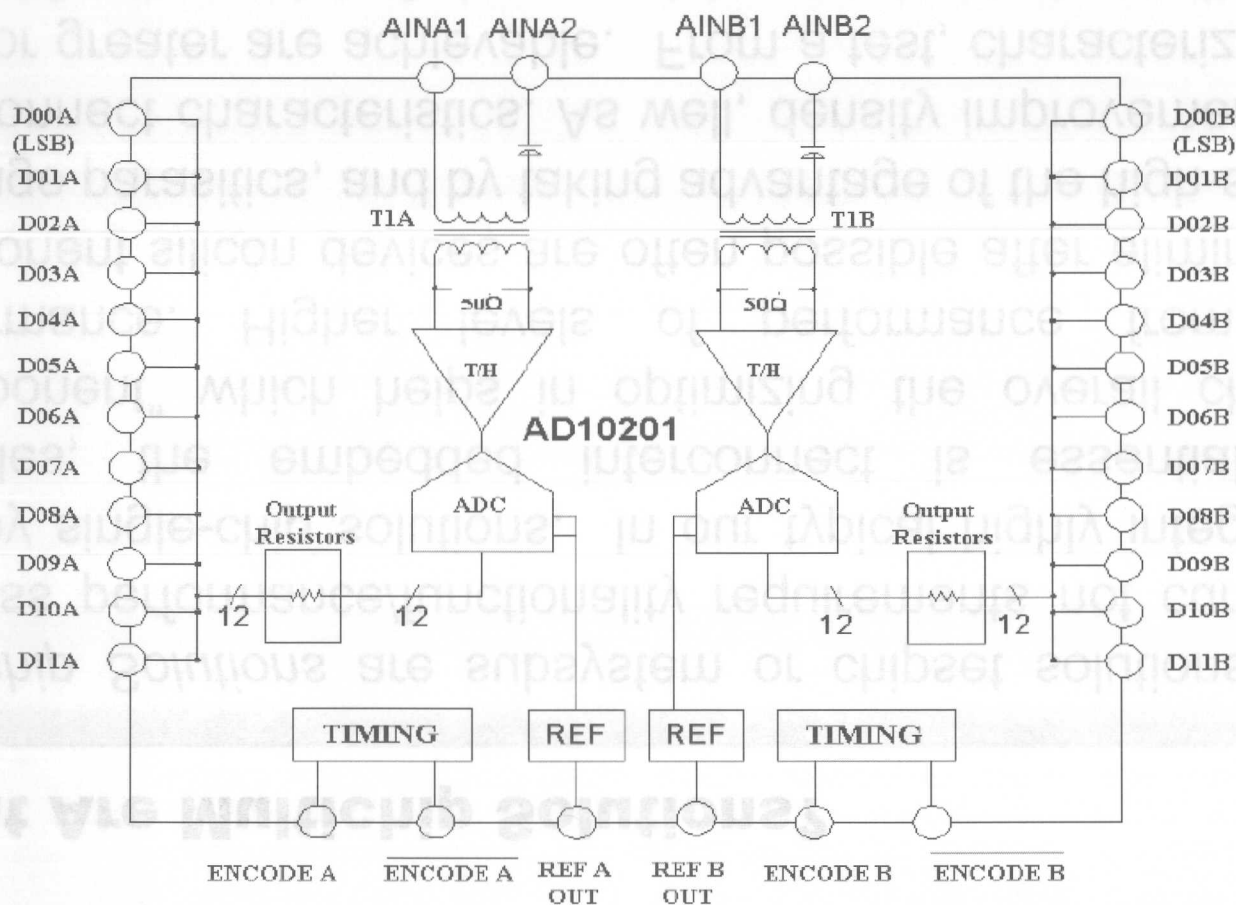
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16-2

What Are Multichip Solutions?

Multichip Solutions are subsystem or chipset solutions that address performance/functionality requirements not currently met by single-chip solutions. In our typical highly integrated modules, the embedded interconnect is essentially a “component” which helps in optimizing the overall chipset performance. Higher levels of performance from the component silicon devices are often possible after eliminating package parasitics, and by taking advantage of the high-speed interconnect characteristics. As well, density improvements of 50% or greater are achievable. From a test, characterization, or qualification point of view, modules are treated equally with monolithic components. *Multichip Solutions* are available as standard products or custom developments.

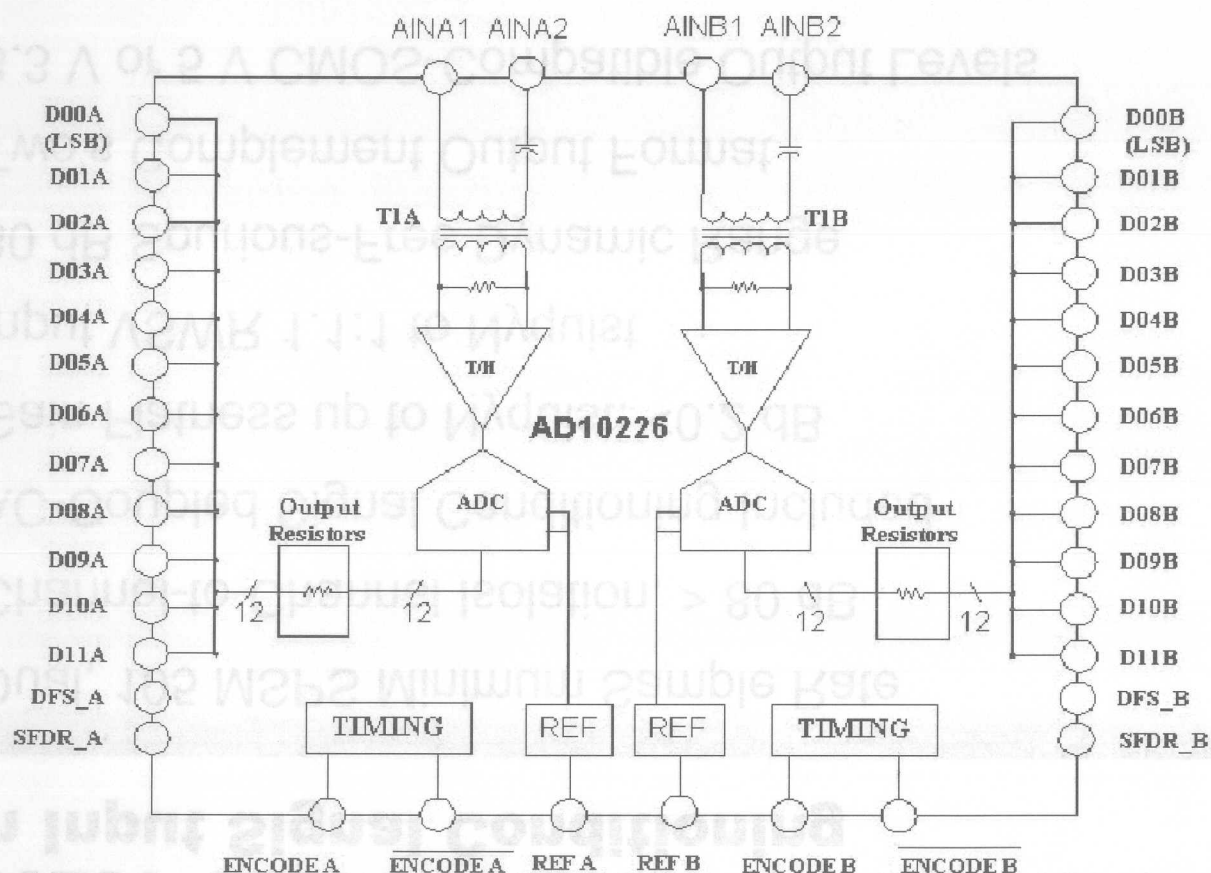
AD10201 Dual Channel 12-Bit 105 MSPS ADC with Input Signal Conditioning



AD10201 Dual Channel 12-Bit 105 MSPS ADC with Input Signal Conditioning

- Dual, 105 MSPS Minimum Sample Rate
- Channel-to-Channel Isolation, > 80 dB
- AC-Coupled Signal Conditioning Included
- Gain Flatness up to Nyquist: <0.2 dB
- Input VSWR 1.1:1 to Nyquist
- 80 dB Spurious-Free Dynamic Range
- Two's Complement Output Format
- 3.3 V or 5 V CMOS-Compatible Output Levels
- 0.850 W Per Channel
- Industrial and Military Grade

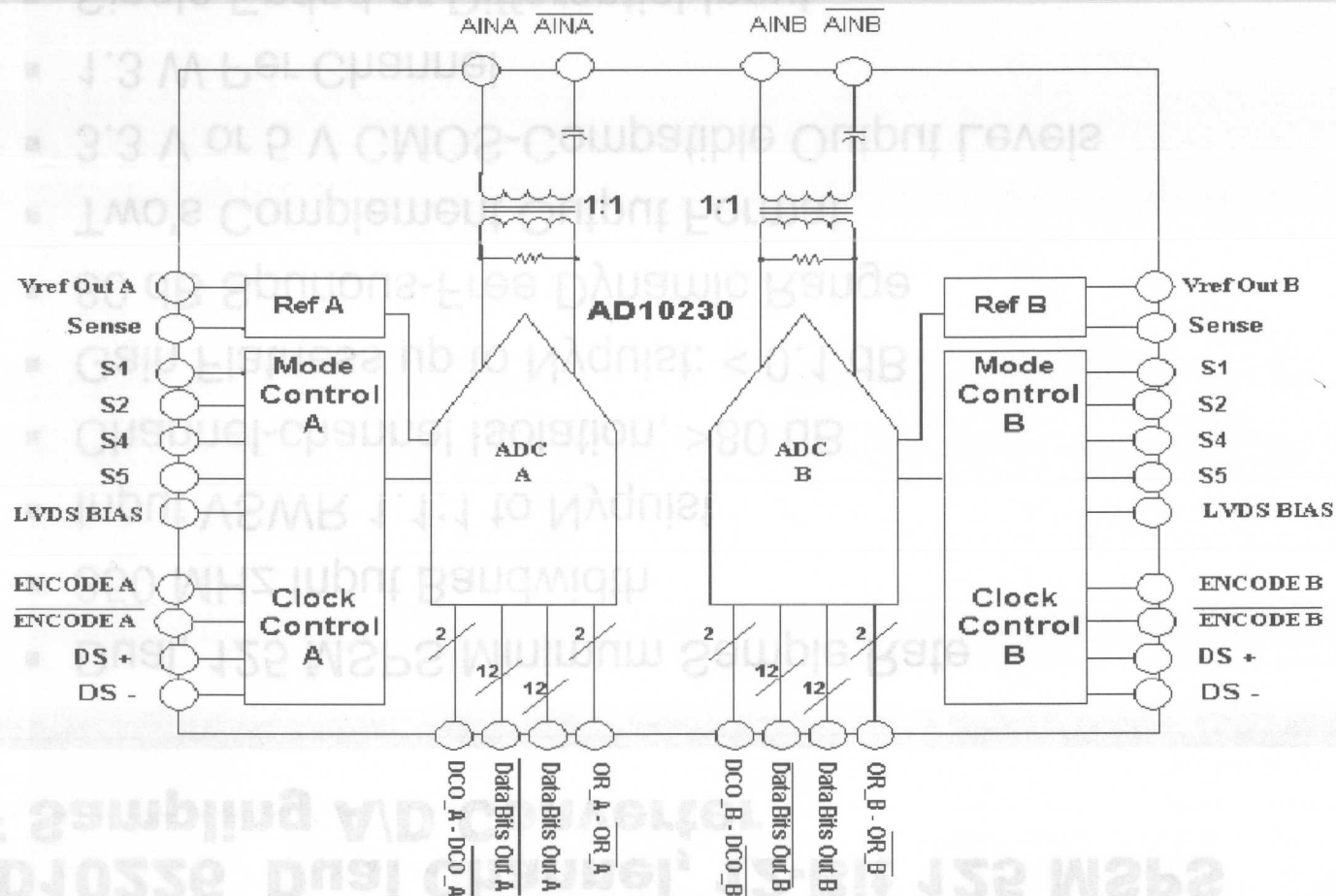
AD10226 Dual Channel, 12-Bit 125 MSPS IF Sampling A/D Converter



AD10226 Dual Channel, 12-Bit 125 MSPS IF Sampling A/D Converter

- Dual, 125 MSPS Minimum Sample Rate
- 350 MHz Input Bandwidth
- Input VSWR 1.1:1 to Nyquist
- Channel-channel Isolation, >80 dB
- Gain Flatness up to Nyquist: < 0.1 dB
- 80 dB Spurious-Free Dynamic Range
- Two's Complement Output Format
- 3.3 V or 5 V CMOS-Compatible Output Levels
- 1.3 W Per Channel
- Single Ended or Differential Input
 - AC Coupled Signal Conditioning Included
- Commercial Grade

AD10230 Dual Channel, 12-Bit 170 MSPS A/D Converter



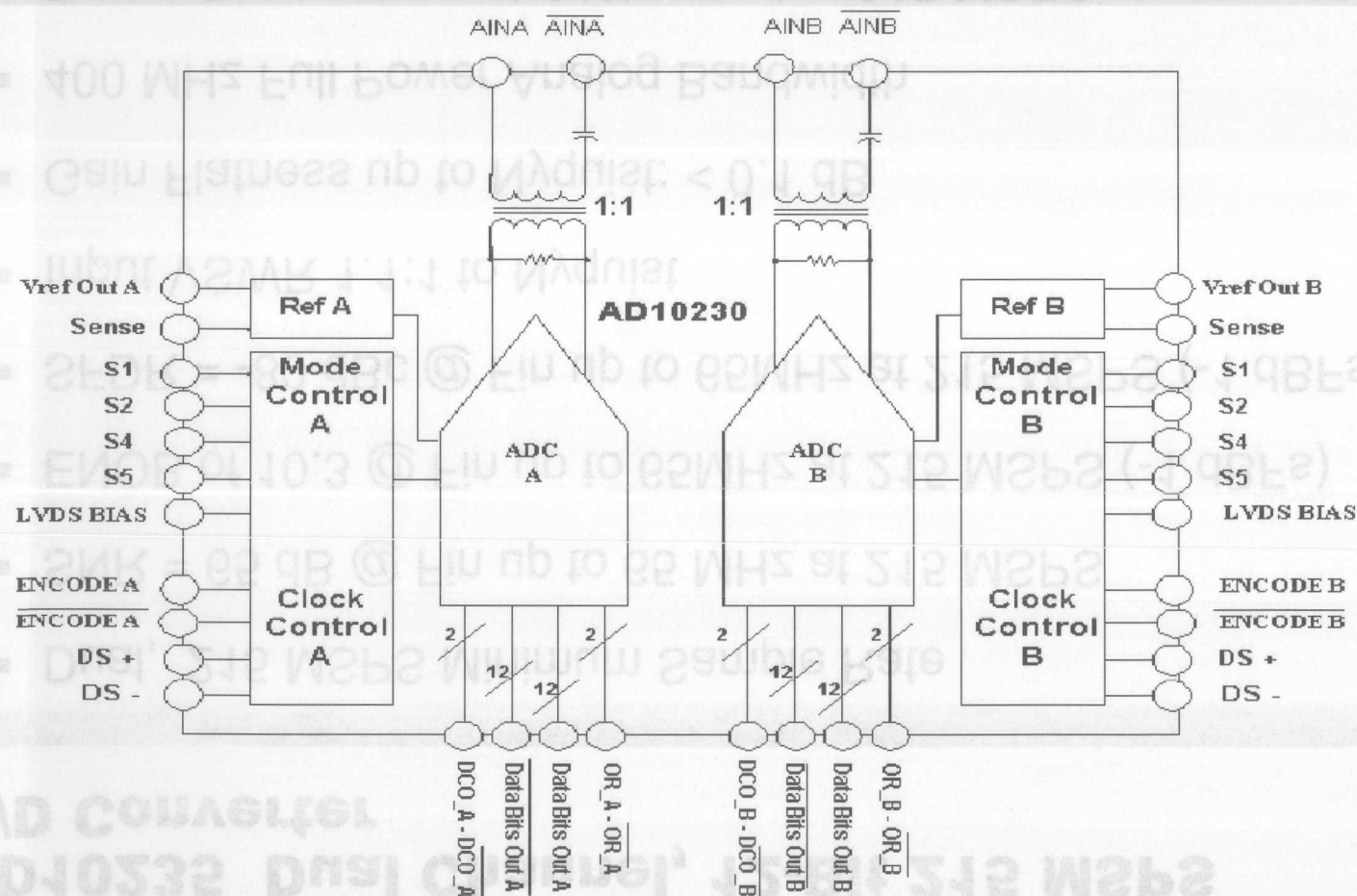
AD10230 Dual Channel, 12-Bit 170 MSPS A/D Converter

- Dual, 170 MSPS Minimum Sample Rate
- SNR = 65 dB @ F_{in} up to 65 MHz at 170 MSPS
- ENOB of 10.3 @ F_{in} up to 65MHz at 170 MSPS (-1 dBFS)
- SFDR = -80 dBc @ F_{in} up to 65MHz at 170 MSPS (-1 dBFS)
- Input VSWR 1.1:1 to Nyquist
- Gain Flatness up to Nyquist: < 0.1 dB
- 400 MHz Full Power Analog Bandwidth
- Power dissipation = 1.3 W typical at 170 MSPS
- 1.5 V Input Voltage Range

AD10230 Dual Channel, 12-Bit 170 MSPS A/D Converter

- LVDS Digital Output Data
- Output Data Format Option
- Data Sync Input and Data Clock Output Provided
- Interleaved or Parallel Data Output Option
- $ENOB = 10.3$ @ F_{IN} up to $65MHz$ at 170 MSPS (-1 qBFS)
- $SINR = 62$ qB @ F_{IN} up to 65 MHz at 170 MSPS
- Dual, 170 MSPS Minimum Sample Rate

AD10235 Dual Channel, 12-Bit 215 MSPS A/D Converter



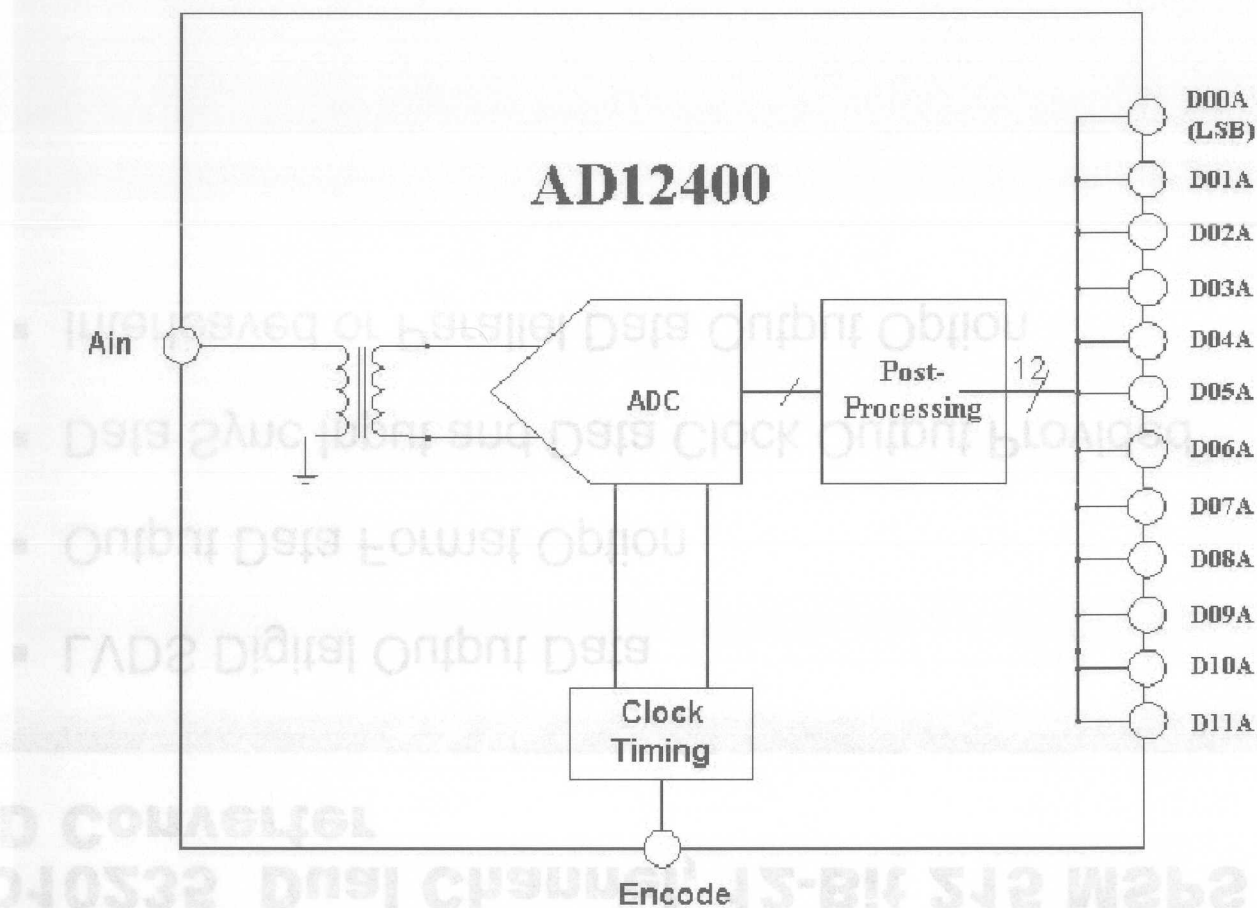
AD10235 Dual Channel, 12-Bit 215 MSPS A/D Converter

- Dual, 215 MSPS Minimum Sample Rate
- SNR = 65 dB @ F_{in} up to 65 MHz at 215 MSPS
- ENOB of 10.3 @ F_{in} up to 65MHz at 215 MSPS (-1 dBFs)
- SFDR = -80 dBc @ F_{in} up to 65MHz at 215 MSPS (-1 dBFs)
- Input VSWR 1.1:1 to Nyquist
- Gain Flatness up to Nyquist: < 0.1 dB
- 400 MHz Full Power Analog Bandwidth
- Power Dissipation = 1.3 W typical at 215 MSPS
- 1.5 V Input Voltage Range

AD10235 Dual Channel, 12-Bit 215 MSPS A/D Converter

- LVDS Digital Output Data
- Output Data Format Option
- Data Sync Input and Data Clock Output Provided
- Interleaved or Parallel Data Output Option

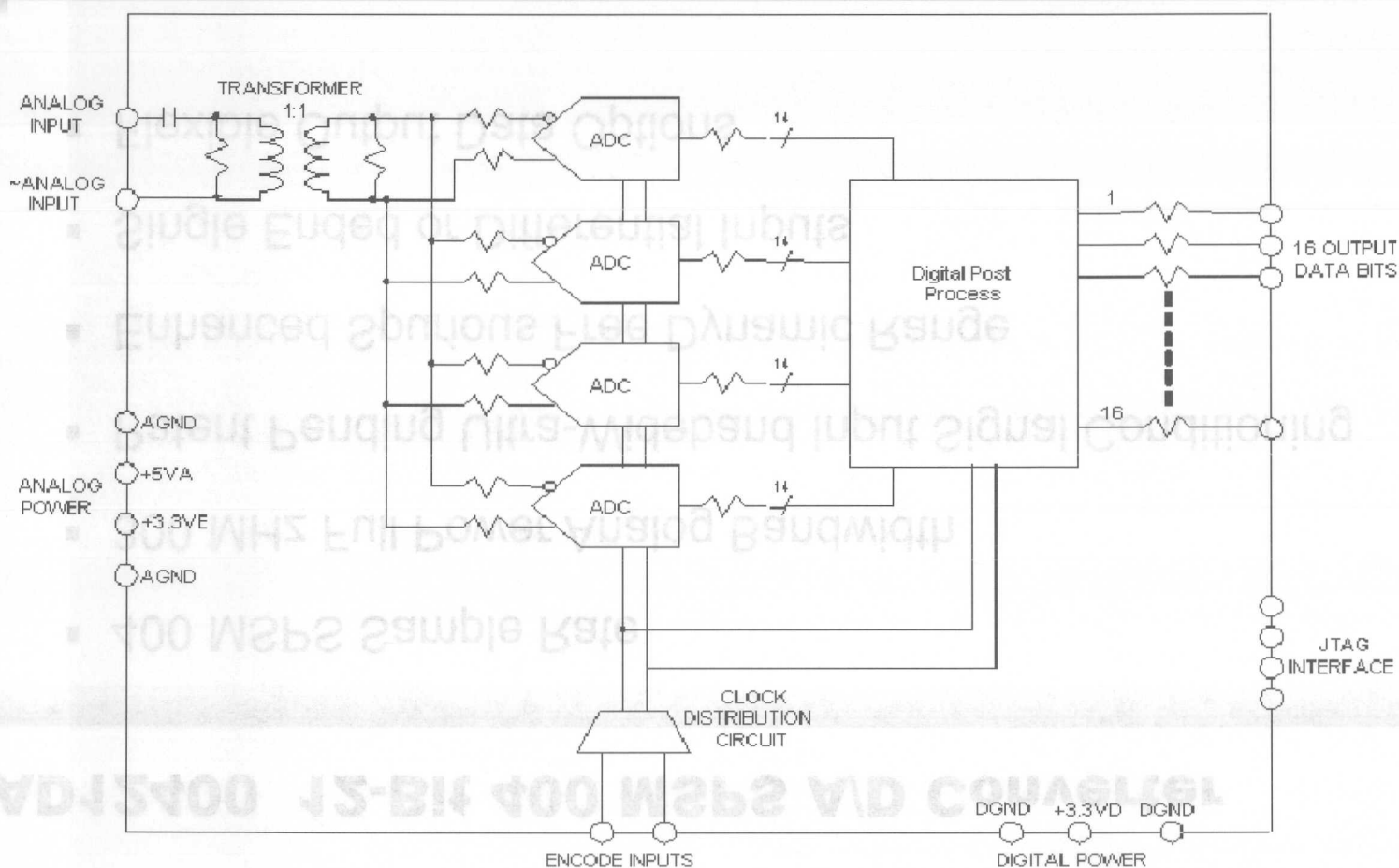
AD12400 12-Bit 400 MSPS A/D Converter



AD12400 12-Bit 400 MSPS A/D Converter

- 400 MSPS Sample Rate
- 300 MHz Full Power Analog Bandwidth
- Patent Pending Ultra-Wideband Input Signal Conditioning
- Enhanced Spurious Free Dynamic Range
- Single Ended or Differential Inputs
- Flexible Output Data Options

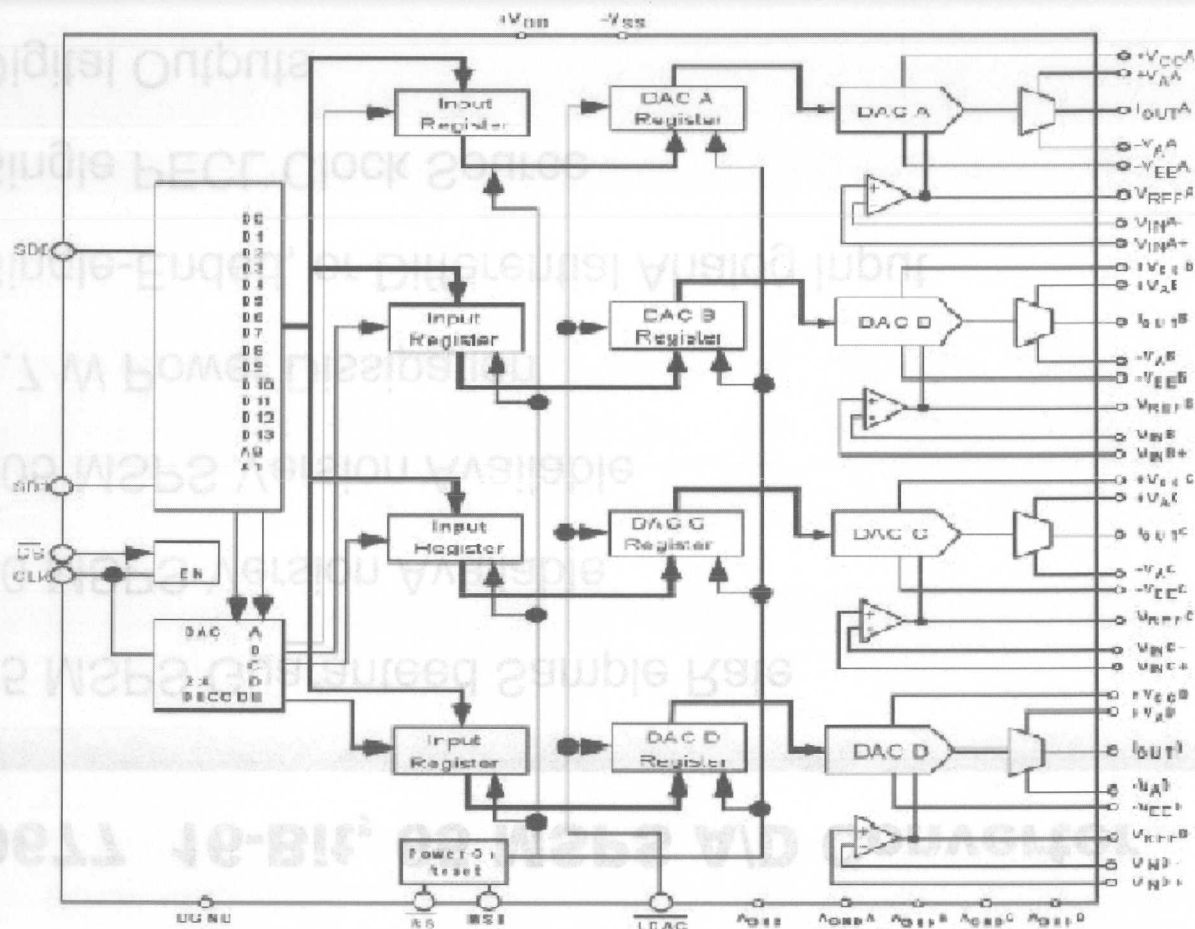
AD10677 16-Bit, 65 MSPS A/D Converter



AD10677 16-Bit, 65 MSPS A/D Converter

- 65 MSPS Guaranteed Sample Rate
- 80 MSPS Version Available
- 105 MSPS Version Available
- 7.7 W Power Dissipation
- Single-Ended, or Differential Analog Input
- Single PECL Clock Source
- Digital Outputs
- True Binary Format
- 3.3 V & 5 V CMOS-Compatible

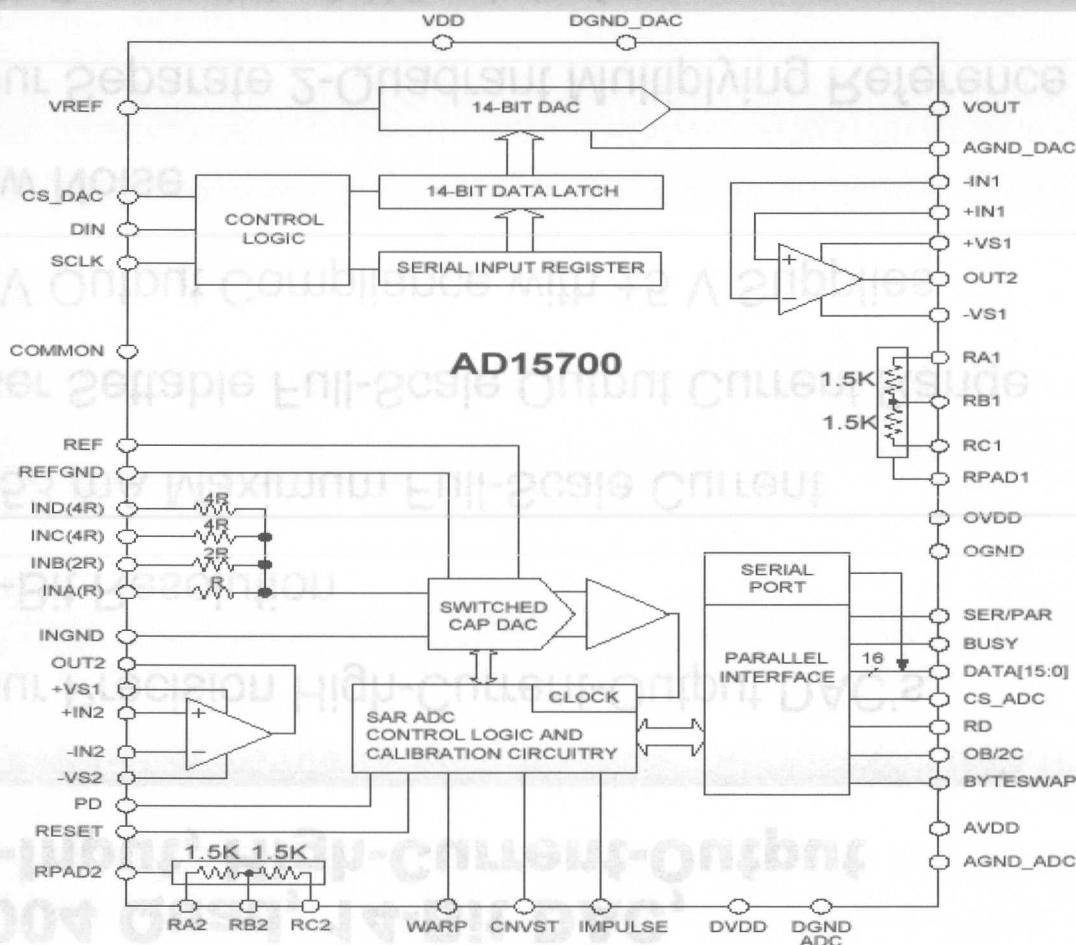
AD15004 Quad, 14-Bit DAC, Serial-Input, High-Current-Output



AD15004 Quad, 14-Bit DAC, Serial-Input, High-Current-Output

- Four Precision High-Current-Output DAC's
- 14-Bit Resolution
- ± 253 mA Maximum Full-Scale Current
- User Settable Full-Scale Output Current Range
- ± 3 V Output Compliance with ± 5 V Supplies
- Low Noise
- Four Separate 2-Quadrant Multiplying Reference Inputs
- SPI-Compatible 3-Wire Interface

AD15700 1 MSPS 16-/14-Bit Analog I/O Port



AD15700 1 MSPS 16-/14-Bit Analog I/O Port

- 16-Bit 1 MSPS A/D Converter
 - S/(N+D): 90 dB Typ @ 250 KHz
- 14-Bit D/A Converter
 - Settling Time: 1 μ s
 - S/N: 92 dB Typ
- Two 80 MHz Amplifiers
- 30 V/ μ s Slew Rate
- Rail-to-Rail Input and Output
- Two Gain Setting Center Tapped Resistors
- Resistor Ratio Tracking: 2 ppm/ $^{\circ}$ C
- Unipolar Operation
- 132 mW Typical Power Dissipation



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PRELIMINARY DATA

10-31

- 135 mW Typical Power Dissipation
- Unipolar Operation
- Resistor Ratio Tacking: $\pm 0.1\%$
- Two Gain Setting Center Tapped Resistors
- Rail-to-Rail Input and Output
- 30 V/s Slew Rate
- Two 80 MHz Amplifiers
 - $g_{m1} = 25 \mu S$
 - Settling Time: 1 μs
- 14-Bit D/A Converter
 - $2(N+1) = 20 \mu V$ @ 520 KHz
- 10-Bit 1 MS/s A/D Converter

AD2200 1 MS/s 10-14-Bit Analog I/O



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